AN11416

1900 MHz low noise, high linearity amplifier using BGU8052

Rev. 1.2 — 01 April 2019 Application note

Document information

Info	Content
Keywords	BGU8052, 1900 MHz, LNA, BTS
Abstract	This document provides circuit schematic, layout, BOM and typical EVB performance for a 1900 MHz LNA. For wireless infrastructure applications.
Ordering info	Evaluation kit number: OM7956, Including 2 BGU8052 1900 MHz LNAs, 1 for FDD and 1 for TDD. 12NC: 9340 679 14598
Contact information	For more information, please visit: http://www.nxp.com

Revision history

Rev	Date	Description
1	20131202	First publication
1.2	20190401	Update on k-factor improvement

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1. Introduction

NXPs semiconductors BGU805x series is a new family of integrated low noise amplifiers for the 300 MHz to 4 GHz range. The series consists of the:

- BGU8051 recommended for 300 MHz - 1500 MHz
- BGU8052 recommended for 1500 MHz – 2500 MHz
- BGU8053 recommended for 2000 MHz – 4000 MHz

The BGU805X series is a low noise high linearity amplifier family intended for wireless infrastructure applications like BTS, RRH, small cells, but can also be used in other general low noise applications, e.g. active antennas for automotive.

Being manufactured in NXPs high performance QUBiC RF Gen 8 SiGe:C technology, the BGU805X combines high gain, ultra-low noise and high linearity with the process stability and ruggedness which are the characteristics of SiGe:C technology.

BGU805X series comes in the industry standard 2 x 2 x 0.75 mm 8 terminal plastic thin small outline package HVSON8 (SOT1327). The LNA is ESD protected on all terminals.

This application note demonstrates of the BGU8052 applied in a 1900MHz LNA for wireless infrastructure applications. In Fig 1 the evaluation board is shown which is described in this application note.

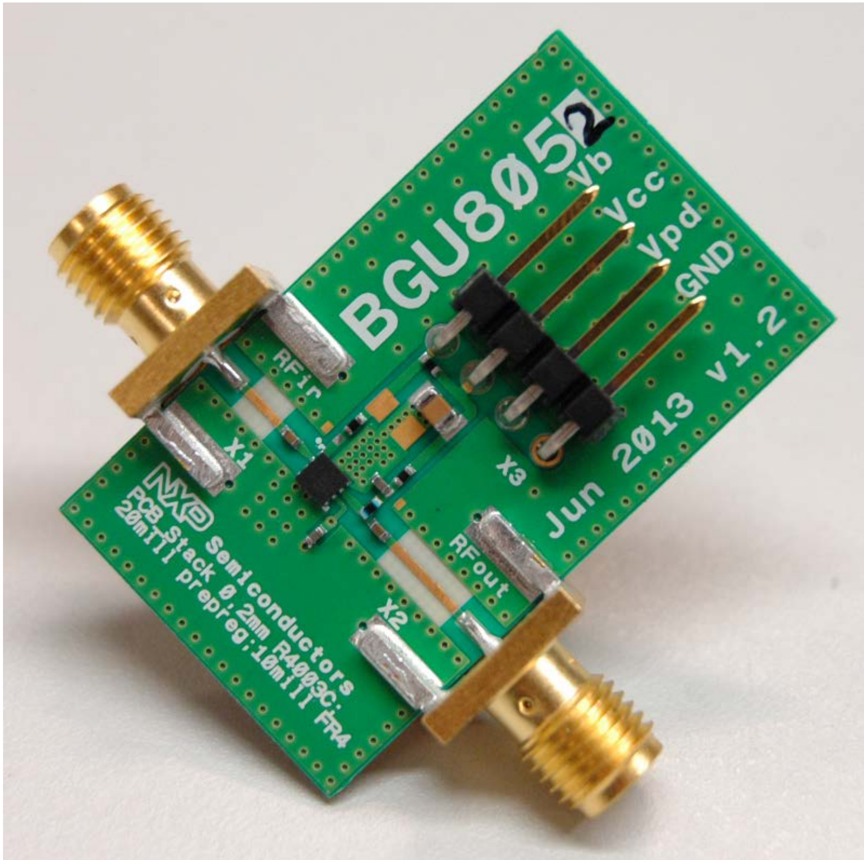


Fig 1. Evaluation board.

The BGU8052 evaluation board is fabricated on a 35 x 20 mm 1mm thick 3 layer PCB that uses 0.2 mm (8 mill) R4003C for the RF performance. The board is fully assembled with the BGU8052, including the external components. The board is supplied with two SMA connectors to connect input and output to the RF test equipment. The EVBs are also enabled with the possibility to evaluate the BGU8052 at different bias currents.

2. Product description

The BGU8052 is a fully integrated low noise amplifier with integrated bias circuit. The MMIC is internally matched to 50 Ω. The BGU8052 also features an integrated shutdown circuit to enable fast turn on/off settling time, enabling switched (time domain duplexing TDD) applications. The device bias current can be set by the value of an external bias resistor R_{BIAS}, which connects the supply voltage to the V_{BIAS} pin, or by an external control voltage applied directly to V_{BIAS} pin 1. This adjustable bias current gives flexibility in biasing the device for the optimum performance on NF or linearity. This feature can be useful in case more than one BGU8052 are cascaded. This bias resistor value changes the bias current directly which can be used to trade of linearity for power saving in battery operated applications.

The BGU8052 key features and benefits at 1900MHz are;

- Low noise performance: NF = 0.51 dB
- High linearity performance: $IP3_O$ = 37 dBm
- High input return loss RL_{in} > 15 dB
- High out return loss RL_{out} > 20dB
- Unconditionally stable up to 20 GHz
- Max RF input power of +20 dBm
- ESD protection on all pins
- Fast shutdown for TDD system.

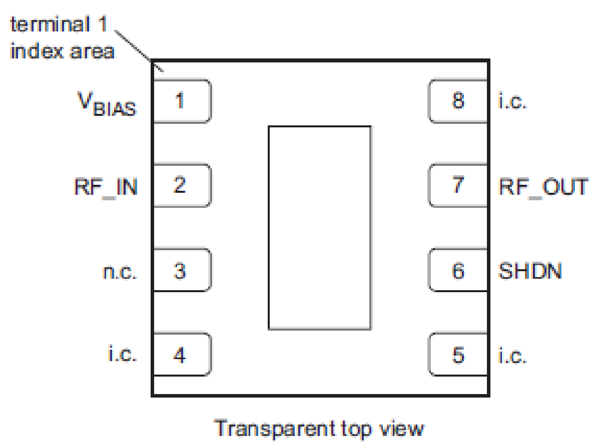


Fig 2. Pin description

In Fig 2 the pin out of the BGU8052 is given, the n.c. and i.c pin are recommended to connect to ground, which is the case on the evaluation boards.

3. Application board

3.1 Application circuit

The application board circuit diagram that is implemented on the EVB is shown in Fig 3

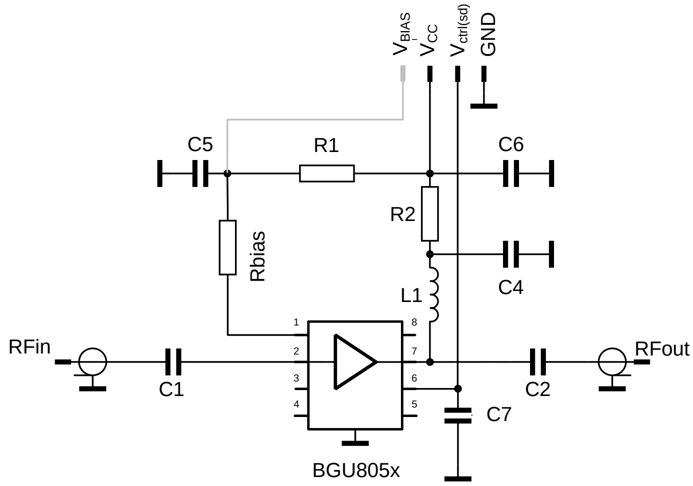
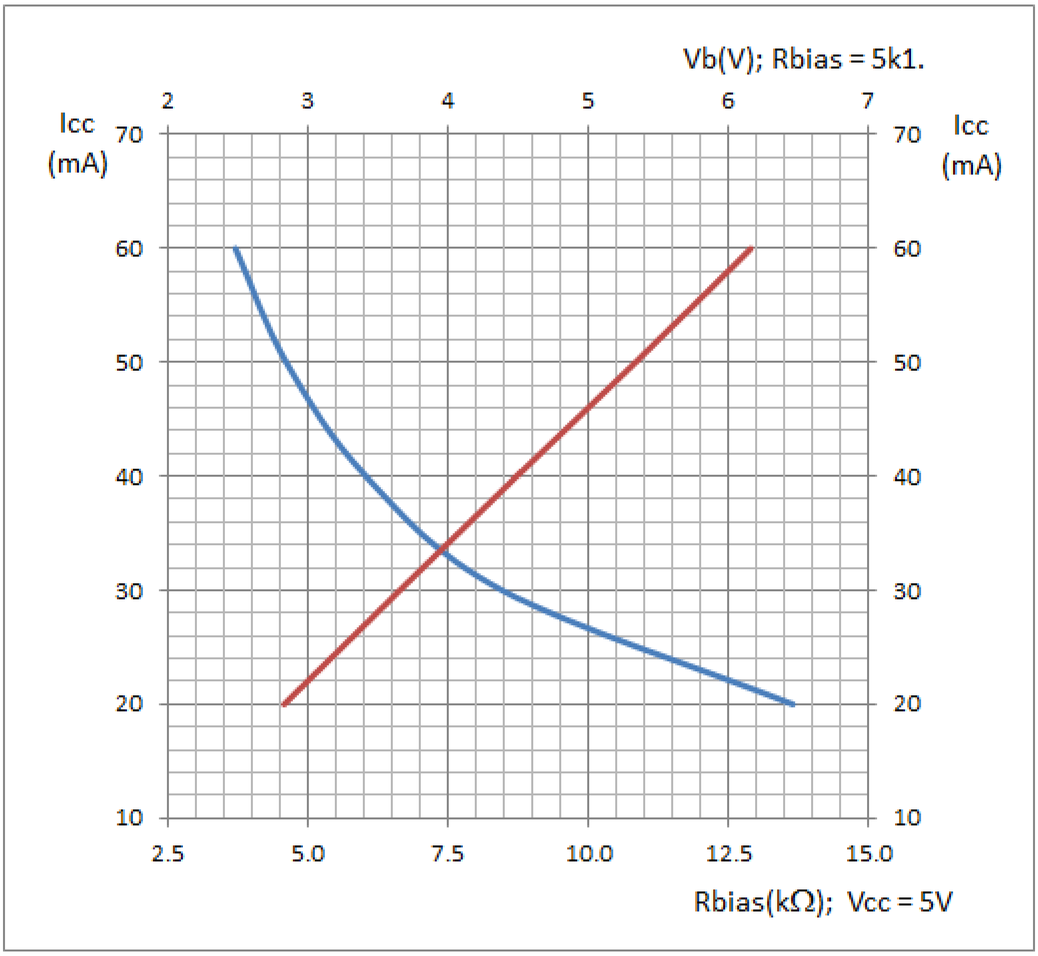


Fig 3. Application board circuit diagram

As stated before the bias current of the BGU8052 can be set by the value of an external resistor R_{BIAS}. The evaluation boards are supplied with a 5.1 kΩ bias resistor (I_{CC} = 48 mA +/-5 mA). If however it is required to evaluate the BGU8052 at different bias currents, resistor R1 which is 0 Ω can be removed and an external control voltage can be applied to V_{BIAS} (V_b pin) on the bias header, see Fig 3.

By applying this separate bias voltage on the V_{BIAS} pin of the bias header, the I_{CC} current can be swept without changing R_{BIAS}. With bias voltage window from 4 to 6 V on V_b while keeping the V_{CC} pin on 5 V, I_{CC} can be varied from 30-60 mA. In Fig 4 the relation between I_{cc} and R_{BIAS} at V_{CC} = 5 V as well as the relation between I_{CC} and V_b with R_{BIAS} = 5k1 is shown.



(1) Blue curve corresponds with the left Y axis and the lower X axis. Giving the I_{CC} versus the value of R_{BIAS}.

(2) Red curve corresponds with the right Y axis and the upper X axis. Giving the I_{CC} versus the voltage applied to the V_b pin with R_{BIAS} = 5k1 in place.

Fig 4. Relation of I_{CC} with R_{BIAS} and V_b

3.2 PCB Layout information

A good PCB layout is an essential part of an RF circuit design. The LNA evaluation board of the BGU8052 can serve as a guideline for laying out a board using the BGU8052. The evaluation board uses micro strip coplanar ground structures for controlled impedance lines for the high frequency input and output. V_{cc} is bypassed by C4 and C6 decoupling capacitors, C4 preferably should be located as close as possible to the device, to avoid AC leakage via the bias lines. For long bias lines it may be necessary to add decoupling capacitors along the line further away from the device. The self-resonance frequency of inductor L1 should be chosen above f0 for good choking. In this case the Murata LQW 15 series has been used. Proper grounding of the GND pins is also essential for good RF performance. Either connect the GND pins directly to the ground plane or through vias, or do both, which is recommended. The layout and component placement of the BGU8052 evaluation board is given in Fig 5

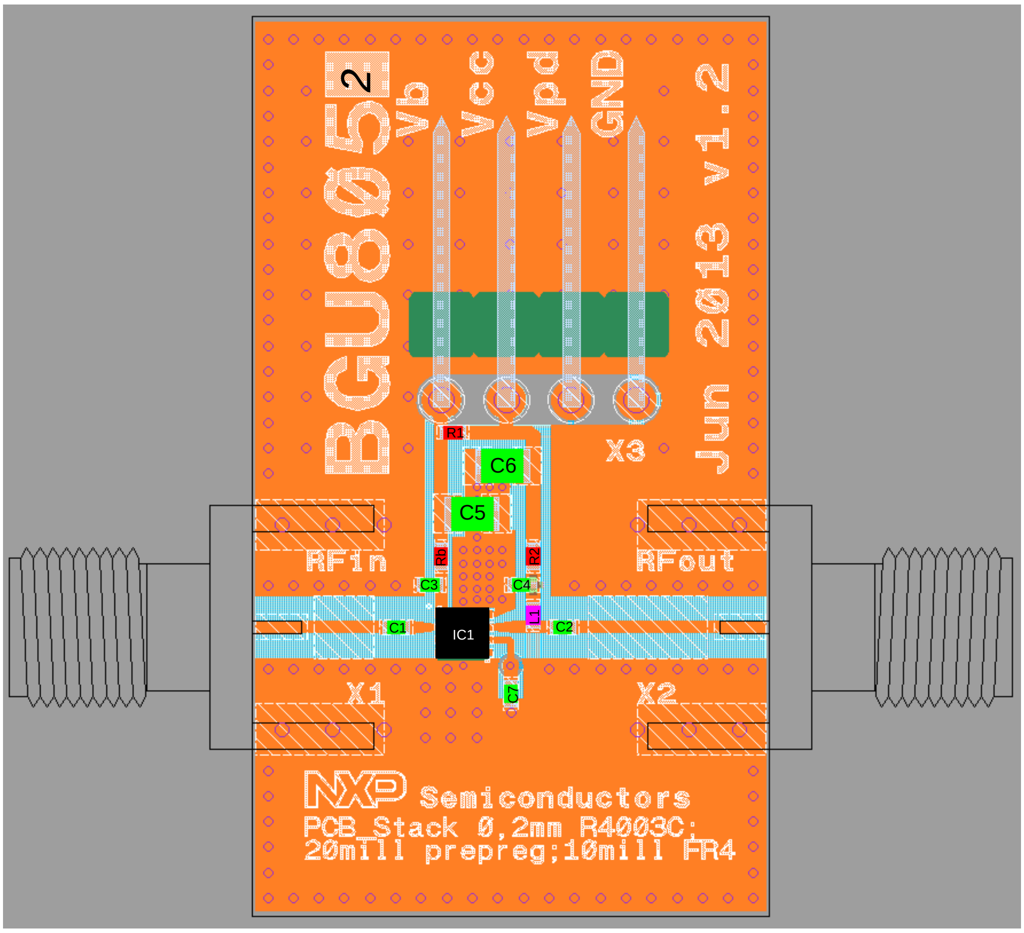
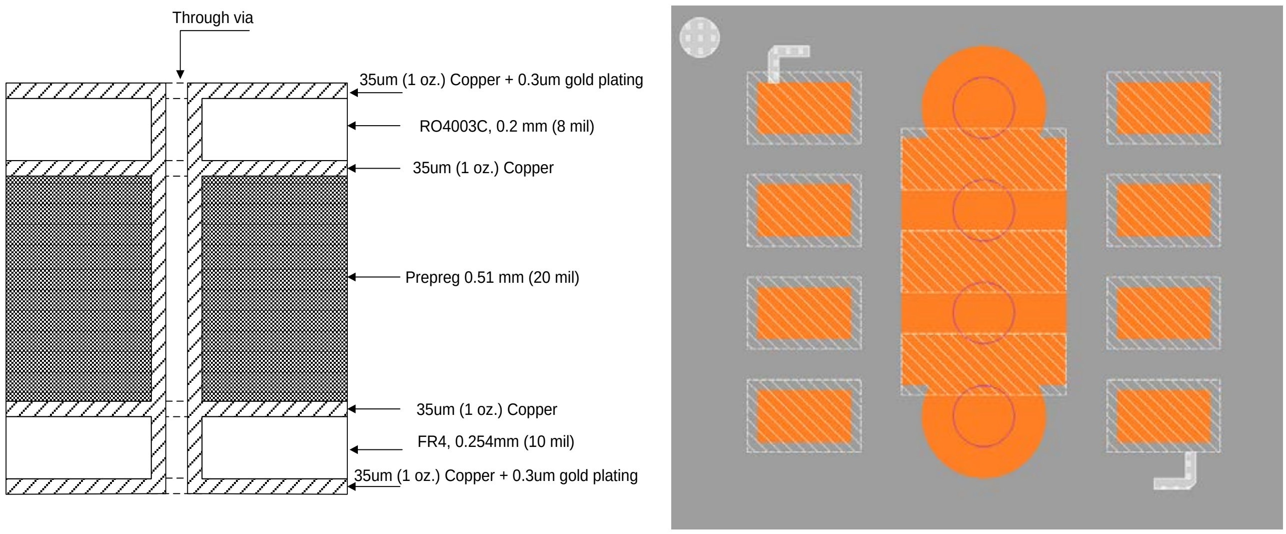


Fig 5. BGU8052 1900MHz evaluation board component placement

3.2.1 PCB stack and recommended footprint.

The PCB material used to implement the LNA is a 0.2 mm (8 mil) RO4003C low loss printed circuit board which is merged to a 0.51 mm (20 mil) prepreg and a 0.254 mm (10 mil) FR4 layer for mechanical stiffness. See Fig 6a

The official drawing of the recommended footprint can be found via following link, sot1327-1_fr.pdf. If micro strip coplanar PCB technology is used it is recommended to use at least 4 ground-via holes of 300um this is also used on the EVBs as shown in Fig 6b.



a. Cross section of the PCB Layer stack.

b. Recommended footprint.

Fig 6. PCB stack and footprint information.

3.3 Bill of materials

Table 1 gives the bill of materials as is used on the EVB for non-switching applications. In paragraph 5 the differences in the BOM related to switched (TDD) applications are given.

Table 1. BOM

Designator	Description	Footprint	Value	Supplier Name/type	Comment/function
IC1	BGU8052				
PCB	20x35x1mm				RO4003C
C1,C2	Capacitor	0402	100nF	Various	DC block
C4	Capacitor	0402	10pF	Various	RF decoupling
C5	Capacitor	0806	4.7uF	Various	Optional
C6	Capacitor	0806	4.7uF	Various	LF Decoupling
C7	Capacitor	0402	100pF	Various	Decoupling
L1	Inductor	0402	15nH	Murata LQW15	Bias choke/Output match
R1	Resistor	0402	0Ohm	Various	
R2	Resistor	0402	10Ohm	Various	stability
Rbias	Resistor	0402	5k1	Various	Bias setting
X1,X2	SMA RF connector			Johnson, End launch SMA 142-0701-841	RF connections
X3	DC header			Molex, PCB header, right angle, 1 row 4 way	DC connections

4. Typical application board results

4.1 Typical board performance

The values given in Table 2 are typical values of >25 boards measured.

Table 2. Typical board performance using the BOM for non-switched applications, unless otherwise indicated.
F=1900MHz; Vcc=5V;T_{amb}=25°C; input and output 50Ω;R_{bias}=5.1kΩ.

Symbol	Parameter	Conditions		Typ	Unit
I_{cc}	Supply current			48	mA
G_{ass}	Associated gain			18.4	dB
NF	Noise figure			0.52	dB
$P_{L((1dB)}$	Output power at 1dB gain compression			18.3	dBm
$IP3_O$	Output third-order intercept point	2-tone; tone spacing = 1MHz; P_i = -15dBm per tone		37	dBm
RL_{in}	Input return loss			15	dB
RL_{out}	Output return loss			21.5	dB
ISL	Isolation			23	dB
$T_{s(pon)}$	Power-on settling time	P_i = -20dBm; SHDN(pin 6) from High to Low	[1]	1.5	µs
$T_{s(poff)}$	Power-off settling time	P_i = -20dBm; SHDN(pin 6) from Low to High	[1]	0.04	µs

[1] The power on/off settling time has been measured on the boards with the BOM for switched applications, C1 and C2 are 100pF.

4.2 S_Parameter,1dB compression, IIP3, measurement setup

The BGU8052 EVBs are fully assembled and tested.

Fig 7 Shows the measurements setup that is used to evaluate the BGU8052 EVB for S_parameters (G_{ass}, RL_{in}, RL_{out}, and ISL), 1dB gain compression as well as OIP3. It is intended as a guide only, substitutions are possible.

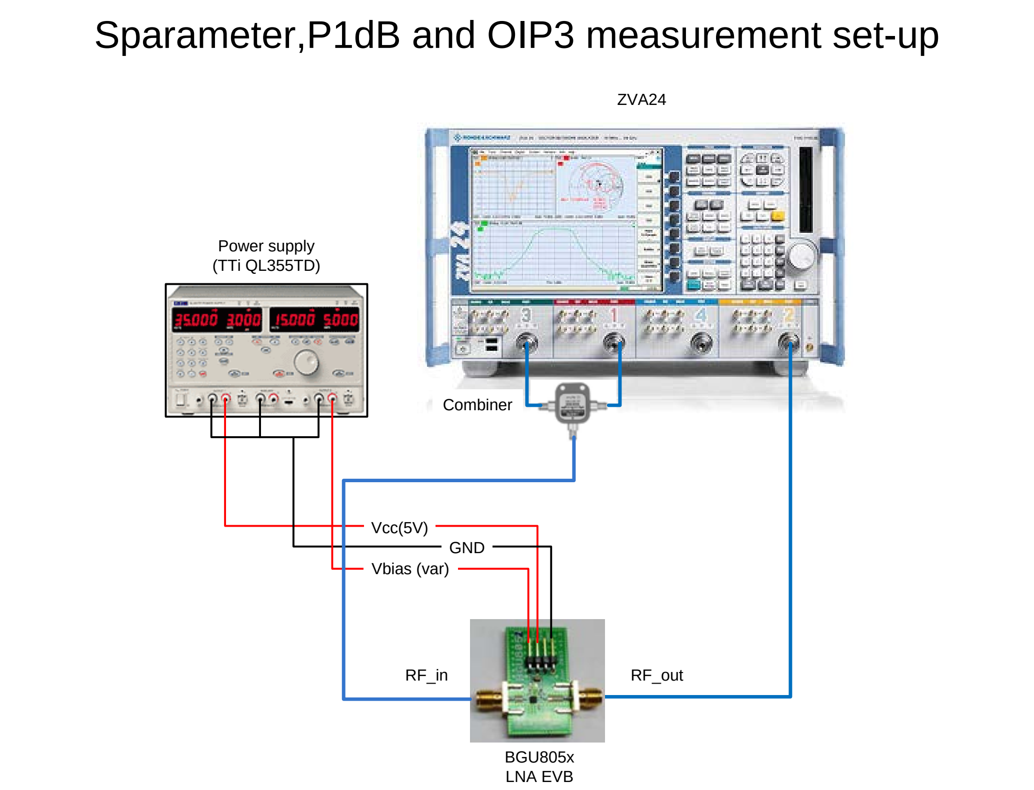
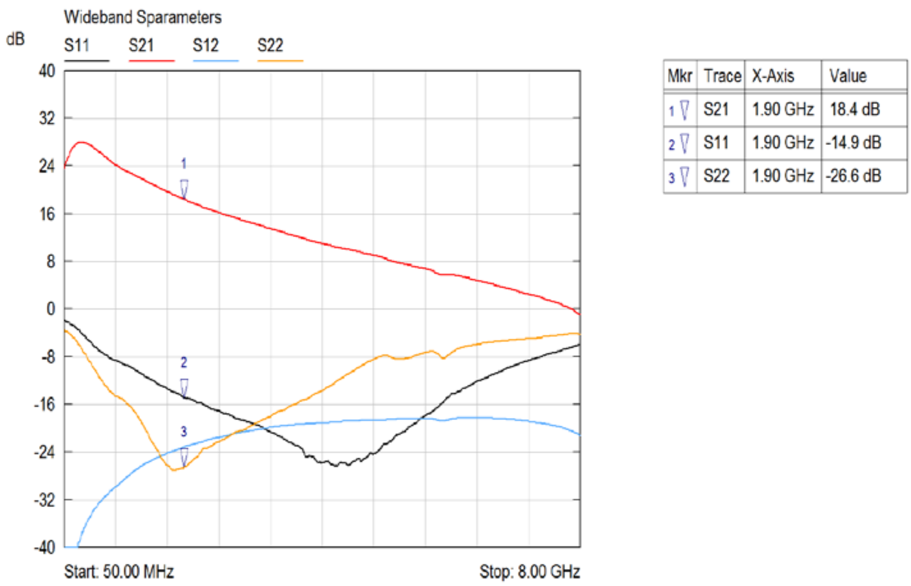


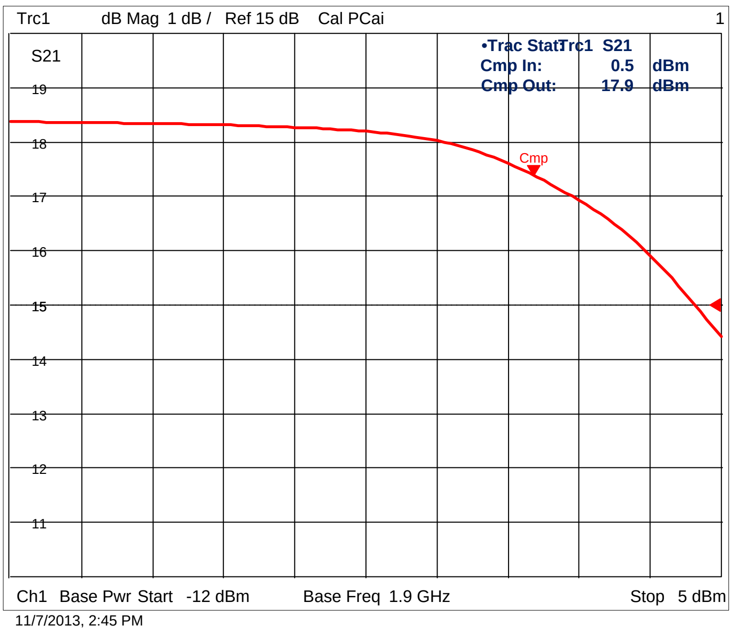
Fig 7. S_parameter, 1dB compression and IP3 measurement setup

Fig 8 shows the typical wide band S parameter measured on the BGU8052 EVB. The 1dB gain compression curve is shown in Fig 9.



V_{CC} = 5V; T_{AMB} = 25 °C; I_{CC} = 48mA

Fig 8. S-parameters as function of frequency.



(1) V_{CC} = 5V; T_{AMB} = 25 °C; I_{CC} = 48mA

(2) P_i1dB = 0.5dBm; P_L1dB = 17.9dBm

Fig 9. 1dB gain compression curve.

4.3 Noise figure measurement setup

In Fig 10 the noise figure measurement set-up is shown, this is also intended as a guide only, substitutions can be made. For noise levels of the BGU8052 which <1 dB it is recommended to perform the noise-measurements in a Faraday's cage or at least put the DUT in a shielded environment. This is recommended to avoid any interference of cellular frequencies that are in the same frequency range.

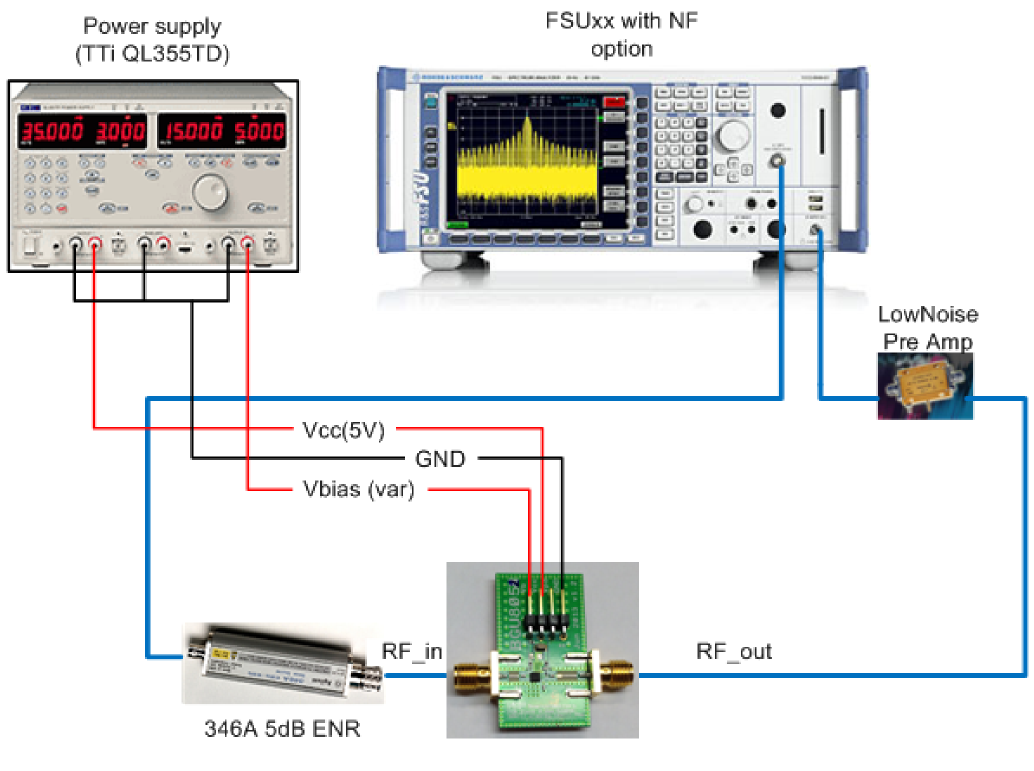
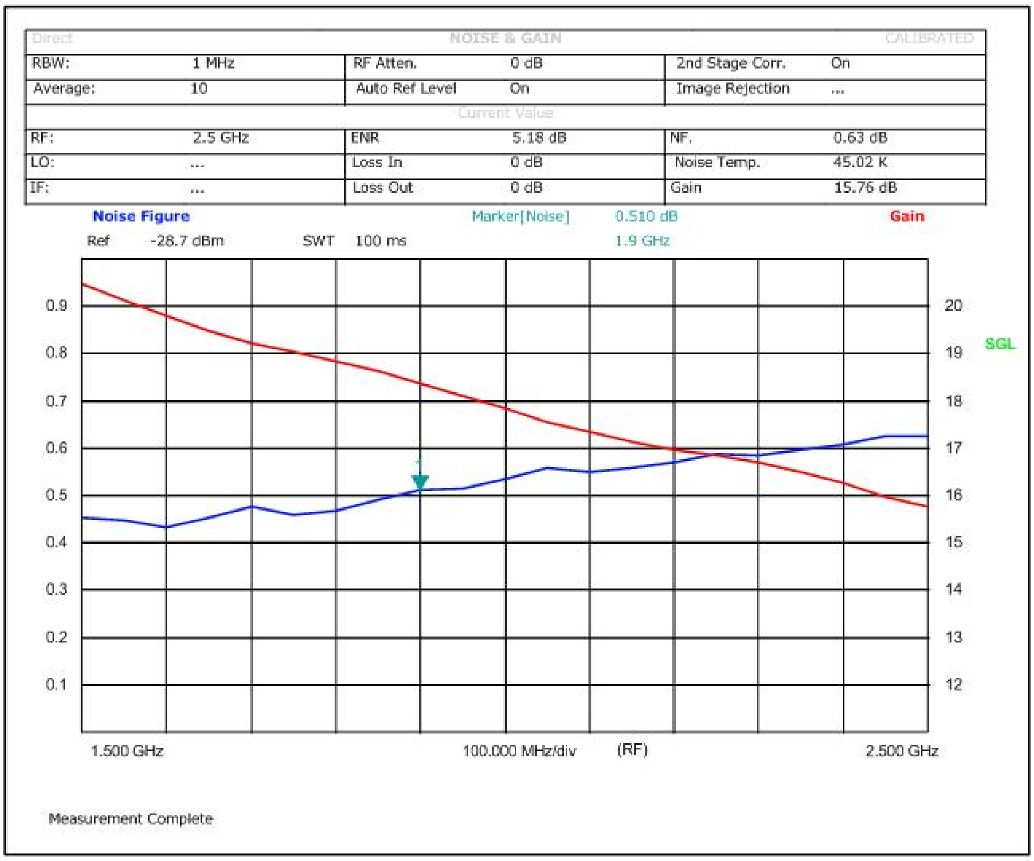


Fig 10. Noise figure test setup



V_{CC} = 5V; T_{AMB} = 25 °C; I_{CC} = 48mA

(1) Measured at the evaluation boards SMA connectors.

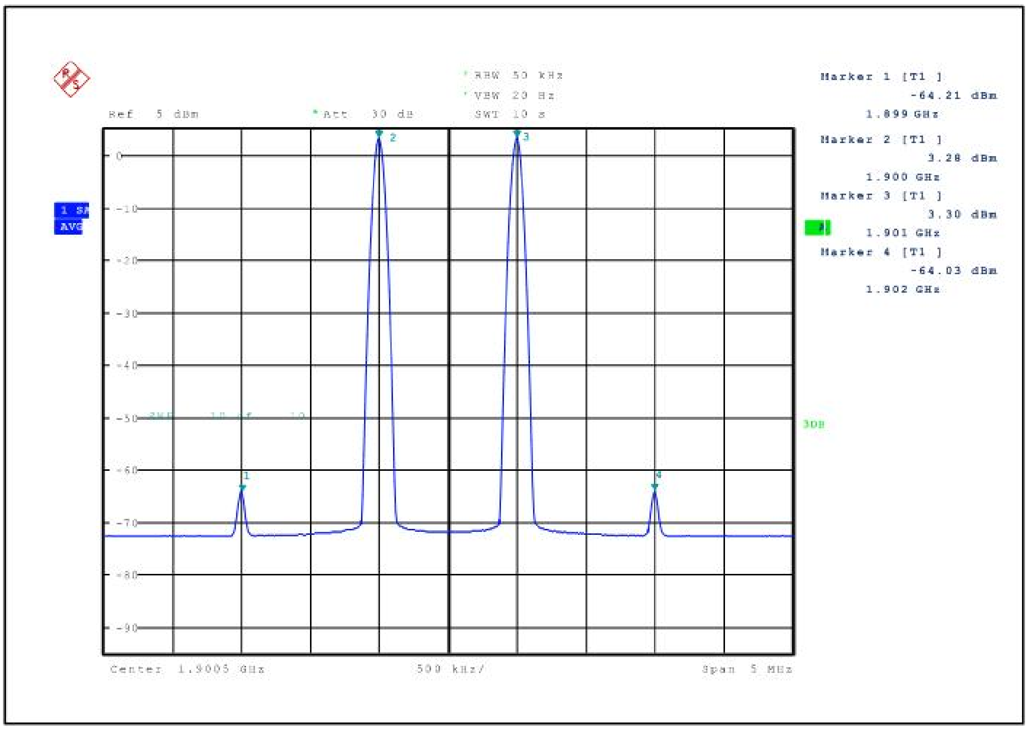
Fig 11. Typical noise figure performance versus frequency.

The noise figure shown in Fig 11 is measured using the setup shown in Fig 10 .A spectrum analyzer with noise option. A 5dB ENR noise source was used. To achieve the lowest possible setup noise-figure an external pre amplifier is also recommended.

The Noise figure value in Fig 11 is the value measured at the evaluation board SMA connectors. Correcting for the connector and PCB loss will end up in 0.05dB lower noise figure.

4.4 3rd order intercept point, output referred

The evaluation boards provided in the customer evaluation kit are automatically measured on linearity using the set-up shown in Fig 7. Alternatively the setup given in Fig 13 can be used, which is done for the spectrum plot in Fig 12.



(1) OIP3 LSB = (64.21+3.28)/2+3.28 = 37.0 dBm; OIP3 USB = (67.43+3.3)/2+3.3 = 37.0 dBm

(2) IIP3 = OIP3-Gain = 37 - 18.4 = 18.6dBm

Fig 12. Typical OIP3 spectrum

The bias choke L1 on the application board is determined empirically in order to get the best OIP3 as well as keeping good output return loss, S22. On the EVB for non-switching applications the values of C1 and C2 are chosen to be 100nF. Capacitors, C1 and C2 do not have any matching functionality, but are only required for DC blocking. In [1] the effect on linearity of SiGe BiCMOS BJTs and the advantage of using low source impedances at the low frequencies of the 2nd order mixing terms is described. These C1 and C2 being 100nF gives better 2nd order mixing suppression. However, for the applications were the LNA is switched with high switching frequencies and power on settling times of several micro seconds is required, the values of C1 has to be decreased to lower than 100pF which effects the IP3.

When measuring the high OIP3 values it is essential check the capabilities of the used measurement equipment. Be aware that the measurement set-up itself is not generating dominating IM3 levels. Advised is to do a back to back measurement without a DUT first.

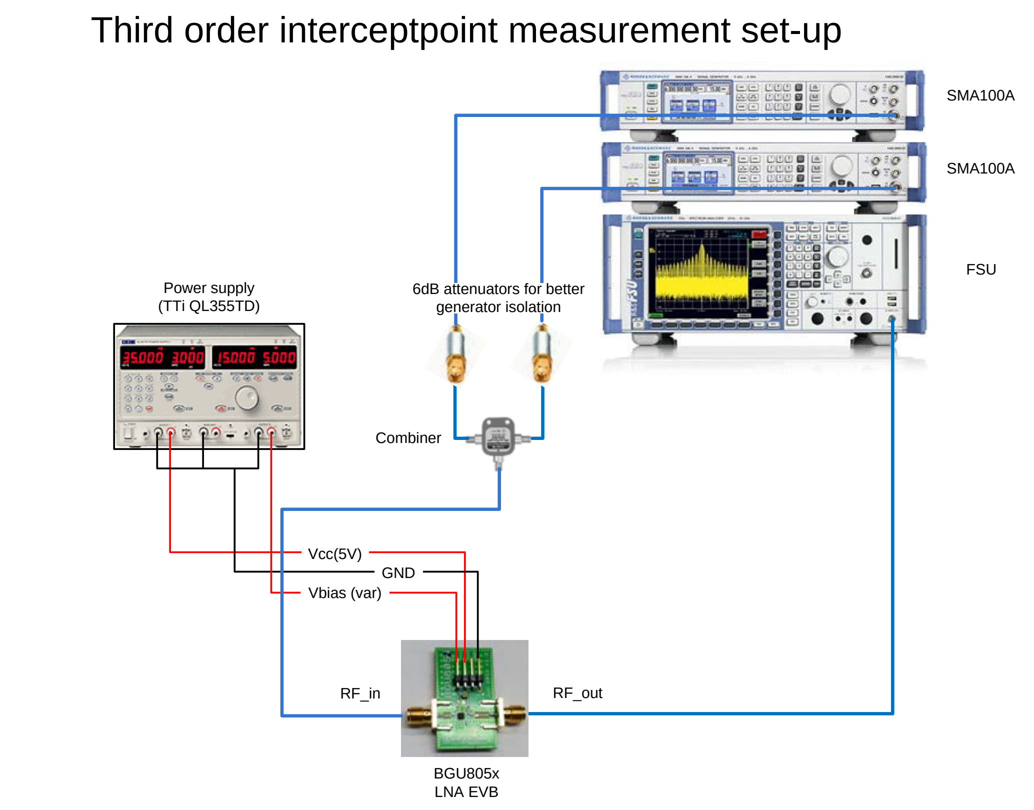
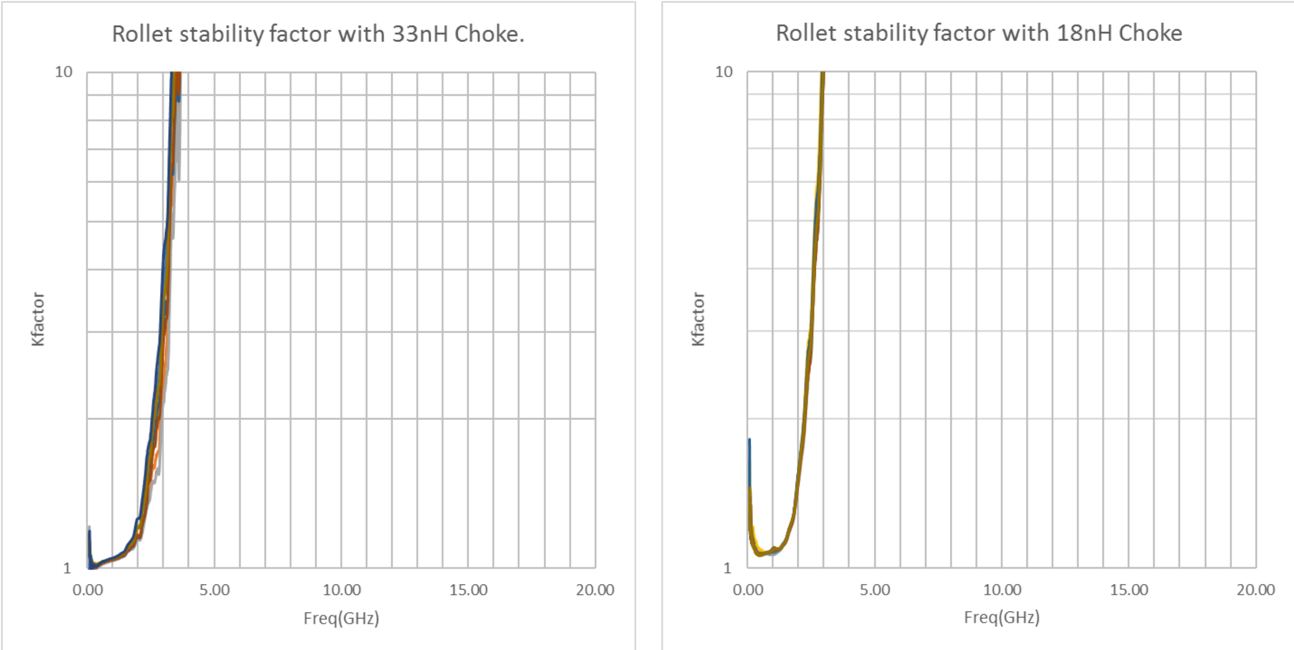


Fig 13. 2 tone OIP3 measurement setup

4.5 Stability Factor

The very high Gain at low frequencies might introduce potential instability issues, K-factor<1. Proper selection of the output bias choke together with the 10 Ohm resistance R1 can improve this. **Error! Reference source not found.** shows the rollet stability factor plots of the typical K factor with 33nH bias choke and 18nH. Please note this change of bias choke will affect the input and output match of the circuits.



a. b.

Fig 14. K factor improvement

5. BGU8052 applied in switched applications

5.1 Description

If the BGU8052 is used in switched applications both the SHDN pin as well as the V_{bias} pin can be used to apply a switch control voltage. It is preferred to use the SHDN pin.

Both pins require less than 1 mA driving current which means they are CMOS compatible. This enables LNA switching directly via a micro controller.

As stated before, if the BGU8052 is applied in time domain duplexing (TDD) kind of systems with requirements on the power on/off settling time, C1 needs to be decreased to ≤ 100 pF, in order to achieve a power on settling time of < 2 µs.

There is an alternative way of switching the LNA, by switching the overall supply. In this case the switching time is limited by the time constant created by C6 x R_{BIAS}. So additional to lowering the value of C1 the decoupling capacitor C6 (4.7 µF) also has to be decreased to values <10 nF. Please note that lowering the low frequency decoupling capacitor makes the circuit more sensitive to V_{CC} modulation of the 2[nd] order mixing products.

5.2 Measuring Power-on-off settling time

The circuit used to measure the power on/off settling time is shown in Fig 15. This can be used as e guidance to determine the power on/off settling time.

The waveform generator is used to provide the control voltage on either the SHDN pin (6) or the V_{BIAS} pin (1).

Set the waveform generator Agilent 33250 to square mode and the output amplitude to required voltage for the used control pin, with 50 ohm output impedance. Set the RF signal generator output level to -25dBm at 1900GHz and increase its level until the peak detector output level is about 5mV on 1mV/division, the signal generator RF output level is approximately -20 dBm.

A peak detector is needed to detect the high frequency AC signal at the output of the DUT, representing it as a DC voltage equal to the peak level of the applied AC signal.

It is very important to keep the cables as short as possible at input and output of the LNA so the propagation delay difference on cables between the two channels is minimized. It is also critical to set the oscilloscope input impedance to 50ohm on channel 2 so the diode detector can discharge quickly to avoid a false result on the Turn OFF time testing.

In case of switching the supply (V_{CC}) an additional PNP switching transistor circuit was used to drive the 48 mA I_{CC}. This circuit is controlled by the waveform generator.

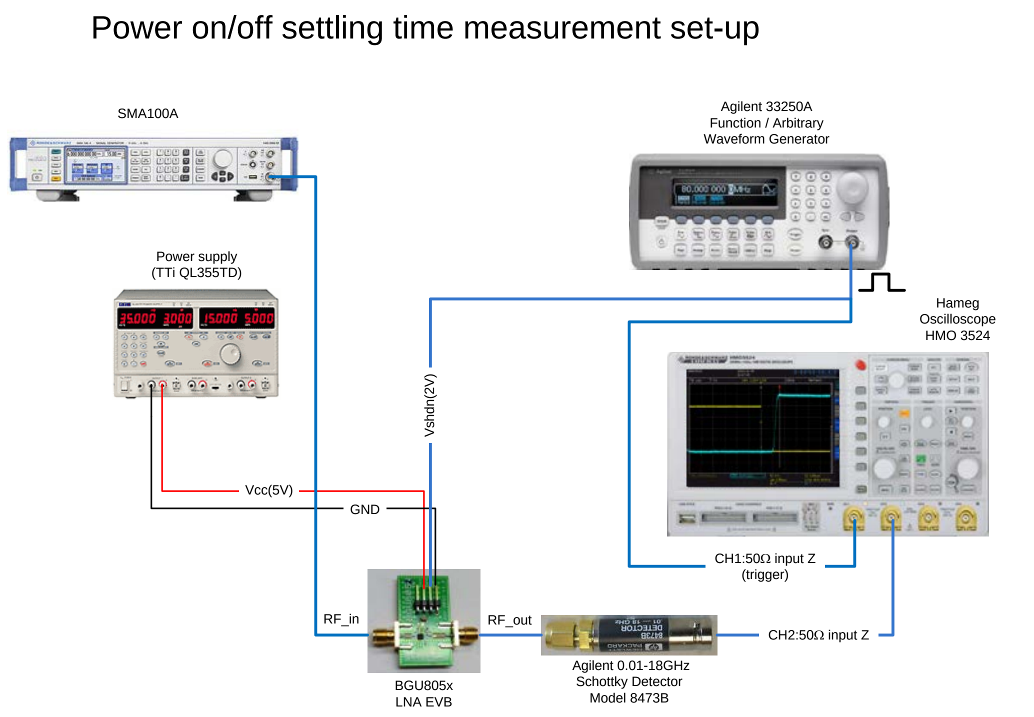


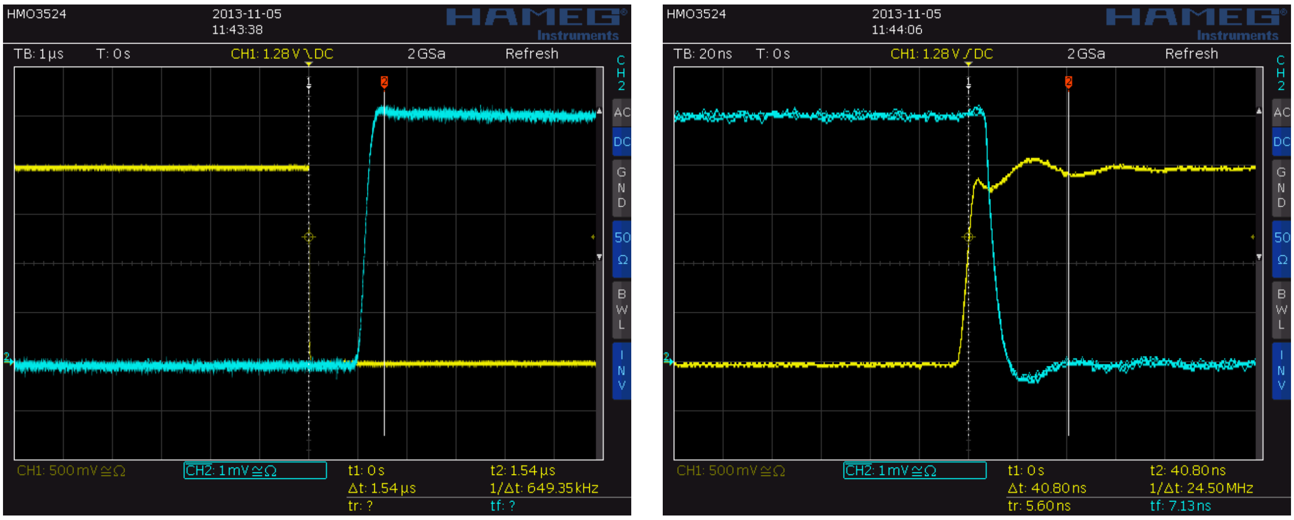
Fig 15. Power on/off settling time measurement setup.

Table 3. Typical power on/off settling time
Measured on BGU8052 EVB. C1=C2=100pF

Control pin	Power on	Power off	Units
SHDN	1.5	0.04	µs
V_{BIAS}	1.2	0.45	µs
V_{CC} [1]	2.1	0.75	µs

[1] C6 ≤ 10nF

Fig 16 to Fig 18 is showing power on/off settling time curves for the different control circuits.

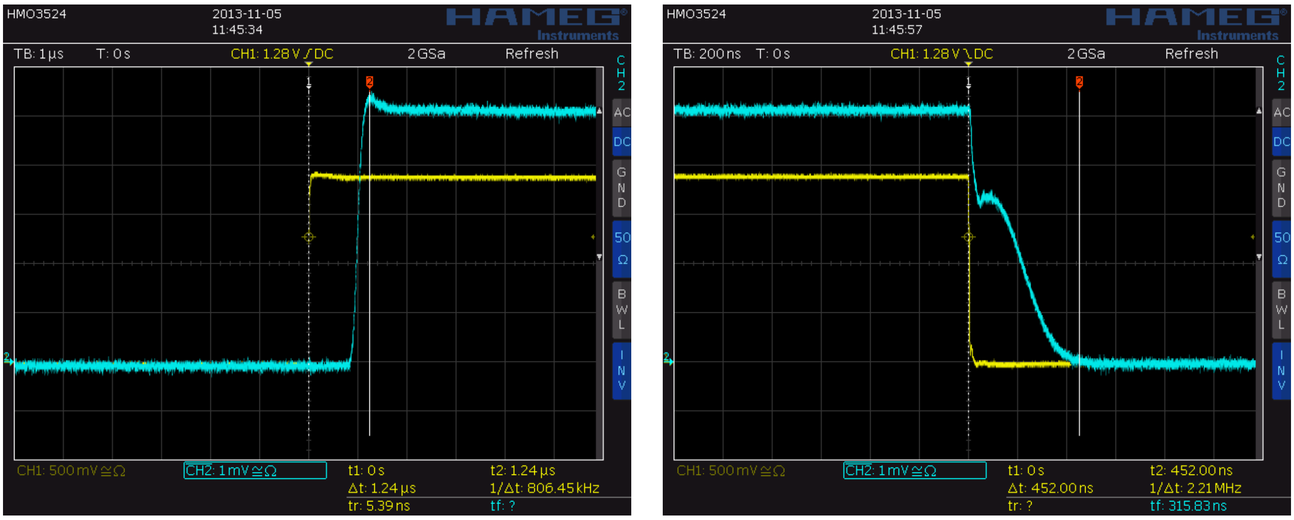


a. T_{on} 1.54 µs

b. T_{off} 40.8 ns

Yellow curve SHDN control voltage
Blue curve output of the detector diode

Fig 16. Power on/off settling time using the SHDN pin(6)

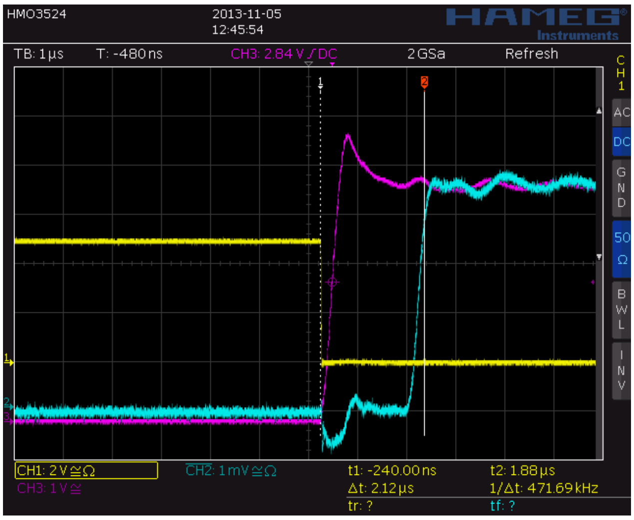


a. T_{on} 1.24 µs

b. T_{off} 452 ns

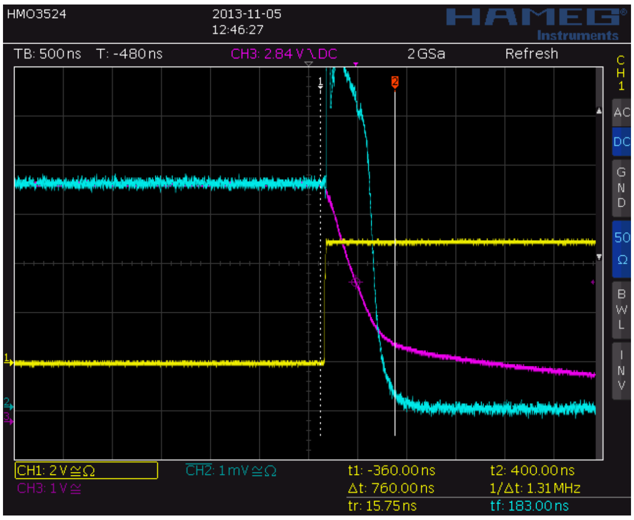
Yellow curve V_{BIAS} control voltage
Blue curve output of the detector diode

Fig 17. Power on/off settling time using the V_{BIAS} pin(1)



a. T_{on} 2.12µs

Yellow curve switch-circuit trigger-pulse.
Pink curve switched supply voltage.
Blue curve output of the detector diode



b. T_{off} 760 ns

Yellow curve switch-circuit trigger-pulse.
Pink curve switched supply voltage.
Blue curve output of the detector diode

Fig 18. Power on off settling time using the supply voltage.

6. References

[1] Vladimir Aparin, Lawrence E. Larson, "Linearization of monolithic LNAs Using Low-Frequency Low-Impedance Input Termination". IEEE 0-7 803-8 108-4/03 ©2003

7. Customer Evaluation Kit

In the customer evaluation kit you will find;

- 2 EVBs
- 10 loose samples.

On the back side of the boards it is indicated whether the board is meant for a fast switching applications TDD or for non-switching applications FDD. **Error! Reference source not found.** shows a picture of the customer evaluation kit.

Fig 19. Customer evaluation kit.

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9. List of figures

10. List of tables

11. Contents

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