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<td><strong>Keywords</strong></td>
<td>BGU8052, 1900 MHz, LNA, BTS</td>
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<tr>
<td><strong>Abstract</strong></td>
<td>This document provides circuit schematic, layout, BOM and typical EVB performance for a 1900 MHz LNA. For wireless infrastructure applications.</td>
</tr>
<tr>
<td><strong>Ordering info</strong></td>
<td>Evaluation kit number: OM7956, Including 2 BGU8052 1900 MHz LNAs, 1 for FDD and 1 for TDD. 12NC: 9340 679 14598</td>
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<tr>
<td><strong>Contact information</strong></td>
<td>For more information, please visit: <a href="http://www.nxp.com">http://www.nxp.com</a></td>
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Contact information

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1. Introduction

NXPs semiconductors BGU805x series is a new family of integrated low noise amplifiers for the 300 MHz to 4 GHz range. The series consists of the:

- BGU8051 recommended for 300 MHz - 1500 MHz
- BGU8052 recommended for 1500 MHz – 2500 MHz
- BGU8053 recommended for 2000 MHz – 4000 MHz

The BGU805X series is a low noise high linearity amplifier family intended for wireless infrastructure applications like BTS, RRH, small cells, but can also be used in other general low noise applications, e.g. active antennas for automotive.

Being manufactured in NXPs high performance QUBiC RF Gen 8 SiGe:C technology, the BGU805X combines high gain, ultra-low noise and high linearity with the process stability and ruggedness which are the characteristics of SiGe:C technology.

BGU805X series comes in the industry standard 2 x 2 x 0.75 mm 8 terminal plastic thin small outline package HVSON8 (SOT1327). The LNA is ESD protected on all terminals.

This application note demonstrates of the BGU8052 applied in a 1900MHz LNA for wireless infrastructure applications. In Fig.1 the evaluation board is shown which is described in this application note.

![Evaluation board](image_url)
The BGU8052 evaluation board is fabricated on a 35 x 20 mm 1mm thick 3 layer PCB that uses 0.2 mm (8 mill) R4003C for the RF performance. The board is fully assembled with the BGU8052, including the external components. The board is supplied with two SMA connectors to connect input and output to the RF test equipment. The EVBs are also enabled with the possibility to evaluate the BGU8052 at different bias currents.

2. Product description

The BGU8052 is a fully integrated low noise amplifier with integrated bias circuit. The MMIC is internally matched to 50 $\Omega$. The BGU8052 also features an integrated shutdown circuit to enable fast turn on/off settling time, enabling switched (time domain duplexing TDD) applications. The device bias current can be set by the value of an external bias resistor $R_{BIAS}$, which connects the supply voltage to the $V_{BIAS}$ pin, or by an external control voltage applied directly to $V_{BIAS}$ pin 1. This adjustable bias current gives flexibility in biasing the device for the optimum performance on NF or linearity. This feature can be useful in case more than one BGU8052 are cascaded. This bias resistor value changes the bias current directly which can be used to trade of linearity for power saving in battery operated applications.

The BGU8052 key features and benefits at 1900MHz are;

- Low noise performance: $NF = 0.51$ dB
- High linearity performance: $IP_{3O} = 37$ dBm
- High input return loss $RL_{in} > 15$ dB
- High out return loss $RL_{out} > 20$dB
- Unconditionally stable up to 20 GHz
- Max RF input power of $+20$ dBm
- ESD protection on all pins
- Fast shutdown for TDD system.

In Fig 2 the pin out of the BGU8052 is given, the n.c. and i.c pin are recommended to connect to ground, which is the case on the evaluation boards.
3. Application board

3.1 Application circuit

The application board circuit diagram that is implemented on the EVB is shown in Fig 3.

![Application board circuit diagram](image)

As stated before the bias current of the BGU8052 can be set by the value of an external resistor $R_{\text{BIAS}}$. The evaluation boards are supplied with a 5.1 kΩ bias resistor ($I_{\text{CC}} = 48$ mA $+/-5$ mA). If however it is required to evaluate the BGU8052 at different bias currents, resistor $R1$ which is 0 Ω can be removed and an external control voltage can be applied to $V_{\text{BIAS}}$ ($V_b$ pin) on the bias header, see Fig 3.

By applying this separate bias voltage on the $V_{\text{BIAS}}$ pin of the bias header, the $I_{\text{CC}}$ current can be swept without changing $R_{\text{BIAS}}$. With bias voltage window from 4 to 6 V on $V_b$ while keeping the $V_{\text{CC}}$ pin on 5 V, $I_{\text{CC}}$ can be varied from 30-60 mA. In Fig 4 the relation between $I_{\text{CC}}$ and $R_{\text{BIAS}}$ at $V_{\text{CC}} = 5$ V as well as the relation between $I_{\text{CC}}$ and $V_b$ with $R_{\text{BIAS}} = 5k1$ is shown.
3.2 PCB Layout information

A good PCB layout is an essential part of an RF circuit design. The LNA evaluation board of the BGU8052 can serve as a guideline for laying out a board using the BGU8052. The evaluation board uses micro strip coplanar ground structures for controlled impedance lines for the high frequency input and output. \( V_{cc} \) is bypassed by C4 and C6 decoupling capacitors, C4 preferably should be located as close as possible to the device, to avoid AC leakage via the bias lines. For long bias lines it may be necessary to add decoupling capacitors along the line further away from the device. The self-resonance frequency of inductor L1 should be chosen above \( f_0 \) for good choking. In this case the Murata LQW 15 series has been used. Proper grounding of the GND pins is also essential for good RF performance. Either connect the GND pins directly to the ground plane or through vias, or do both, which is recommended. The layout and component placement of the BGU8052 evaluation board is given in Fig 5.
3.2.1 PCB stack and recommended footprint.

The PCB material used to implement the LNA is a 0.2 mm (8 mil) RO4003C low loss printed circuit board which is merged to a 0.51 mm (20 mil) prepreg and a 0.254 mm (10 mil) FR4 layer for mechanical stiffness. See Fig 6a.

The official drawing of the recommended footprint can be found via following link, sot1327-1_fr.pdf. If micro strip coplanar PCB technology is used it is recommended to use at least 4 ground-via holes of 300um this is also used on the EVBs as shown in Fig 6b.
3.3 Bill of materials

Table 1 gives the bill of materials as is used on the EVB for non-switching applications. In paragraph 5 the differences in the BOM related to switched (TDD) applications are given.

<table>
<thead>
<tr>
<th>Designator</th>
<th>Description</th>
<th>Footprint</th>
<th>Value</th>
<th>Supplier Name/type</th>
<th>Comment/function</th>
</tr>
</thead>
<tbody>
<tr>
<td>IC1</td>
<td>BGU8052</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCB</td>
<td>20x35x1mm</td>
<td>0402</td>
<td>100nF</td>
<td>Various</td>
<td>DC block</td>
</tr>
<tr>
<td>C1,C2</td>
<td>Capacitor</td>
<td>0402</td>
<td>10pF</td>
<td>Various</td>
<td>RF decoupling</td>
</tr>
<tr>
<td>C4</td>
<td>Capacitor</td>
<td>0806</td>
<td>4.7uF</td>
<td>Various</td>
<td>Optional</td>
</tr>
<tr>
<td>C5</td>
<td>Capacitor</td>
<td>0806</td>
<td>4.7uF</td>
<td>Various</td>
<td>LF Decoupling</td>
</tr>
<tr>
<td>C6</td>
<td>Capacitor</td>
<td>0402</td>
<td>100pF</td>
<td>Various</td>
<td>Decoupling</td>
</tr>
<tr>
<td>C7</td>
<td>Capacitor</td>
<td>0402</td>
<td>15nH</td>
<td>Murata LQW15</td>
<td>Bias choke/Output match</td>
</tr>
<tr>
<td>L1</td>
<td>Inductor</td>
<td>0402</td>
<td>0Ohm</td>
<td>Various</td>
<td></td>
</tr>
<tr>
<td>R1</td>
<td>Resistor</td>
<td>0402</td>
<td>10Ohm</td>
<td>Various</td>
<td>stability</td>
</tr>
<tr>
<td>R2</td>
<td>Resistor</td>
<td>0402</td>
<td>5k1</td>
<td>Various</td>
<td>Bias setting</td>
</tr>
<tr>
<td>X1,X2</td>
<td>SMA RF connector</td>
<td>0402</td>
<td>Johnson, End launch</td>
<td>RF connections</td>
<td></td>
</tr>
<tr>
<td>X3</td>
<td>DC header</td>
<td>Molex, PCB header, right angle, 1 row 4 way</td>
<td>DC connections</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
4. Typical application board results

4.1 Typical board performance

The values given in Table 2 are typical values of >25 boards measured.

Table 2. Typical board performance using the BOM for non-switched applications, unless otherwise indicated.  
\( F=1900\,\text{MHz}; \, V_{cc}=5V; \, T_{amb}=25^\circ \text{C}; \, \text{input and output 50}\,\Omega; \, R_{bias}=5.1\,\text{k}\Omega. \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typ</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{cc} )</td>
<td>Supply current</td>
<td></td>
<td>48</td>
<td>mA</td>
</tr>
<tr>
<td>( G_{\text{ass}} )</td>
<td>Associated gain</td>
<td></td>
<td>18.4</td>
<td>dB</td>
</tr>
<tr>
<td>( \text{NF} )</td>
<td>Noise figure</td>
<td></td>
<td>0.52</td>
<td>dB</td>
</tr>
<tr>
<td>( P_{L(1\text{dB})} )</td>
<td>Output power at 1dB gain compression</td>
<td></td>
<td>18.3</td>
<td>dBm</td>
</tr>
<tr>
<td>( IP_{3O} )</td>
<td>Output third-order intercept point</td>
<td>2-tone; tone spacing = 1MHz; ( P_{i} = -15\text{dBm} ) per tone</td>
<td>37</td>
<td>dBm</td>
</tr>
<tr>
<td>( R_{L_{in}} )</td>
<td>Input return loss</td>
<td></td>
<td>15</td>
<td>dB</td>
</tr>
<tr>
<td>( R_{L_{out}} )</td>
<td>Output return loss</td>
<td></td>
<td>21.5</td>
<td>dB</td>
</tr>
<tr>
<td>( \text{ISL} )</td>
<td>Isolation</td>
<td></td>
<td>23</td>
<td>dB</td>
</tr>
<tr>
<td>( T_{\text{sp(on)}} )</td>
<td>Power-on settling time</td>
<td>( P_{i} = -20\text{dBm} ); SHDN(pin 6) from High to Low</td>
<td>( \uparrow )</td>
<td>1.5</td>
</tr>
<tr>
<td>( T_{\text{sp(off)}} )</td>
<td>Power-off settling time</td>
<td>( P_{i} = -20\text{dBm} ); SHDN(pin 6) from Low to High</td>
<td>( \uparrow )</td>
<td>0.04</td>
</tr>
</tbody>
</table>

[1] The power on/off settling time has been measured on the boards with the BOM for switched applications, \( C_{1} \) and \( C_{2} \) are 100pF.
4.2 S_Parameter, 1dB compression, IIP3, measurement setup

The BGU8052 EVBs are fully assembled and tested.

**Fig 7** Shows the measurements setup that is used to evaluate the BGU8052 EVB for S_parameters (Gass, RL_in, RL_out, and ISL), 1dB gain compression as well as OIP3. It is intended as a guide only, substitutions are possible.

![S-parameter, P1dB and OIP3 measurement set-up](image)

**Fig 7.** S_parameter, 1dB compression and IP3 measurement setup

**Fig 8** shows the typical wide band S parameter measured on the BGU8052 EVB. The 1dB gain compression curve is shown in **Fig 9**.
$V_{CC} = 5V; \ T_{AMB} = 25\ ^{\circ}C; \ I_{CC} = 48\ mA$

**Fig 8.** S-parameters as function of frequency.

$P_{1dB} = 0.5\ dBm; \ P_{L1dB} = 17.9\ dBm$

**Fig 9.** 1dB gain compression curve.
4.3 Noise figure measurement setup

In Fig 10 the noise figure measurement set-up is shown, this is also intended as a guide only, substitutions can be made. For noise levels of the BGU8052 which <1 dB it is recommended to perform the noise-measurements in a Faraday’s cage or at least put the DUT in a shielded environment. This is recommended to avoid any interference of cellular frequencies that are in the same frequency range.
The noise figure shown in Fig 11 is measured using the setup shown in Fig 10. A spectrum analyzer with noise option. A 5dB ENR noise source was used. To achieve the lowest possible setup noise-figure an external pre amplifier is also recommended.

The Noise figure value in Fig 11 is the value measured at the evaluation board SMA connectors. Correcting for the connector and PCB loss will end up in 0.05dB lower noise figure.

Fig 11. Typical noise figure performance versus frequency.

Vcc = 5V; Tamb = 25 °C; Icc = 48mA

(1) Measured at the evaluation boards SMA connectors.
### 4.4 3rd order intercept point, output referred

The evaluation boards provided in the customer evaluation kit are automatically measured on linearity using the set-up shown in Fig 7. Alternatively the setup given in Fig 13 can be used, which is done for the spectrum plot in Fig 12.

![Typical OIP3 spectrum](image)

**Fig 12. Typical OIP3 spectrum**

1. \( \text{OIP3 LSB} = \frac{(64.21+3.28)}{2}+3.28 = 37.0 \text{ dBm} \)
2. \( \text{OIP3 USB} = \frac{(67.43+3.3)}{2}+3.3 = 37.0 \text{ dBm} \)

\( \text{IIP3} = \text{OIP3} - \text{Gain} = 37 - 18.4 = 18.6 \text{ dBm} \)

The bias choke L1 on the application board is determined empirically in order to get the best OIP3 as well as keeping good output return loss, S22. On the EVB for non-switching applications the values of C1 and C2 are chosen to be 100nF. Capacitors, C1 and C2 do not have any matching functionality, but are only required for DC blocking. In [1] the effect on linearity of SiGe BiCMOS BJTs and the advantage of using low source impedances at the low frequencies of the 2nd order mixing terms is described. These C1 and C2 being 100nF gives better 2nd order mixing suppression. However, for the applications were the LNA is switched with high switching frequencies and power on settling times of several micro seconds is required, the values of C1 has to be decreased to lower than 100pF which effects the IP3.

When measuring the high OIP3 values it is essential check the capabilities of the used measurement equipment. Be aware that the measurement set-up itself is not generating dominating IM3 levels. Advised is to do a back to back measurement without a DUT first.
4.5 Stability Factor

The very high Gain at low frequencies might introduce potential instability issues, K-factor<1. Proper selection of the output bias choke together with the 10 Ohm resistance R1 can improve this. Error! Reference source not found. shows the rollet stability factor plots of the typical K factor with 33nH bias choke and 18nH. Please note this change of bias choke will affect the input and output match of the circuits.
Fig 14. K factor improvement

a. Rollet stability factor with 33nH Choke.

b. Rollet stability factor with 18nH Choke.
5. BGU8052 applied in switched applications

5.1 Description

If the BGU8052 is used in switched applications both the SHDN pin as well as the Vbias pin can be used to apply a switch control voltage. It is preferred to use the SHDN pin.

Both pins require less than 1 mA driving current which means they are CMOS compatible. This enables LNA switching directly via a micro controller.

As stated before, if the BGU8052 is applied in time domain duplexing (TDD) kind of systems with requirements on the power on/off settling time, C1 needs to be decreased to $\leq 100$ pF, in order to achieve a power on settling time of $< 2$ $\mu$s.

There is an alternative way of switching the LNA, by switching the overall supply. In this case the switching time is limited by the time constant created by $C6 \times R_{bias}$. So additional to lowering the value of $C1$ the decoupling capacitor $C6 (4.7 \mu F)$ also has to be decreased to values $<10$ nF. Please note that lowering the low frequency decoupling capacitor makes the circuit more sensitive to $V_{CC}$ modulation of the 2nd order mixing products.

5.2 Measuring Power-on-off settling time

The circuit used to measure the power on/off settling time is shown in Fig 15. This can be used as a guidance to determine the power on/off settling time.

The waveform generator is used to provide the control voltage on either the SHDN pin (6) or the Vbias pin (1).

Set the waveform generator Agilent 33250 to square mode and the output amplitude to required voltage for the used control pin, with 50 ohm output impedance. Set the RF signal generator output level to -25 dBm at 1900GHz and increase its level until the peak detector output level is about 5mV on 1mV/division, the signal generator RF output level is approximately -20 dBm.

A peak detector is needed to detect the high frequency AC signal at the output of the DUT, representing it as a DC voltage equal to the peak level of the applied AC signal.

It is very important to keep the cables as short as possible at input and output of the LNA so the propagation delay difference on cables between the two channels is minimized. It is also critical to set the oscilloscope input impedance to 50ohm on channel 2 so the diode detector can discharge quickly to avoid a false result on the Turn OFF time testing.

In case of switching the supply (Vcc) an additional PNP switching transistor circuit was used to drive the 48 mA Icc. This circuit is controlled by the waveform generator.
Power on/off settling time measurement set-up

Fig 15. Power on/off settling time measurement setup.

Table 3. Typical power on/off settling time
Measured on BGU8052 EVB. C1=C2=100pF

<table>
<thead>
<tr>
<th>Control pin</th>
<th>Power on</th>
<th>Power off</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHDN</td>
<td>1.5</td>
<td>0.04</td>
<td>µs</td>
</tr>
<tr>
<td>VBIAS</td>
<td>1.2</td>
<td>0.45</td>
<td>µs</td>
</tr>
<tr>
<td>VCC [1]</td>
<td>2.1</td>
<td>0.75</td>
<td>µs</td>
</tr>
</tbody>
</table>

[1] C6 ≤ 10nF
Fig 16 to Fig 18 is showing power on/off settling time curves for the different control circuits.

**Fig 16. Power on/off settling time using the SHDN pin(6)**

- **T\text{on}** 1.54 µs
  - Yellow curve SHDN control voltage
  - Blue curve output of the detector diode

- **T\text{off}** 40.8 ns

**Fig 17. Power on/off settling time using the V\text{BIAS} pin(1)**

- **T\text{on}** 1.24 µs
  - Yellow curve V\text{BIAS} control voltage
  - Blue curve output of the detector diode

- **T\text{off}** 452 ns
a. $T_{off} \ 2.12\mu s$

Yellow curve switch-circuit trigger-pulse.
Pink curve switched supply voltage.
Blue curve output of the detector diode

b. $T_{off} \ 760\ ns$

Yellow curve switch-circuit trigger-pulse.
Pink curve switched supply voltage.
Blue curve output of the detector diode

Fig 18. Power on off settling time using the supply voltage.

6. References


7. Customer Evaluation Kit

In the customer evaluation kit you will find;
- 2 EVBs
- 10 loose samples.

On the back side of the boards it is indicated whether the board is meant for a fast switching applications TDD or for non-switching applications FDD. Error! Reference source not found. shows a picture of the customer evaluation kit.
Fig 19. Customer evaluation kit.
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