AN11431

BFU550 ISM 433 MHz LNA design

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Document information

Info	Content
Keywords	BFU520, BFU530, BFU550 series, ISM-band, 433MHz 866MHz
Abstract	This document describes an ISM Frequency LNA design on BFU5xx Starter kit
Ordering info	BFU5xx Starter kit OM7962, 12nc 9340 678 71598
Contact information	For more information, please visit: http://www.nxp.com

Revision history

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1. Abstract

In this application note an ISM band (industrial, scientific and medical) LNA design (low noise amplifier) using a BFU5xx transistor from NXP latest wideband transistor range is described. It shows the design, simulation and implementation phases. Together with measurement results, parameters measured over temperature are shown.
The application note (AN) can be a starting point for new design(s), and/or derivative designs.

2. Introduction

The BFU5xx transistor family is designed to meet the latest requirements on high frequency applications (up to approximately 2 GHz) such as communication, automotive and industrial equipment.
As soon as fast, low noise analogue signal processing is required, combined with medium to high voltage swings the BFU5xx transistors are the perfect choice. Due to the high gain at low supply current those types can also be applied very well in battery powered equipment.
Compared to previous Philips / NXP transistor generations and competitor products' improvements on gain, noise and thermal properties are realized. BFU5xx transistors are available in various packages.

The transistors are promoted with a full promotion package, called "starter kits" (one kit type per package-type). Those kits include two PCB's (one with grounded emitter, one with emitter degeneration provision), RF connectors, transistors and simulation model parameters required to perform simulations. See the overview of available starter kits in the table below.

Table 1. Customer evaluation kits

	Basic type	Customer evaluation kits
1	BFU520W, BFU530W, BFU550W	OM7960, starter kit for transistors in SOT323 package
2	BFU520A, BFU530A, BFU550A	OM7961, starter kit for transistors in SOT23 package
3	BFU520, BFU530, BFU550	OM7962, starter kit for transistors in SOT143 package
4	BFU520X, BFU530X, BFU550X	OM7963, starter kit for transistors in SOT143X package
5	BFU520XR, BFU530XR, BFU550XR	OM7964, starter kit for transistors in SOT143XR package
6	BFU580Q, BFU590Q	OM7965, starter kit for transistors in SOT89 package
7	BFU580G, BFU590G	OM7966, starter kit for transistors in SOT223 package

Basic type	Customer evaluation kits

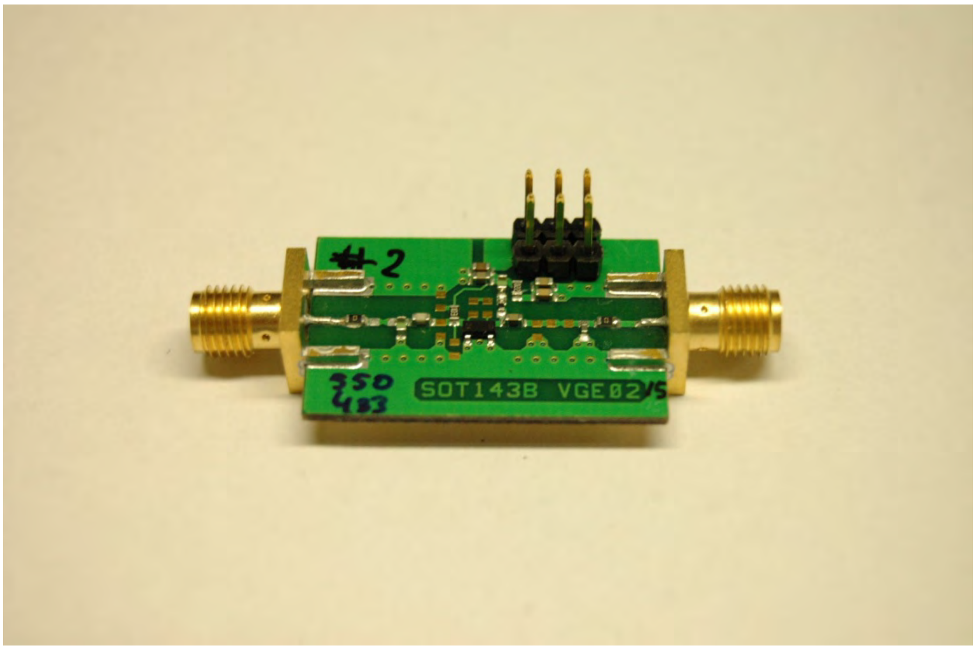


Fig 1. BFU5xx evaluation boards

3. Requirements

The demonstrator circuit is designed to show the BFU550 capabilities for a 433 MHz ISM LNA with strong focus on best possible Noise Figure at low to medium supply current.
The aim of the demonstrator circuit was to design a LNA optimized for the ISM band for battery powered equipment meeting following requirements:

Supply Voltage: 3.6 Volts nominal
Supply current: 20mA at ambient temperature
Noise Figure: < 1.4dB
Gain: approx. 13dB
OIP3: priority on NF but preferably >+20dBm
Input Return-Loss: < -8dB
Output Return-Loss: < -10dB

The design is aimed at low BOM cost and small PCB area, inductors are SMD types (preferable low cost multilayer types) to enable simple tuning to other frequency bands.

4. Design considerations

In order to achieve minimum Noise Figure, with Gain still close to the maximum available gain, the source impedance has to be close to the optimum for Noise Figure and not too far from to the maximum gain impedance. Designing for optimum Noise Figure will compromise, for example, the input return loss, but this is assumed to be acceptable.

At any time the circuit should be stable, hence during the design phase the K-factor needs to be observed carefully.

5. Design approach

The design starts in the simulation phase, applying the Mextram Model (available at http://www.nxp.com). Agilent "Advanced Design System" (ADS) was used for this but other simulation software packages should give equal results. Spice / Gummel Poon models are available.

Once simulation results meet the requirements, the circuit is built on a universal Printed Circuit Board (PCB) and evaluated. If measurement results show significant offset from simulated results, fine tuning is required until required performance is met. To achieve better matching between simulations and measurements, the PCB parasitic properties were added in the simulation template.

Following blocks of passive components can be identified:
1) resistors for DC biasing
2) passives set up collector load
3) passives for output matching
4) passives for input matching
5) passives required to ensure stable operation

Each block will be discussed separately below.

5.1 Simulation steps

Following simulation / design approach can be useful:

1) Configure the DC bias set-up, ensuring the Icc is set around desired value.
2) Configure the collector load circuit and output matching circuitry, optimizing the output Return Loss (RL).
3) Check stability.
4) Configure the input matching, for LNA optimize for minimum noise figure (NF) but keep close to optimum gain, if possible optimum NF gain points should be close.
5) Check stability.

Assumptions:

- Realistic passives are used by applying Murata design kit (0603 / 0402)
- PCB tracks represented by strip-lines

5.2 Implementation / evaluation steps

Following implementation / evaluation steps have been executed:

1) Implement simulated design on universal PCB.
2) Evaluate LNA on Gain / NF / matching / Stability at ambient temperature.
3) Fine tune passives if required.
4) In case significant differences between simulations and measured results are observed, try to modify parasitic properties in the simulation template.
5) Measure LNA design on RF parameters over temperature.

5.3 Setting up the DC bias circuit

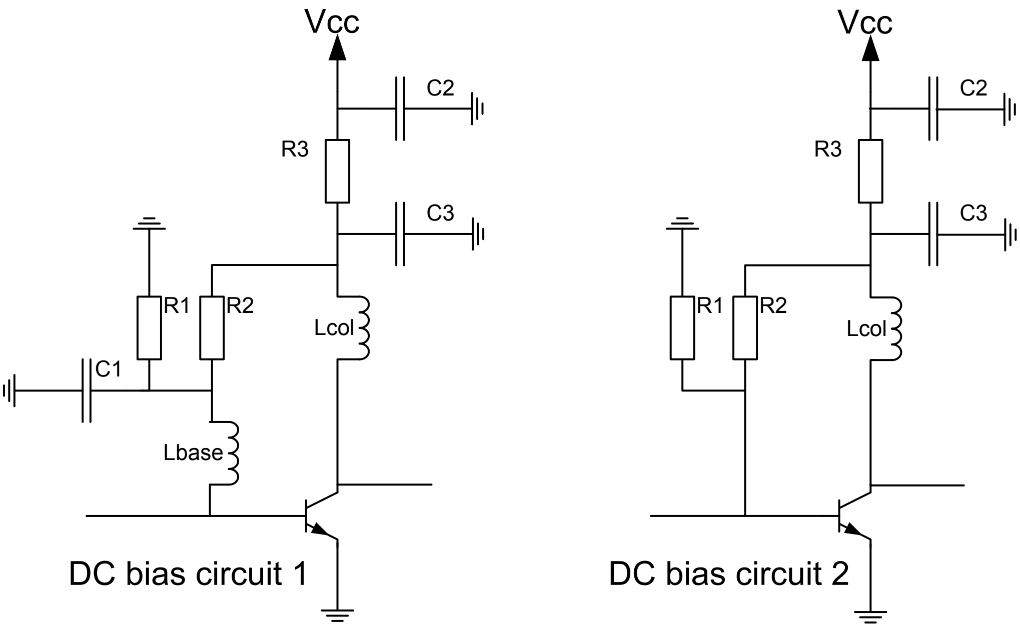


Fig 2. Circuitry to set DC bias current

Circuit 1 has the advantage that resistive noise from the resistors R1 and R2 is suppressed by capacitor C1, but at the cost of an extra inductor. This inductor can be part of the input matching.

Circuit 2 is commonly used and saves two passive components. Both circuits tend to have increasing collector current (Icc) with increasing temperature, partly stabilized by R3. Increasing R3 will have impact on the linearity (OIP3, P1dB).

5.4 Definition of collector load and output match

The configuration used and simulation display is shown below (ADS).

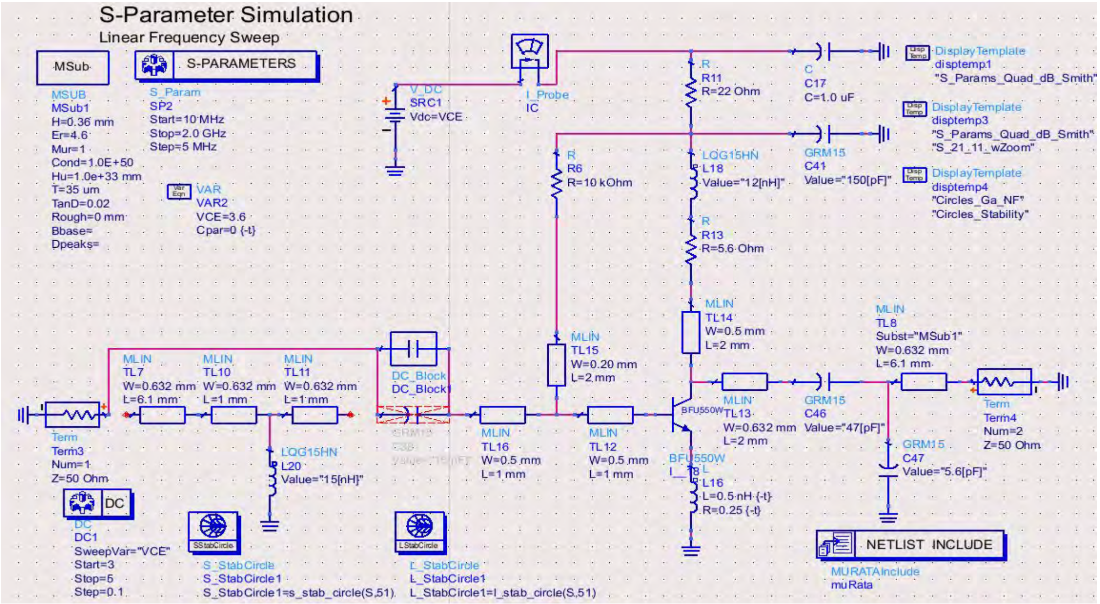
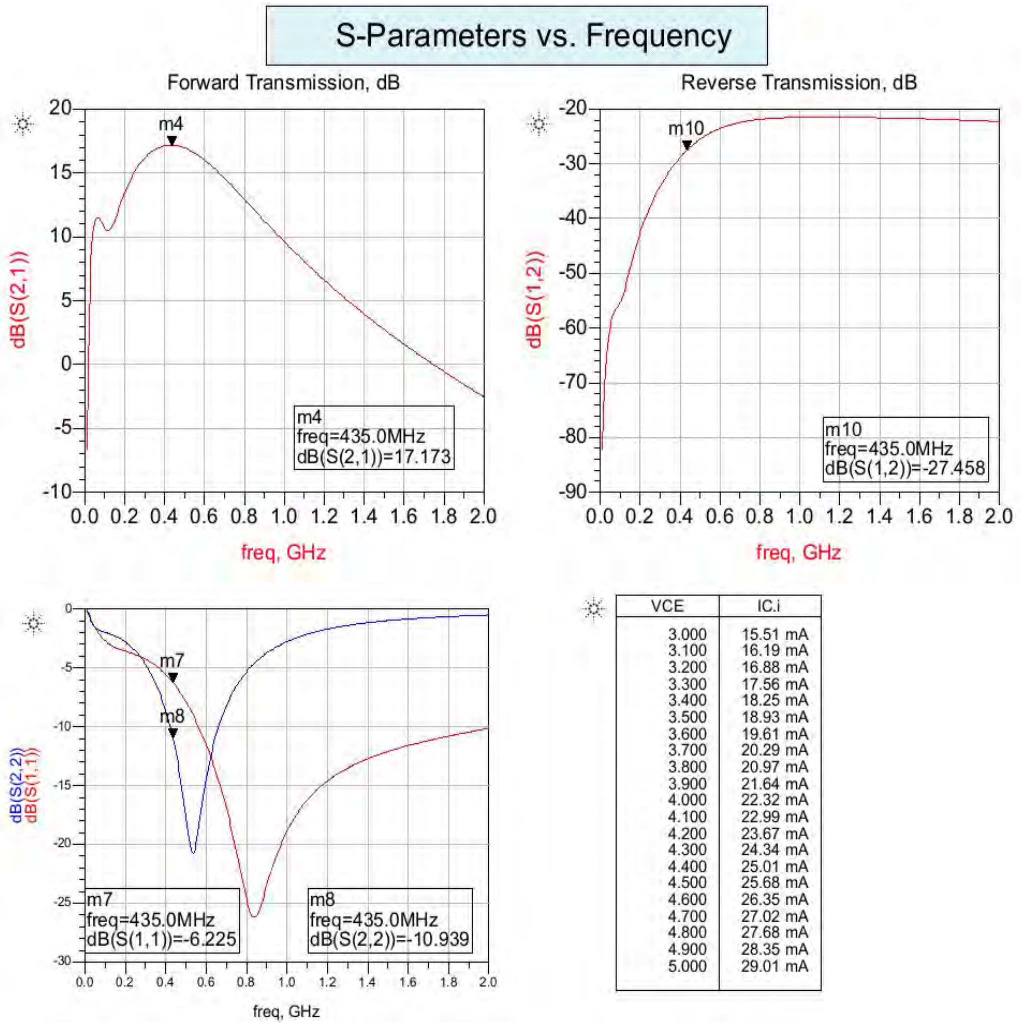


Fig 3. ADS design template for output stage design

In this simulation for the 433 MHz ISM Band the input matching circuit is bypassed. The components L18, C46, C47 are tuned to get a match in the required frequency band.



VCE	IC.i
3.000	15.51 mA
3.100	16.19 mA
3.200	16.88 mA
3.300	17.56 mA
3.400	18.25 mA
3.500	18.93 mA
3.600	19.61 mA
3.700	20.29 mA
3.800	20.97 mA
3.900	21.64 mA
4.000	22.32 mA
4.100	22.99 mA
4.200	23.67 mA
4.300	24.34 mA
4.400	25.01 mA
4.500	25.68 mA
4.600	26.35 mA
4.700	27.02 mA
4.800	27.68 mA
4.900	28.35 mA
5.000	29.01 mA

Fig 4. ADS simulation results for transistor + bias + output match

After defining the configuration for the collector load / output matching network and tuning the component values, a simulation is executed to observe the amplifiers stability. See figure below.

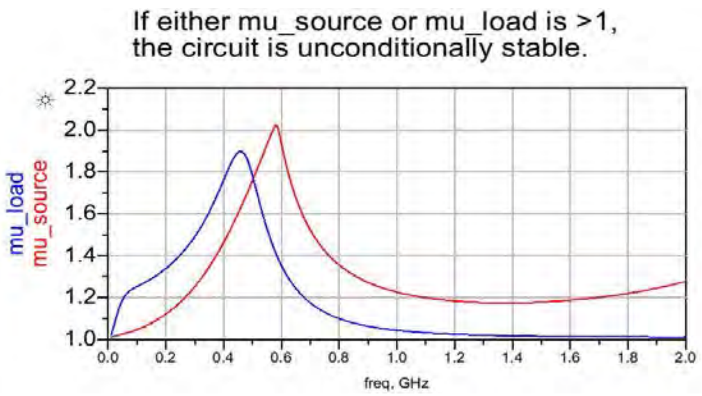


Fig 5. ADS simulation results for stability (μ-factor)

5.5 Definition of input / source matching circuit

In case the amplifier has to be designed to get minimum noise figure, the “noise and gain circles” can be applied.

See figure below: In the noise circles plot you can find the area for optimum source impedance, as should be seen by the base of the transistor, to achieve lowest noise figure.

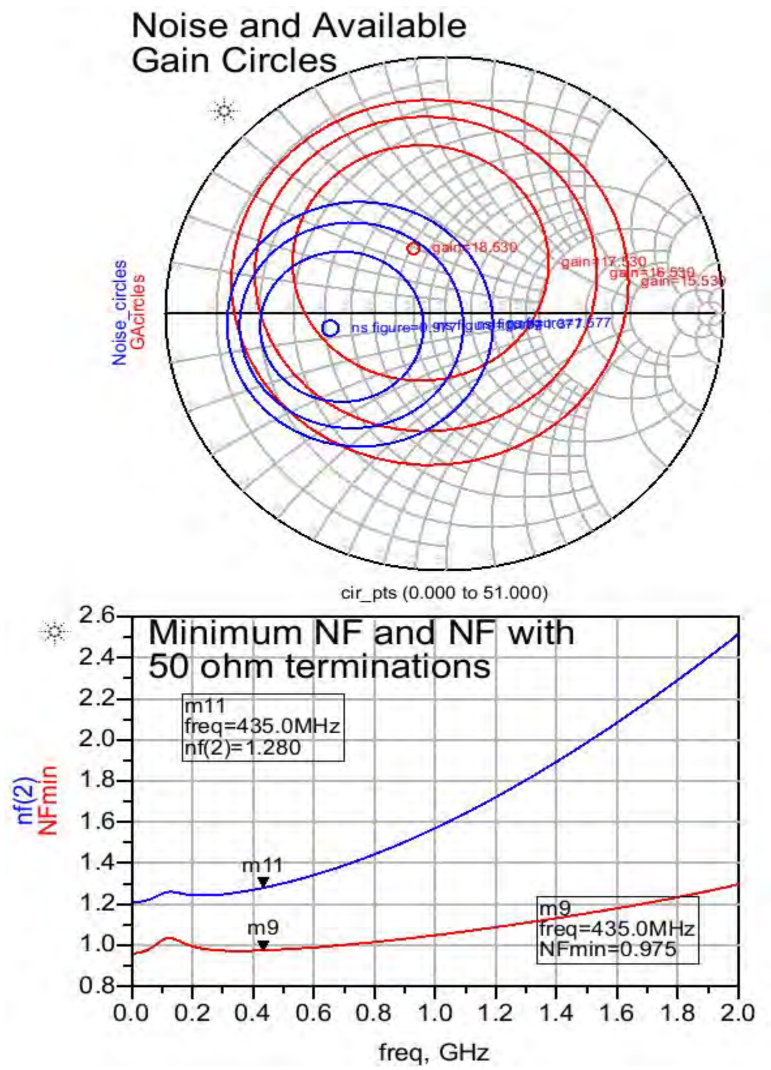


Fig 6. BFU550 Noise and Gain circles at 433 MHz

This is the result from simulations of the set-up as shown in section 5.4, Fig 3.

In this Smith Chart you can find the optimum load impedance for optimum noise in the smallest blue circle, NF 0.76dB (this is the expected NF for the transistor without matching/PCB losses). In case the source impedance is shifted into the region of the second blue circle, the NF will be increased by approximately 0.2dB.
The same applies to the Gain, but in that case the red circles needs to be considered.

The input matching network needs to be set up such that the source impedance as seen by the transistor is close to the optimum for NF, preferably also close to optimum gain circle.

In the next figure the simulation template to optimize for best source impedance is shown. Please note that the active part of the circuit is bypassed. We want to observe the S22 which is the source impedance for the transistor applied.

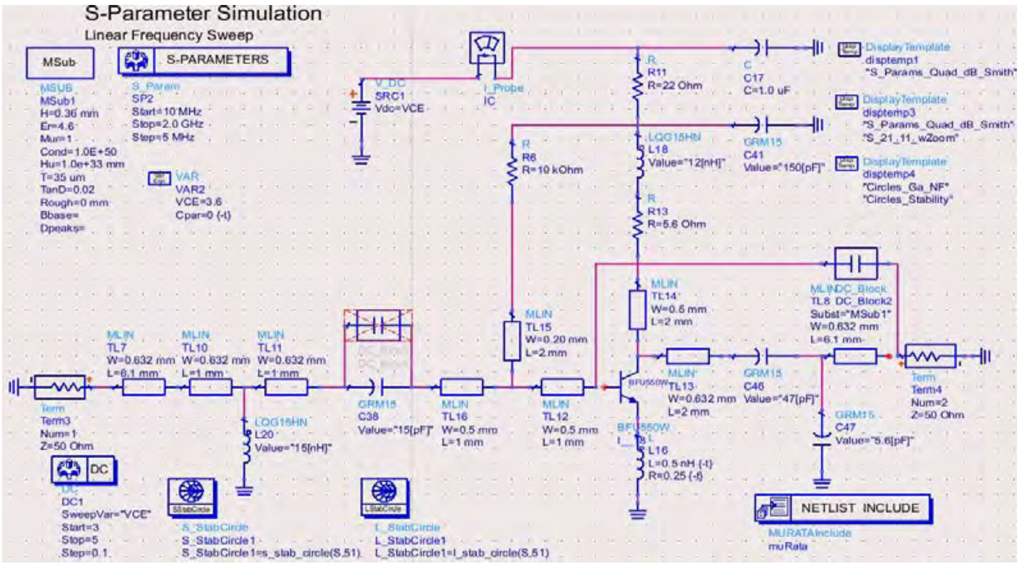


Fig 7. ADS simulation template for input matching

By tuning the components L20, C38 you could move the source impedance towards required area.

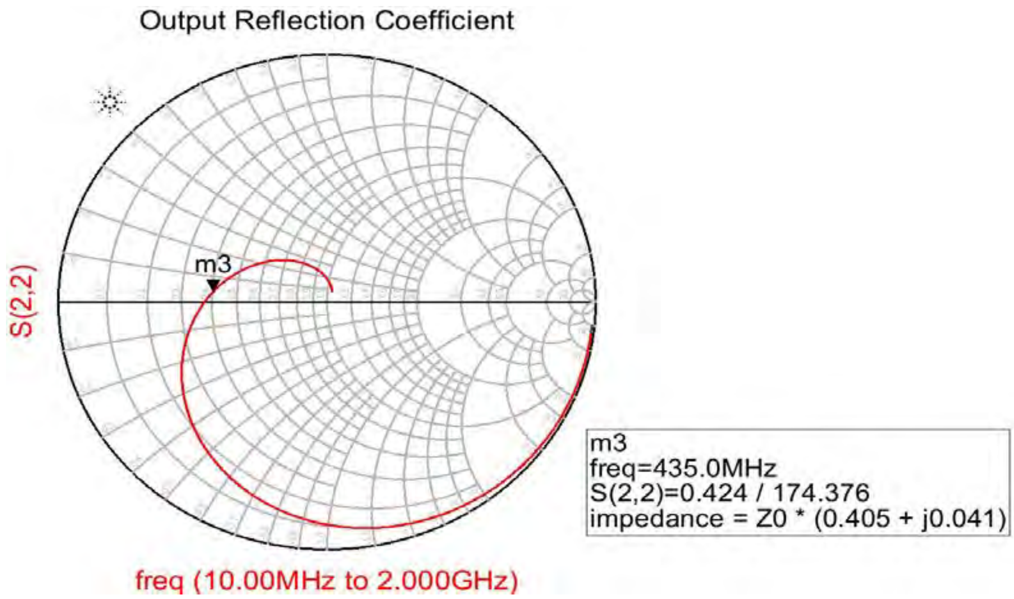


Fig 8. ADS simulation results for source matching

From this figure we see the source impedance at 433 MHz is in the area we want.

5.6 Overall LNA simulation

ADS template used:

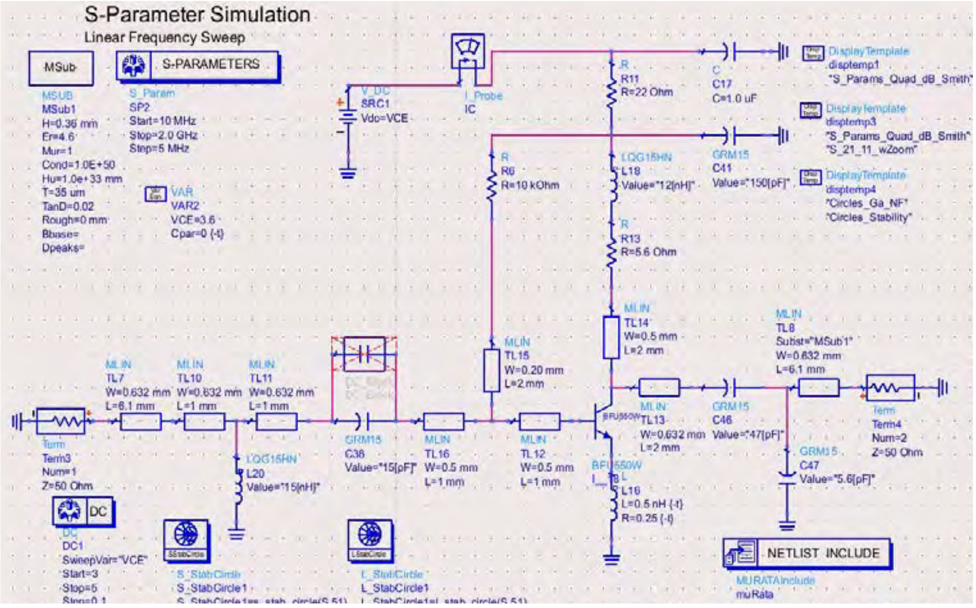


Fig 9. BFU550 433 MHz LNA simulation

Simulation results:

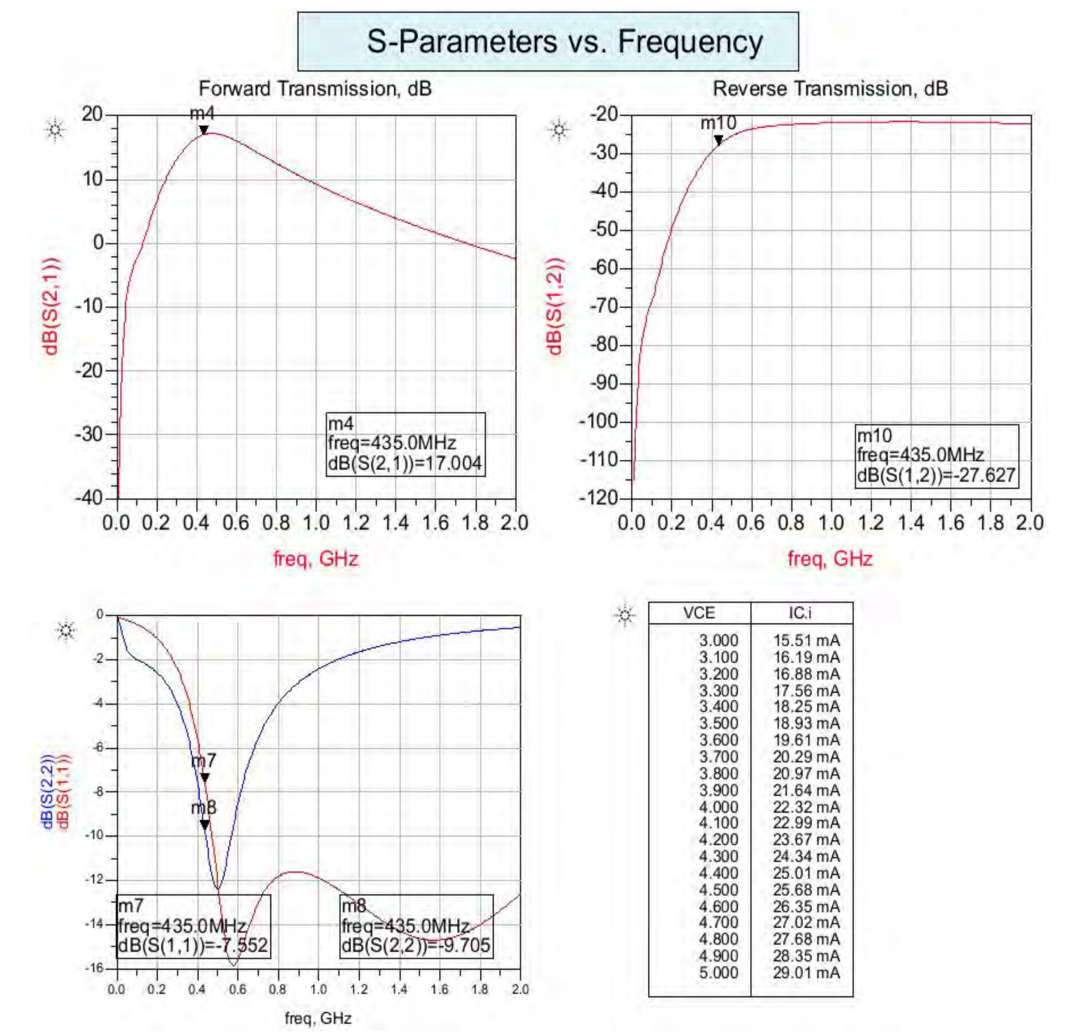


Fig 10. BFU550 433 MHz LNA simulation results, S-parameters/ DC biasing

S-parameters at 3.6 Volt.

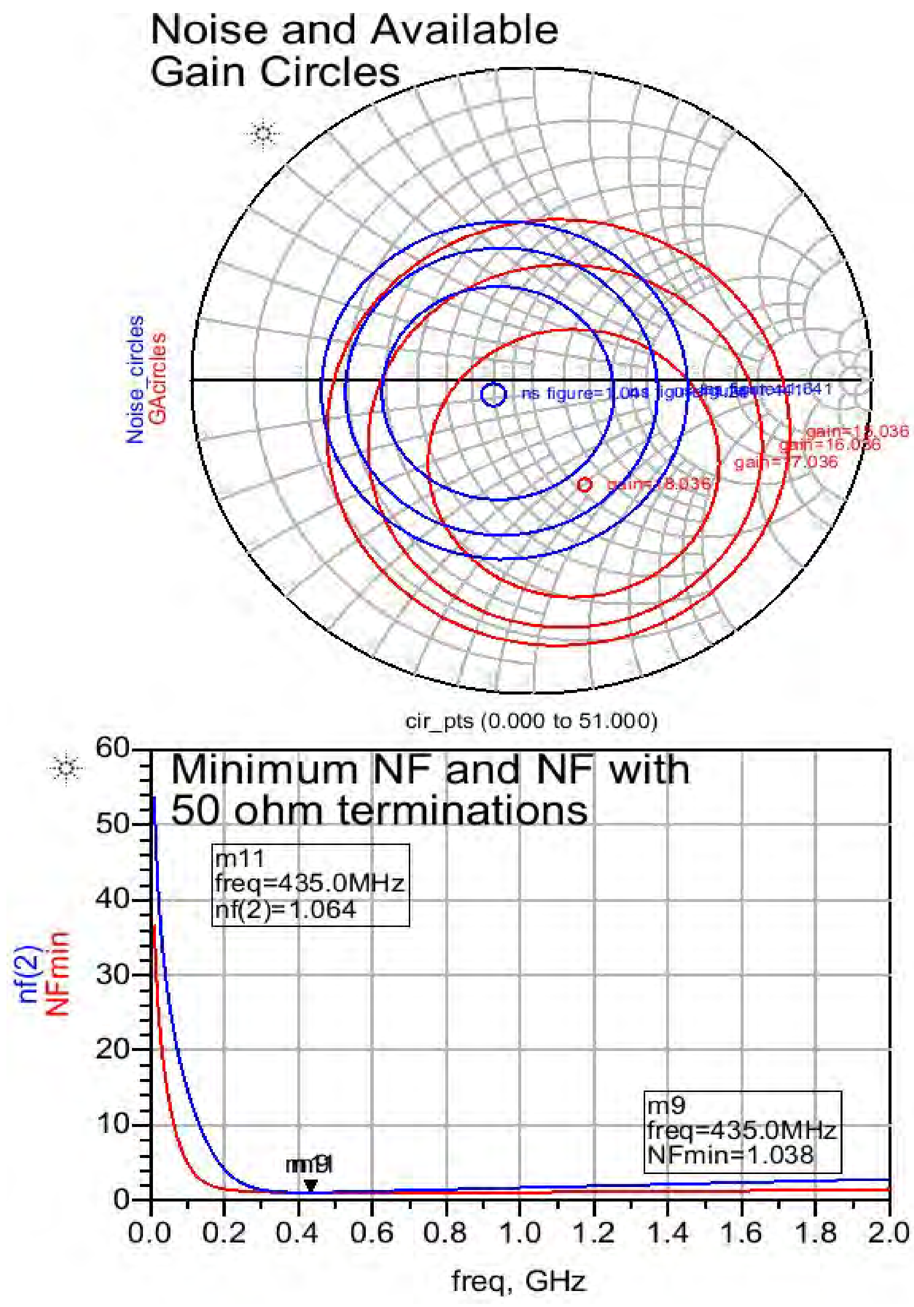


Fig 11. BFU550 433 MHz LNA simulations, Noise / Gain circles

Compared to the noise circles of the unmatched circuit (section 5.5), we can clearly see the optimum noise point has moved towards the ideal 50R point.

6. Application circuit

The circuit diagram of the evaluation board is shown in Fig 12 PCB schematic.

6.1 BFU550 433 MHz ISM LNA schematic

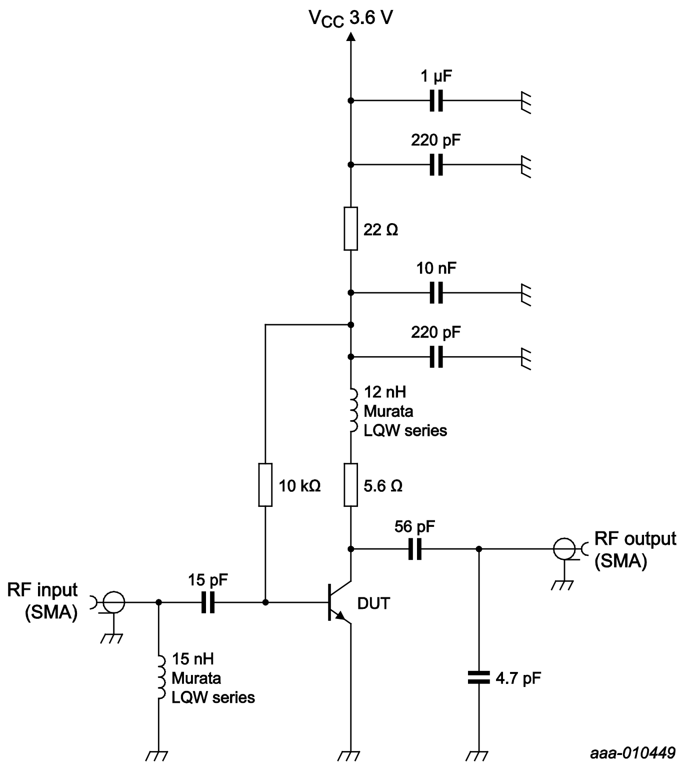


Fig 12. Schematic as implemented for measurements

The PCB layout used for our internal evaluations did not accommodate the 33nH inductor to be in the bias path (as shown in the ADS schematics) the input matching inductor was placed to ground (GND) and an additional DC blocking capacitor (220pF) was used. This should give equal results and a slight improvement on the Noise Figure can be expected as the resistive noise from the two bias resistors is not suppressed by a blocking capacitor to GND.

6.2 BFU550 433 MHz ISM LNA PCB drawing

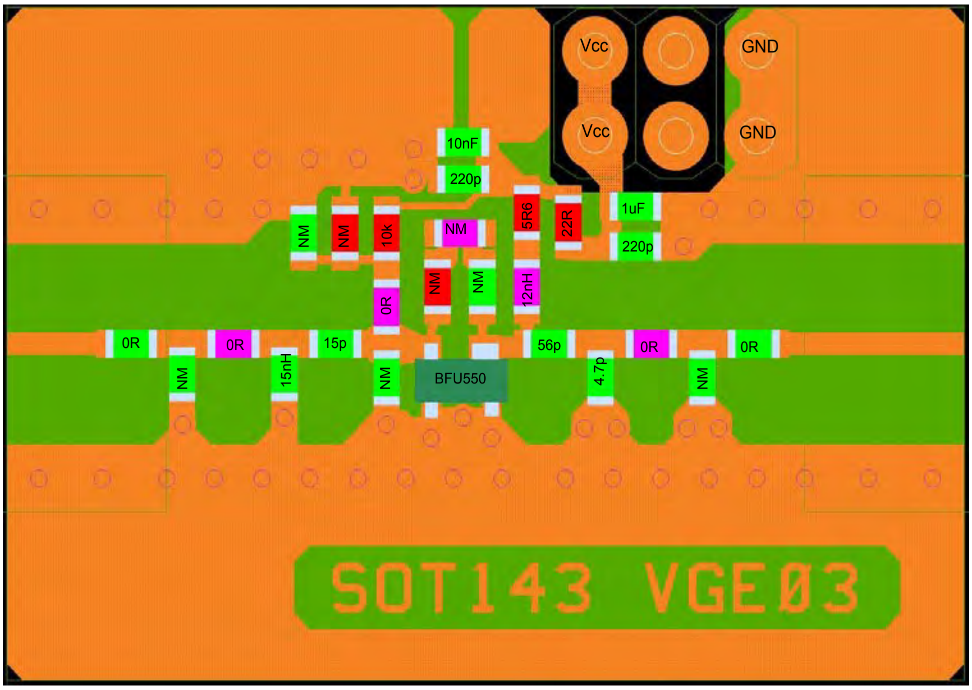


Fig 13. PCB implementation for measurements

Remarks:
0R = SMD jumper
NM = component not mounted.
This layout, as delivered with the Starter kit, accommodates the possibility to implement the biasing as shown in the ADS schematics.

6.3 PCB properties, layer stack

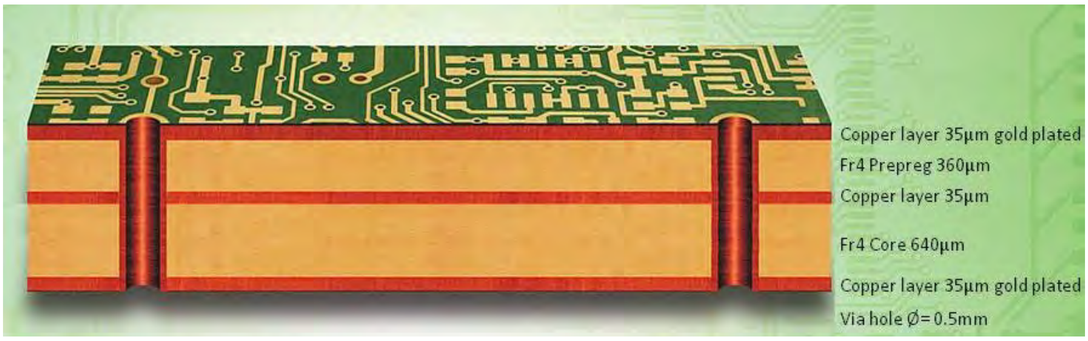


Fig 14. PCB layers used for Evaluation Boards in Starter kit

6.1 Typical LNA evaluation board results

Table 2. Typical results measured on the evaluation boards

Operating Frequency is f = 433 MHz unless otherwise specified; Temp = 25 °C

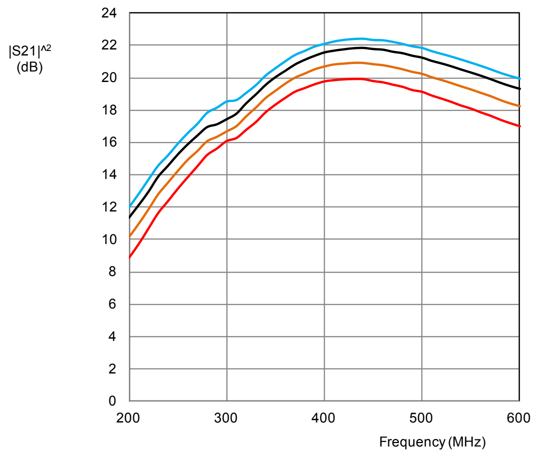
Parameter	Symbol	EVB	Unit	Remarks
Supply Voltage	V_{CC}	3.6	V	
Supply Current	I_{CC}	20	mA	
Noise Figure	NF	1.3	dB	
Power Gain	G_p	21	dB	
Input Return Loss	RL_{in}	-8	dB	
Output Return Loss	RL_{out}	-12	dB	
Output third order intercept point	OIP3	19	dBm	

Table 3. Bill Of Materials

Value	Description	Footprint	Manufacturer
BFU550	Transistor	SOT143	NXP Semiconductors
4.7 pF	Capacitor	0603	Various
15 pF	Capacitor	0603	Various
56 pF	Capacitor	0603	Various
220 pF	Capacitor	0603	Various
220 pF	Capacitor	0603	Various
10 nF	Capacitor	0603	Various
1 uF	Capacitor	0603	Various
5.6 Ω	Resistor	0603	Various
22 Ω	Resistor	0603	Various
10 kΩ	Resistor	0603	Various
12 nH	Inductor	0603	Murata LQW18A
15 nH	Inductor	0603	Murata LQW18A

7. Characterization of LNA over temperature and supply voltage

7.1 Gain (S21) = f (freq)

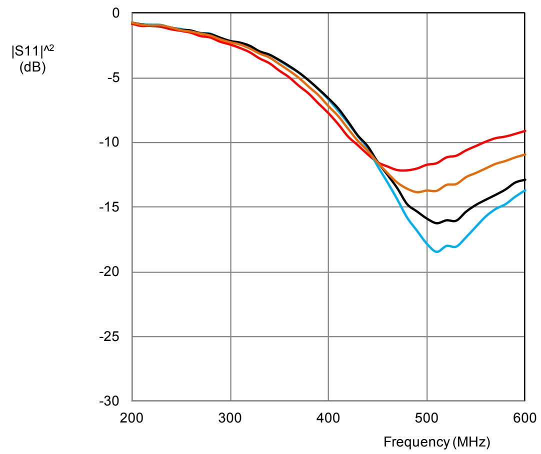


Vsup = 3.6 V;
Tamb = -40 °C
Tamb = 25 °C
Tamb = 85 °C
Tamb = 125 °C

Insertion power gain as a function of frequency; typical values

Fig 15. Measured S21 over frequency for different temperatures

7.2 Input return-loss (S11) = f (freq)



Vsup = 3.6 V;
Tamb = -40 °C
Tamb = 25 °C
Tamb = 85 °C
Tamb = 125 °C

Input return loss as a function of frequency; typical values

Fig 16. Measured S11 over frequency for different temperatures

7.3 Output return-loss (S22) = f (freq)

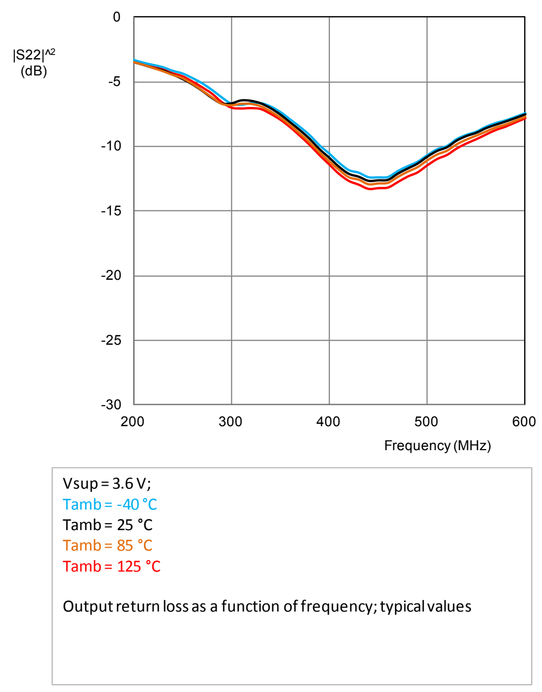


Fig 17. Measured S22 over frequency for different temperatures

7.4 Isolation (S12) = f (freq)

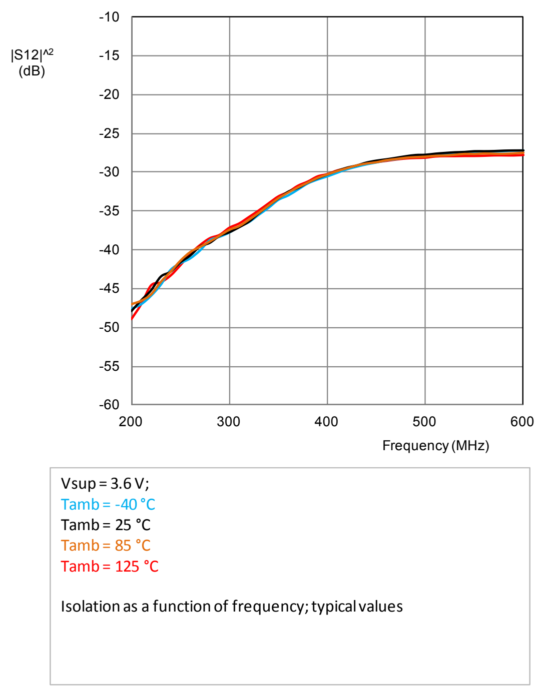


Fig 18. Measured S12 over frequency for different temperatures

7.5 Output third-order intercept point (OIP3) = f (Tamb)

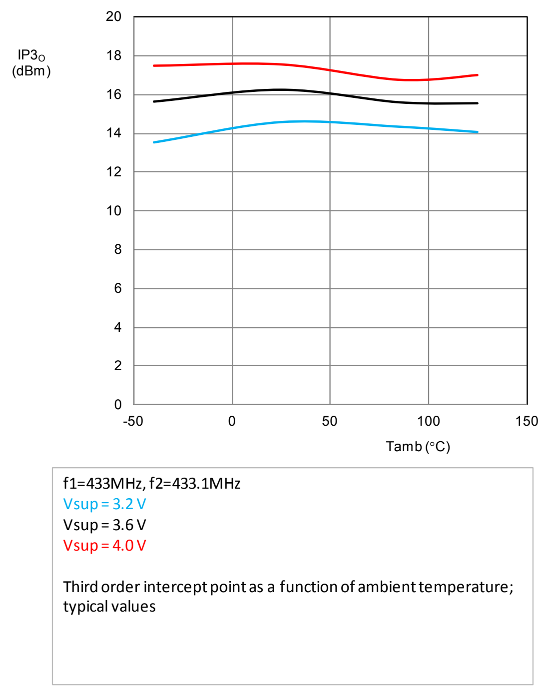


Fig 19. Measured OIP3 over temperature for different supply voltages

7.6 Output Power at 1 dB compression (P1dB) = f (Tamb)

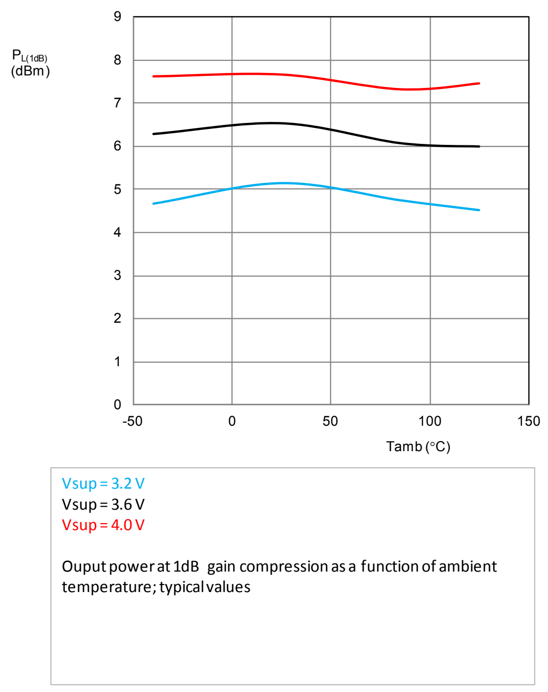


Fig 20. Measured 1dB compression point over temperature for different supply voltages

7.7 Noise Figure = f (Freq)

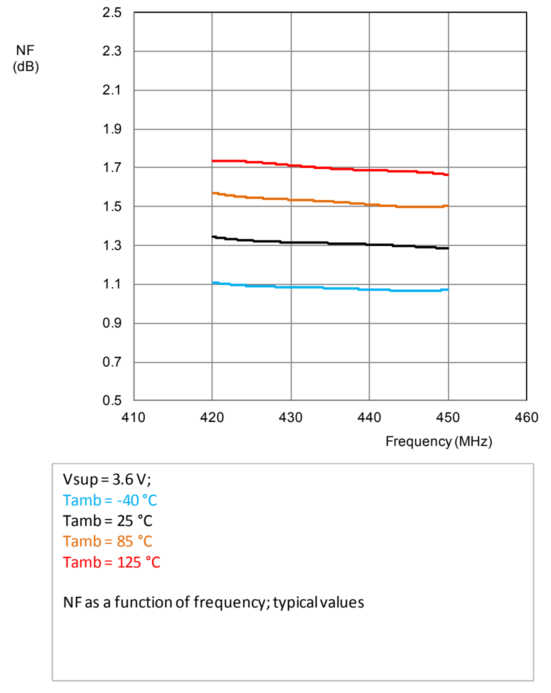


Fig 21. Measured Noise Figure over temperature for different supply voltages

8. Conclusions / recommendations

With BFU550 a ISM 433 MHz LNA design with NF close to 1.4dB can be implemented, for this the input return loss has to be compromised. The circuit can be used as a base for derivative designs, matching to other frequencies can be done by tuning relevant capacitors and inductors.

For improvements on linearity it could be recommended to increase the DC biasing current and increase values for decoupling capacitors to GND, for example on the biasing network in case the matching inductor is in the configuration as shown in the ADS schematics.

	BFU520 series	BFU530 series	BFU550 series
Lowest Noise at low supply current	x		
Low Noise and medium Linearity		x	
Low Noise and high Linearity, high Icc			x

8.1 Tuning the design for other frequencies

This LNA can be tuned to other frequencies as well. The presented configuration has been designed for a low bandwidth application (Center frequency/required bandwidth = approx 10-100 depending on the used components).

The LNA can be tuned to other frequencies following section 5.4 till 5.6. The use of printed inductors or micro-strip elements is recommended above 1GHz to prevent gain drop.

For wideband amplifiers a feedback is recommended which can be implemented on the existing board.

A reference design for a wideband amplifier, applying feedback, is planned to be issued. Please regularly visit the NXP PIP pages to monitor availability of BFU5- series related AN's.

9. References

BFU550 datasheet

BFU5xx starter-kit (OM7962) User Manual, UM10772

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