AN11460

Design migration from TDA8024 to TDA8037T

Rev. 1.0 — 1 October 2014 Application note

Document information

Info	Content
Keywords	TDA8037, TDA8024, migration
Abstract	This application note describes how to migrate a design from TDA8024 to TDA8037: SW updates, HW differences, and an example based on a double layout implementation.

Revision history

Rev	Date	Description
1.0	20141001	First version

Contact information

For additional information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

1. Introduction

The TDA8024 is one of the most used Contact Smart Card readers in the Pay TV market.

It has been used for more than 10 years and has created a standard in contact reader front-end interfaces for Set Top Boxes.

The TDA8037T is a low cost and focused on class B card device.

For the Set Top Boxes that traditionally use the TDA8024, it is now recommended to switch from TDA8024 to TDA8037T in the new designs where class B cards are used.

The goal of this document is to:

- Present the differences between TDA8024 and TDA8037T.
- List all the modifications that should apply to design the TDA8037T instead of TDA8024.

In the whole document the TDA8037T is called TDA8037.

2. Differences TDA8024 – TDA8037

2.1 Summary

Table 1. TDA8024 – TDA8037 differences summary

Item	TDA8024	TDA8037T	Comments
Package	SO28 or TSSOP28	SO28	-
Inactive mode	No Shutdown mode	Automatic SD mode	New feature of TDA8037 for lower current consumption in inactive mode
Crystal clock input	Crystal never stopped	No crystal input, clock signal input instead	Be sure that the clock frequency is adapted, only one CLKDIV pin on TDA8037
DC/DC converter	Doubler mode	No DC/DC convertor	Supply must be 3,3V
Power supply strategy	2 power supply sources generally required	1 power supply source is used	-
Presence pins	2 presence pins PRES (active high) and PRESN (active low)	1 presence pin PRESN (active low)	-
Chip select pin (CS)	No chip select pin	1 Chip select pin	Several TDA8037 can be cascaded.
Card class support	Classes A and B (5V and 3V)	Class B only (3V)	-
CLKDIV	4 divisions available	2 divisions available	On TDA8037 : f/1 and f/2

2.2 Shutdown mode

From a functional point of view, the TDA8024 inactive mode corresponds to the Shutdown mode of the TDA8037: it is reached when CMDVCCn goes HIGH. There is no specific management here from the host.

The only difference is the current consumption which is lower in this mode for the TDA8037: 400µA max for TDA8037, and 1.3 mA max for TDA8024.

2.3 Clock input

With TDA8024, the clock input can be a crystal or an external clock. With TDA8037, only an external clock can be used.

2.4 DC/DC

TDA8024 embed a DC/DC converter based on capacitor, but not the TDA8037. The TDA8037 directly uses the power supply input to generate the card voltage.

2.5 Power Supply strategy

The TDA8037 can be supplied with a single source, if the CPU digital interface power supply level is 3.3V. In this case, 3.3V can be used to supply the TDA8037's host interface and the IC core.

This was generally not the case with TDA8024, which requires a 4V for the DC/DC converter.

2.6 PORADJ

PORADJ can be used in the same way in both chips when it is used, but the connection is different when PORADJ is not used:

For TDA8024, PORADJ must be connected to GND

For TDA8037, PORADJ must be connected to VDD

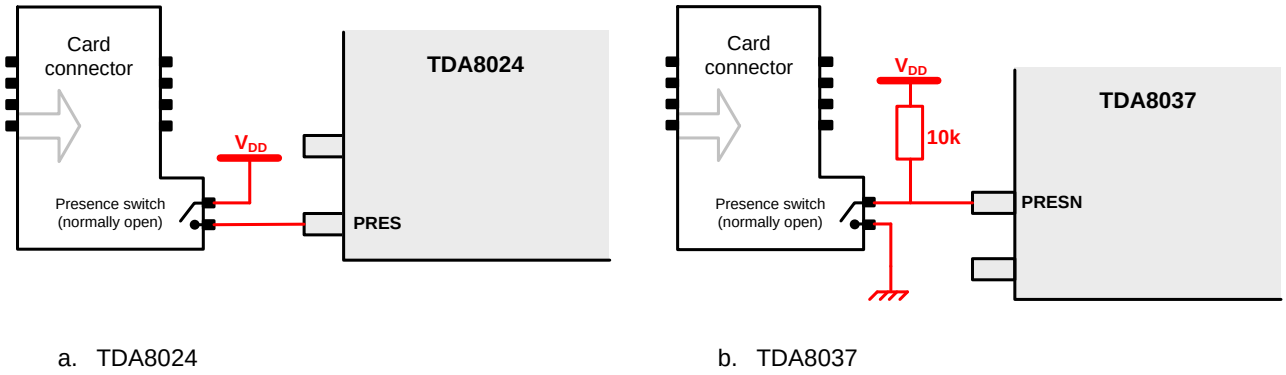
2.7 PRES

TDA8024 has two presence inputs: PRES and PRESN, which are respectively active high and active low. Only one pin can be used at a time.

TDA8037 only offers one presence pin, PRESN, which is active low.

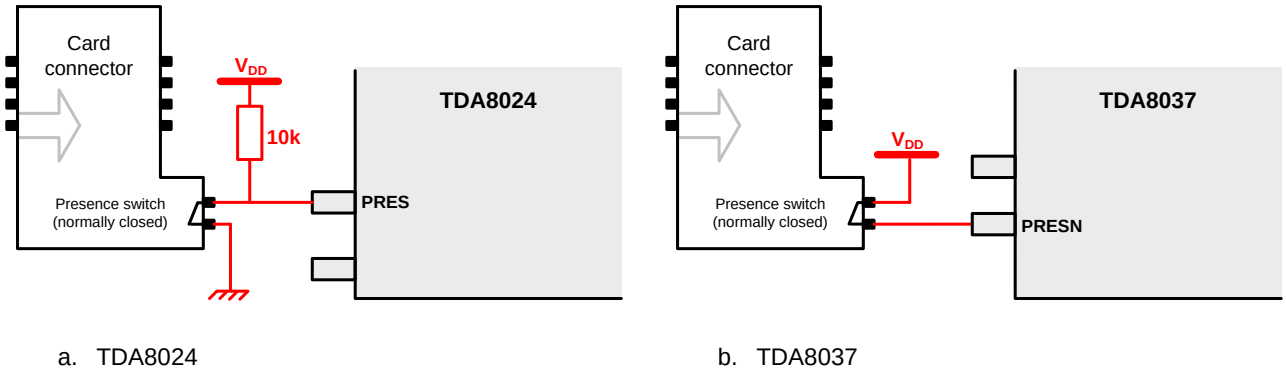
In the TDA8024 designs where PRESN is used, then no change is to apply.

In the TDA8024 designs using PRES pin, then the presence pin connection must be switched as described in the following figure, depending on the smart card connector type (normally open or normally close)



a. TDA8024 b. TDA8037

Fig 1. Presence pin change – Card connector Normally open



a. TDA8024 b. TDA8037

Fig 2. Presence pin change – Card connector Normally closed

2.8 CS

TDA8037 has a Chip Select pin, allowing cascading as many devices in parallel as wanted.

In the case only one TDA8037 is needed, this pin must stay connected to VDD. This is the case for a design where TDA8037 replaces TDA8024

3. New Design Summary

In case of new design switching from TDA8024 to TDA8037, the following items must be checked and updated if required:

Table 2. TDA8024 to TDA8037 migration checklist

Item	HW/SW	Description	Comment
Activation timing	SW	Update the activation timings management (CMDVCCn / RSTIN)	Only if the RST assertion must respect a timing constraint
Single power supply source	HW	Use only one power supply for all TDA8037 blocks.	Optional
PORADJ	HW	Connect PORADJ to VDDI instead of GND	Only if PORADJ functionality is not used
PRES pin	HW	Change the presence detection management	Mandatory if PRES is used on TDA8024 No change if PRESN is used
CS	HW	Connect CS of the TDA8037	Mandatory

4. Legal information

4.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

4.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

4.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

5. List of figures

6. List of tables

7. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 1 October 2014
Document identifier: AN11460