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PN7120 Hardware Design Guide

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Application note
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Document information

Info	Content
Keywords	PN7120, Hardware Design, Power modes, Chip interfaces
Abstract	This document is intended to provide an overview on how to integrate the NFC Controller PN7120 from hardware perspective. It presents the different hardware design options offered by the IC and provides guidelines on how to select the most appropriate ones for a given implementation. In particular, this document highlights the different chip power states and how to operate them in order to minimize the average NFC-related power consumption.

Revision history

Rev	Date	Description
1.1	20151008	• New Quartz reference added • Useless components from reference schematic removed • Recommendation for matching capacitors duplication added • Section 14.3 Licenses updated
1.0	20150315	Approved version for product release
0.1	20141223	Initial version of the document

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1. Introduction

The PN7120 is a full feature NFC Controller designed for integration in devices compliant with NFC Forum standards.

It is designed based on learning from previous NXP NFC device generation to ease the integration of the NFC technology in mobile devices by providing:

A low PCB footprint and a reduced external Bill of Material by enabling as unique feature the capability to achieve RF standards with small form factor antenna

An optimized architecture for low power consumption in different modes (standby, low power polling loop)

An highly efficient integrated power management unit allowing direct supply from a battery while a constant output power (operating distance in Poll mode) for extended battery supply range (2.75 to 5.5V) can be achieved.

It embeds a new generation RF contactless front-end supporting various transmission modes according to NFCIP-1 and NFCIP-2, ISO/IEC 14443, ISO/IEC 15693, MIFARE and FeliCa specifications. This new contactless front-end design brings a major performance step-up with a higher sensitivity.

Detailed chip features set can be found in the *PN7120 Product Datasheet [1].*

This application note is intended to give an overview of the way the PN7120 must be integrated into a hardware platform. It presents in particular the different hardware design options offered by the PN7120 and it provides guidelines on how to select the most appropriate ones for a given implementation.

An overview of the different chip interfaces is first shown. Then detailed information related to each interface is depicted and the related configurations are presented.

2. Interfaces

The purpose of this chapter is to give an overview of the PN7120 interfaces and to show how the chip is interconnected to the external world.

PN7120 external connections are shown in *Fig 1*.

Then, PN7120 interfaces are listed in *Table 1* and the different configuration options are mentioned.

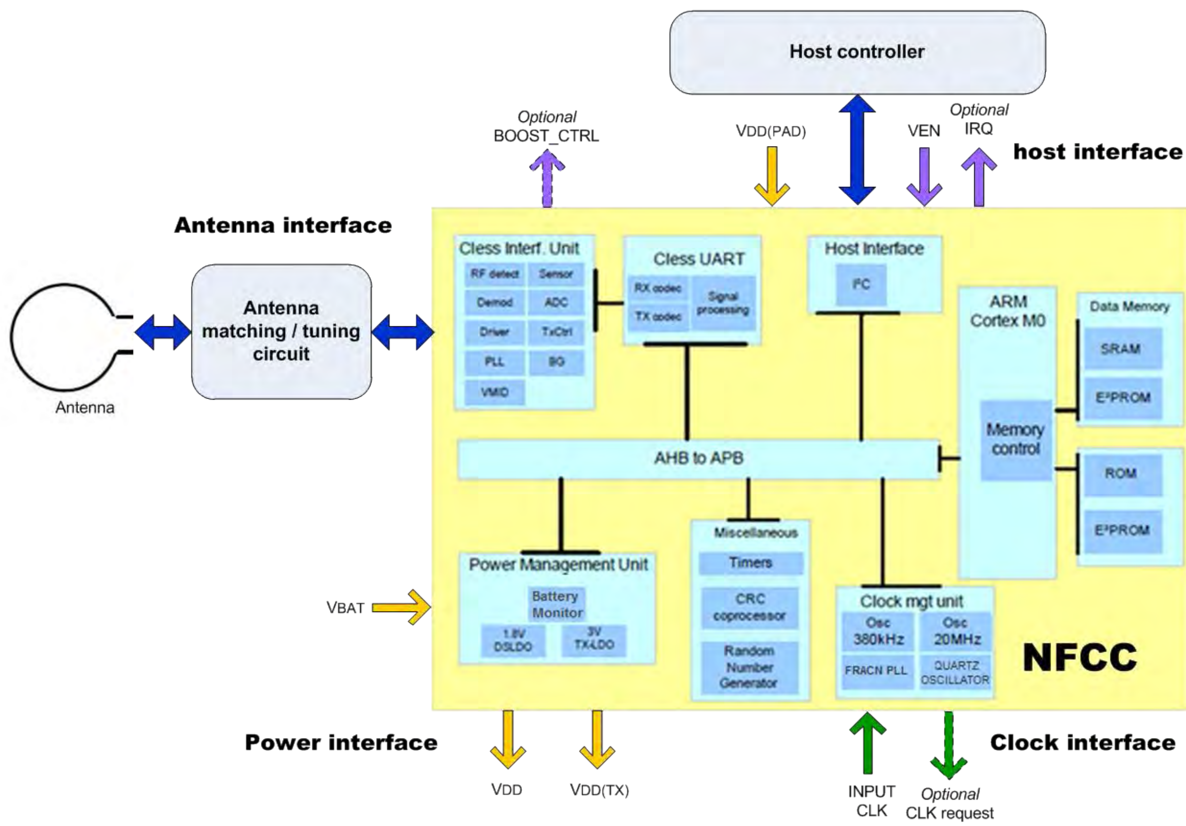


Fig 1. Interfaces summary

The PN7120 provides the following interfaces:

- Host interface
- Clock interface
- Power interface
- Antenna interface

Table 1. Interface summary

Interface	Short description	Options
Host interface	Link with host controller	• I^2C address configuration • IRQ or polling • Reset control
Clock interface	Input clock required when generating RF field	• Input clock characteristics • CLK request mechanism
Power interface	Interface to power management unit (direct battery supply supported)	• Power management concept • Decoupling capacitors
Antenna interface	Link to an NFC antenna in order to enable communication with a remote contactless device	• Antenna selection • Antenna matching

3. Typical application schematics

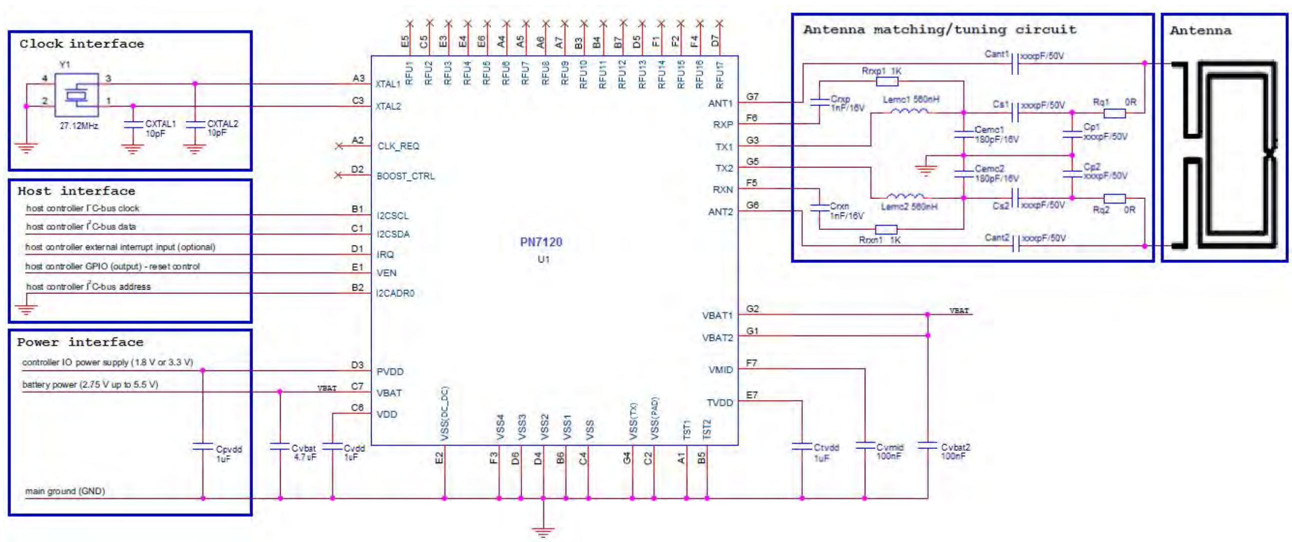
The purpose of this chapter is to propose an application schematic for PN7120.

The below depicted configuration is based on the following implementation choices:

a. The use of a crystal as input clock source

b. The use of a standard antenna

c. No use of external booster



Note: Duplication of Cs and Cp capacitors is recommended in order to allow fine tuning (see 7.2)

Fig 2. Typical Application Schematic

4. Host interface

4.1 Host interface pinning

Table 2. Host interface pinning

Pin	Symbol	Description
B1	I2CSCL	I2C-bus serial clock input
B2	I2CADR0	I2C-bus address bit 0 input
C1	I2CSDA	I2C-bus serial data
D1	IRQ	Interrupt request output
E1	VEN	Reset pin. Set the device in Hard Power Down

4.2 Host interface pin characteristics

Detailed characteristics of the host interface pins can be found in the *PN7120 Product datasheet [1].*

4.3 Digital interface levels

The host controller interface power supply must be connected to the PN7120 on the PVDD pin. Both 1.8V and 3V supply levels are supported.

Thus multiple digital levels between the host controller and the PN7120 can be supported without the need for level shifters.

For details on the PVDD range, please refer to the *PN7120 Product Datasheet [1]*

4.4 I²C bus specificities

Slave address:

In the case where I²C is the selected host interface, the chip will answer to a given I²C slave address.

This is determined by the combination of a base address and the logical state of I2CADR0 pin: b' 0 1 0 1 0 0 I2C_ADR0' where I2CADR0 is the least significant bit. For instance, if I2CADR0 is tied to ground, the 7-bits slave address of the PN7120 is “0x28”.

Table 3. I²C slave 8-bits address

I2C_ADR0 Level	I²C write address (R/W bit = 0)	I²C read address (R/W bit = 1)
0 (GND)	0x50	0x51
1 (PVDD)	0x52	0x53

Pull-up selection:

Pull-up resistors to PVDD are required on the I²C lines SDA and SCL. The resistors value must be selected in order to meet the I²C timing requirements based on the line capacitance, the PVDD level and the targeted maximum I²C clock speed. More details can be found in the *I²C bus specification [3]* document.

4.5 Frames reading synchronization

PN7120 answers / notifications toward the host controller are asynchronous and they can be triggered by an external event (e.g. detection of a card in the RF field).

Therefore, a mechanism must be put in place so that asynchronous frames from the PN7120 are well captured by the host controller. For this, 3 implementations can be foreseen on the host controller side:

- 1- IRQ pin external interrupt
- 2- IRQ pin polling
- 3- Read polling

For 1-, connect pin IRQ of the PN7120 to an external interrupt line on the host controller side. In this case, when the PN7120 has some data available, the IRQ line will be asserted and if configured accordingly, a software interrupt is generated on the host controller side. An I2C read is then managed by the corresponding interrupt handler.

For 2-, the principle is to regularly poll the status of the IRQ pin and when it toggles, to perform a read on the I2C interface.

For 3-, the principle is to regularly perform some read on the I2C interface and to discard frames starting with the default value as in this case it would mean that no data is available from the PN7120. The I²C address will not be acknowledged in case the PN7120 doesn't have any meaningful data to send to the host.

Implementation -1 is recommended.

IRQ Signal Specification:

- The signal can be configured active high or active low via the NCI Configuration API. This configuration is stored in non-volatile memory. Details can be found in the *PN7120 User Manual [2]*.
- The signal will be active any time data is available in the PN7120 send buffer
- The pad state is maintained during the standby mode
- The pad is configured in pull down in hard power down mode

4.6 Reset control (VEN)

The PN7120 HW is activated using the input pin VEN.

When VEN is greater than 1.1V the PN7120 core is supplied from VBAT.

For VEN lower than 0.4V the PN7120 is in hard power down state and the chip's internal core is no more supplied.

The chip is reset when VEN is switched back to a voltage level higher than 1.1V.

It is strongly recommended to foresee a control of VEN pin from the host controller side so that it can reset PN7120 whenever needed.

The VEN pad state is considered as valid information only when the PVDD pad is supplied.

Indeed, VEN signal is supposed to be driven by the host controller with which PVDD supply is shared. When the supply is not there, this means that the host controller is not able to drive a meaningful state on the PN7120 VEN pin.

An internal pull-down resistor can be programmed on the PN7120 internal VEN signal in order to define a clear pin state when it is not externally driven by the host (details can be found in *PN7120 User Manual [2])*. It means that when the device is powered-up with VBAT and PVDD supplied to the PN7120, the NFC chip will stand in hard power down until the host controller explicitly drives the VEN pin to the digital high state (during its boot sequence).

The full PN7120 power states, considering VBAT, PVDD and VEN pin level, is given in *PN7120 Product datasheet [1].*

5. Clock interface

The core microcontroller of the PN7120 chip can run without any external clock (based on an internal oscillator).

However, the 13.56MHz RF field carrier accuracy requirements are not compatible with the use of an internal oscillator. As a consequence, the PN7120 needs either to have an external clock supplied to its XTAL1 pin or to be connected to a crystal oscillator before starting to emit an RF field.

The PN7120 clock interface must be configured properly to reflect whether it is connected to a crystal oscillator or to an external clock (in this case, the frequency must also be configured). This is done through the NCI host interface. Details can be found in *PN7120 User Manual [2].*

5.1 Use of crystal oscillator

A 27.12MHz crystal can be used as input clock for PN7120. For instance, when there is no clock on the system complying with the PN7120 input clock specification. When using a crystal, frequency accuracy and drive level must be carefully selected according to the specification provided in the *PN7120 Product Datasheet [1].*

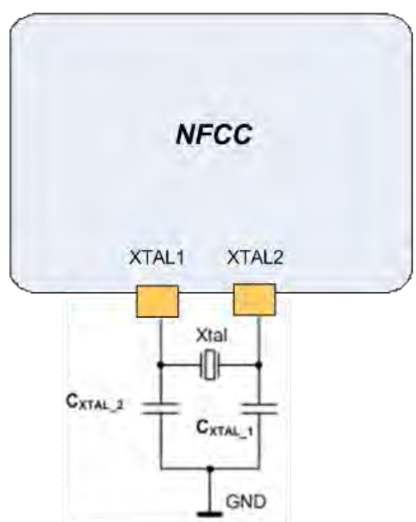


Fig 3. Crystal based clock configuration

Crystal interface has been verified with several references as given below. Other crystal units might be suitable for the specified usage, but only the ones below have been properly checked by NXP.

- NDK:
  - NX2016AA 27.12MHz EXS00A-03778 (discontinued)
  - NX2016SA 27.12MHz EXS00A-CS06346
  - NX2016HA 27.12MHz EXS00A-CH00075
- MURATA
  - XRCGB27M120F3M10R0

5.2 Use of system clock

5.2.1 Input clock characteristics

When an external system clock is used, the input clock frequency must be one of the following values: 13MHz, 19.2MHz, 24MHz, 26MHz, 38.4MHz or 52MHz

Please note that the voltage level of the system clock signal provided to PN7120 must be 1.8V.

The system clock used with the PN7120 chip must fulfill the phase noise requirement described in the datasheet.

The PN7120 input impedance on the XTAL1 pin depends on the input clock frequency:

At 13MHz, it is between 25Kohms and 86Kohms in active mode and between 49Kohms and 53Kohms in standby or Hard Power Down mode.

At 52MHz, it is between 5Kohms and 7.5Kohms in active mode and between 12Kohms and 14Kohms in standby or Hard Power Down mode.

Based on this input clock signal, the PN7120 internal PLL generates the required 27.12MHz internal clock for field generation.

Detailed system clock characteristics can be found in the *PN7120 Product Datasheet [1]*

5.2.2 Clock request mechanism

In order to optimize the device power consumption, the input clock could be provided by the system only when it is actually needed by the chip (i.e. when the NFCC needs to generate an RF field). For this, a clock request mechanism has been put in place.

When the PN7120 needs an input clock, it toggles the CLK_REQ pin to the digital high level and keeps it high as long as the input clock is required.

It requires a specific connection of the CLK_REQ pin which would switch-on the system clock signal whenever the pin is at the digital high level and switch it off when the pin is set back to the digital low level.

This feature is enabled according to PN7120 EEPROM configuration (see details in the *PN7120 User Manual [2]*).

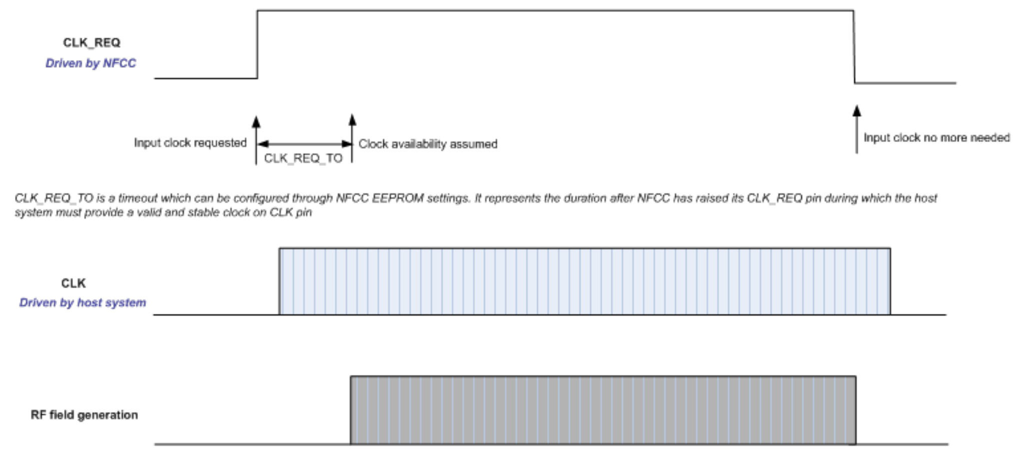


Fig 4. Clock request through CLK_REQ pin

Warning: XTAL1 pin is referenced to PVDD supply. Therefore PVDD must always be supplied to the PN7120 when a valid input clock signal is required (i.e. to generate an RF field)

The dedicated clock request pin (CLK_REQ) can be optionally connected to a clock buffer. CLK_REQ pin is driven high when the NFCC needs an input clock. Otherwise it is driven low.

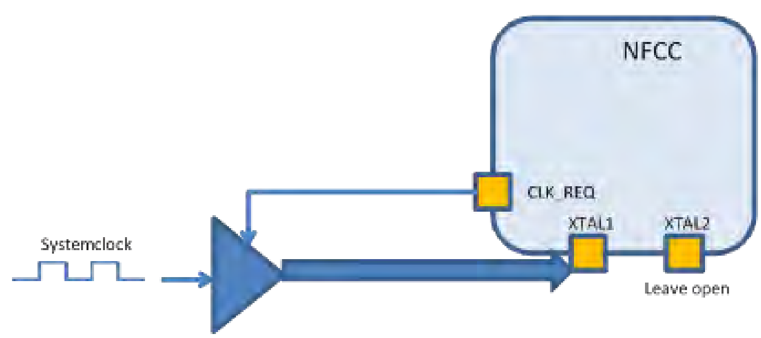


Fig 5. External system clock configuration

6. Power interface

6.1 Power Management Unit

The PN7120 supports to be directly connected to a battery power supply.

It is able to operate with a wide voltage input range from 5.5V down to 2.75V.

Detailed current consumption versus the different power mode and min/typical/max voltage information can be found in the *PN7120 Product Datasheet [1]*.

6.2 External capacitors requirement

The recommended external capacitors (value and voltage it must at least withstand) are listed below:

Table 4. Decoupling capacitors need

	Values	Comments
C_{VDD}	1µF/2V	
C_{PVDD}	1µF/2V or 3.3V	Depending on host power supply decoupling needs
C_{TVDD}	1µF/3.6V	
C_{VBAT}	4.7µF/5.5V	
C_{VDHF}	470nF/3.6V	Optional
C_{VBAT2}	100nF/5V	
C_{VMID}	100nF/1.8V	

A tolerance of 10% or better is recommended for those capacitors. Component de-rating over voltage and temperature must be carefully considered during the decoupling capacitors selection process.

6.3 Power application schematic

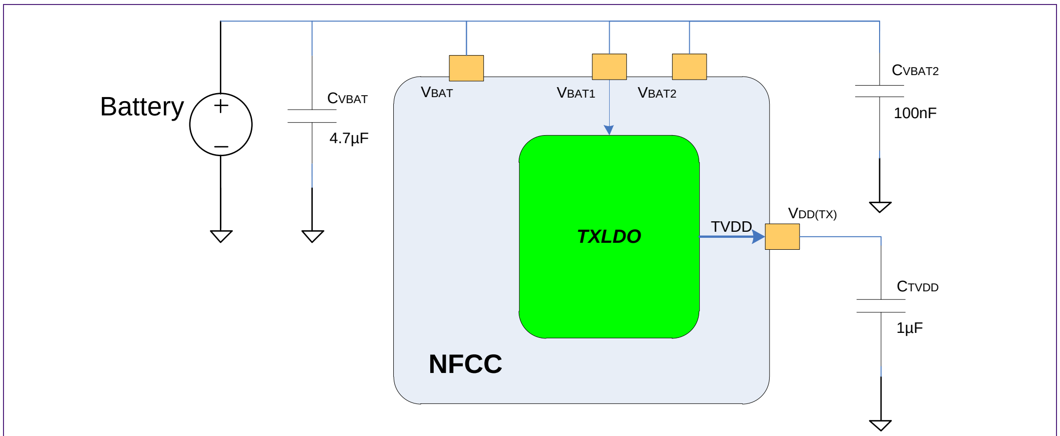


Fig 6. Power application schematic

6.4 TVDD power level

The strength of the field emitted by the PN7120 is linked to several parameters such as the antenna geometrical characteristics, the antenna matching circuit and the voltage level on TX output buffer.

The voltage level on TX output buffer is coming from TVDD. Typical TVDD influence on RF reading distance is depicted on the below picture:

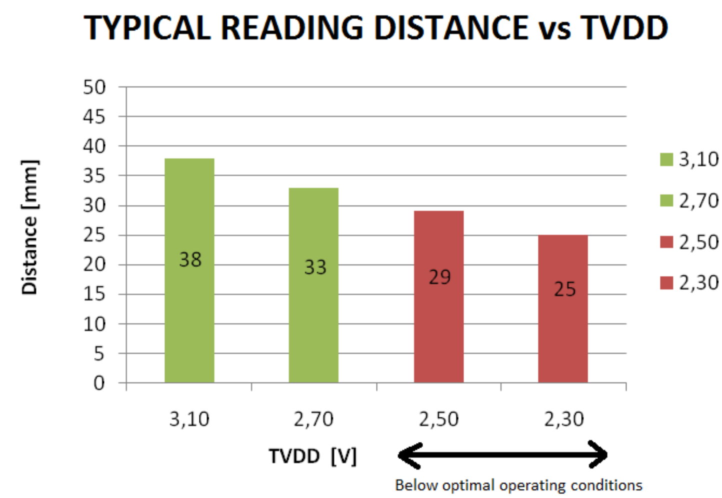


Fig 7. Typical reading distance vs TVDD

TVDD can be adjusted by software settings to be either 2.7V or 3.1V. When battery voltage drops below TVDD level, TVDD starts collapsing.

The figure below illustrates the expected voltage on TVDD versus the input battery voltage level for a given battery discharge cycle.

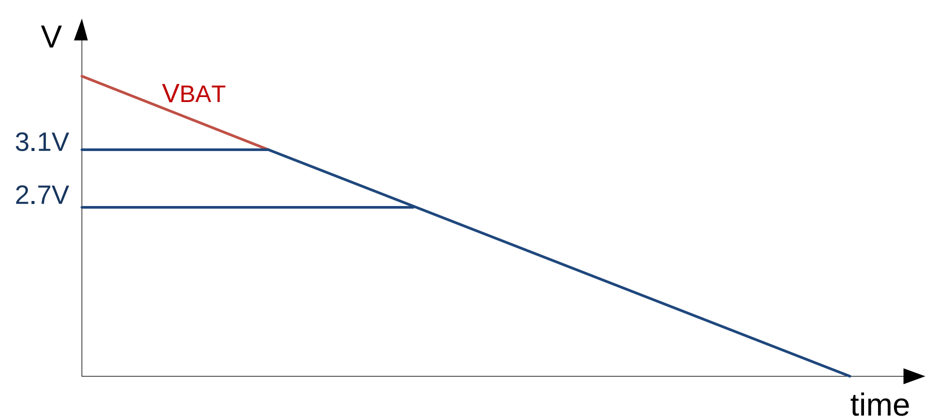
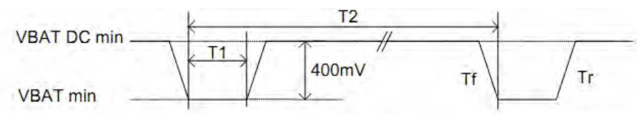


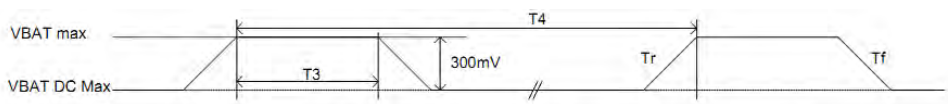
Fig 8. TVDD level vs. VBAT

In addition to these upper mentioned operating voltage ranges, the variation which can be seen on the battery voltage needs to be considered. The following battery voltage variation specification is taken as a reference:



Parameter	Min	Typ	Max
T1	577uS		2.31mS
T2		4.6mS	
Tr/Tf	10uS		

Fig 9. VBAT dip specification



Parameter	Min	Typ	Max
T3	3.91mS		
T4		1S	
Tr/Tf	200uS		2mS

Fig 10. VBAT peak specification

PN7120 is able to operate at fixed RF field strength in Poll mode with a continuous battery voltage down to:

a. 3.1V when TVDD is set to 2.7V

b. 3.5V when TVDD is set to 3.1V

The figure below shows 2 typical battery discharge cycles.

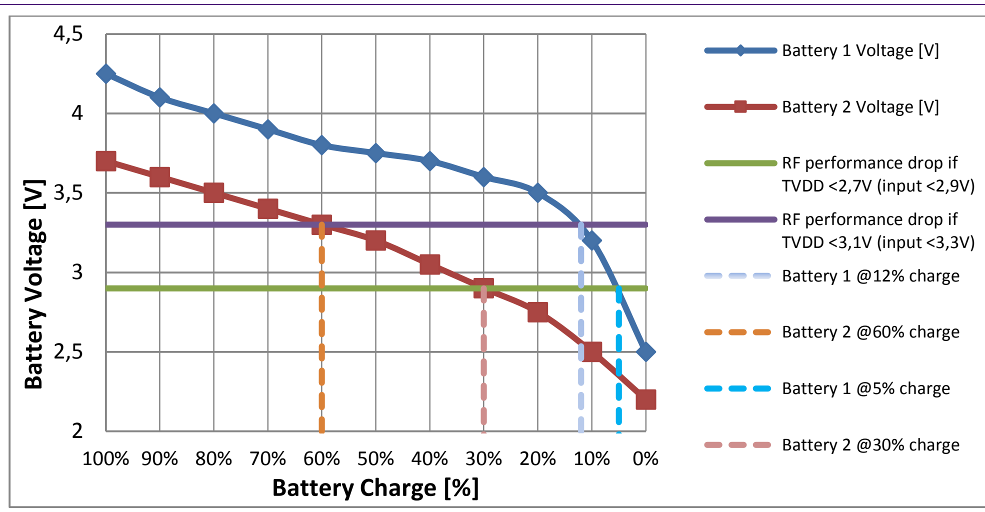


Fig 11. Battery discharge curve

7. Antenna interface

7.1 Typical matching circuit

The PN7120 is intended to be connected to an antenna through a matching circuit.

The typical topology for this circuit is depicted below:

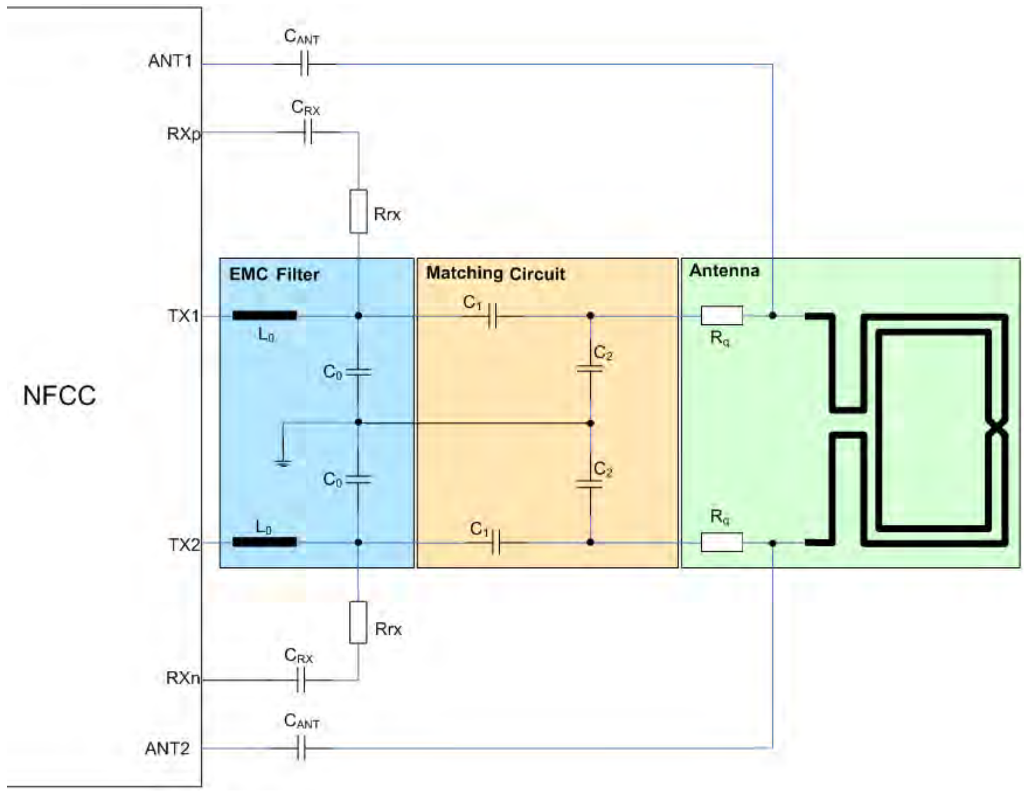


Fig 12. Typical antenna matching circuit

The components values are antenna dependent.

L_0 / C_0 are a 2nd order low pass filter used to reduce the spectrum power amplitude in the high frequency range but without altering the meaningful communication signal.

C_1 / C_2 / C_{ANT} are used to tune the Poll mode frequency at 13.56MHz and to adapt the equivalent impedance presented on TX1/TX2 at this frequency (70 ohms recommended).

The ratio between C_2 & C_{ANT} will define the Listen mode frequency and indirectly the back load modulation that the device is able to generate in front of a contactless reader.

R_q is optionally used to reduce the qualify factor of the antenna when it is above 35 (if it is already below, which is rather common in embedded equipment environment with ferrite shielding, R_q must not be placed)

How to select or design a proper antenna for the PN7120 and how to calculate the value of the matching components is explained in a dedicated application note. Please refer to the *PN7120 Antenna Design and Matching Guide [4]*

7.2 Matching circuit BoM recommendation

It is recommended to duplicate C1 and C2 in order to allow fine tuning of the Poll mode frequency and impedance:

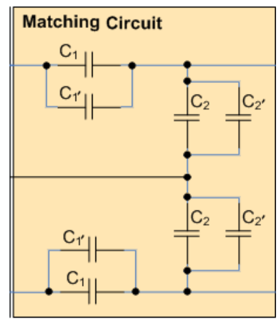


Fig 13. Matching circuit recommendation

7.3 Matching circuit BoM optimization

Based on careful technical consideration, the number of matching circuit components presented on the above schematics can be lowered.

7.3.1 Damping resistors

R_q damping resistors are used to lower the antenna quality factor when it is above 35. Indeed, a too high quality factor will negatively impact the generated signal shaping.

However, in an embedded environment, the presence of metal (battery, PCB tracks, electronic components...) tends to significantly reduce the antenna quality factor. Therefore, although they can be needed on an open-air board environment, it is very unlikely that these 2 resistors are required for embedded equipment integration.

Proof point:

Once the customer has measured its NFC antenna within its final environment he should calculate the resulting quality factor as explained in the *PN7120 Antenna Design Guide [4].* If the quality factor is below or equal to 35, R_q resistors can be safely removed.

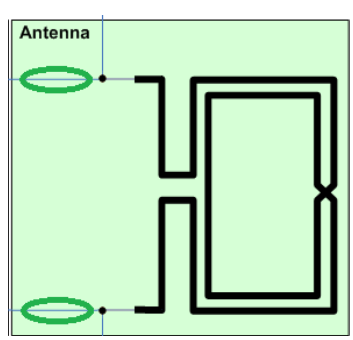


Fig 14. Optimized matching circuit: Rq removal

7.3.2 C_2 parallel capacitor

2 serial capacitors are used in parallel with the antenna to tune it to 13.56MHz.

The reason to have 2 capacitors in parallel in that the peak to peak voltage at antenna ends can reach more than 50V depending on the antenna geometrical characteristics (size, number of turns…)

However, if for a given antenna, the maximum peak to peak voltage measured at antenna ends is lower, then a single parallel capacitor on C_2 can eventually be used.

Its value needs then to be divided by 2 compared to the ones used in case of 2 serial capacitors solution.

Proof point:

As the voltage generated at antenna ends for a given external field power will be strongly linked to the antenna environment, this measurement must be performed within the final product.

It must be placed on an ISO/IEC10373-6 PCD assembly test bench and the maximum external field strength that an ISO/IEC14443 compliant device must withstand (12A/m) must be generated.

Then, the peak to peak voltage at antenna end must be measured with an oscilloscope using a low parasitic capacitor probe (2pF max).

Depending on the value measured, the customer can decide whether a single 50V parallel capacitor is suitable

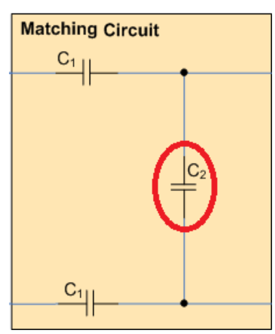


Fig 15. Optimized matching circuit: single C2

8. Power modes

- Hard Power Down (HPD)
- Full Power
- Standby

In order to get an overview of the different PN7120 power modes, a simplified figure is depicted below with VEN and VBAT as input parameters. The complete diagram including PVDD is given in *PN7120 Product Datasheet [1].*

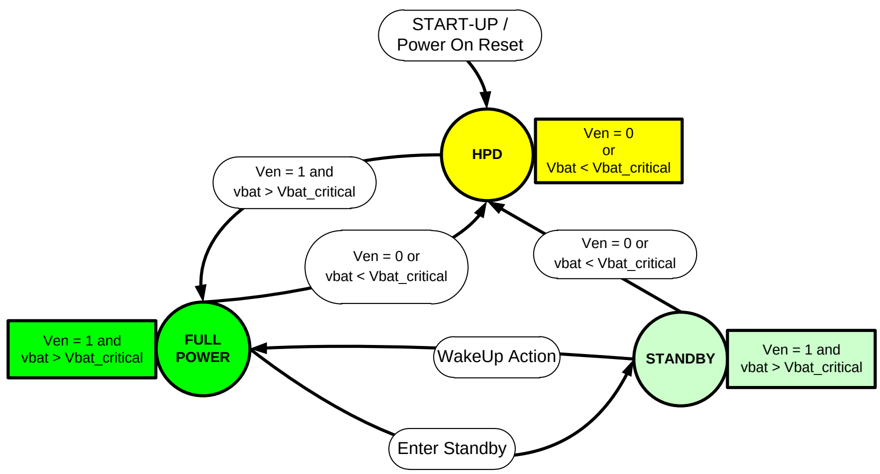


Fig 16. Power modes

When VEN is low or when the battery voltage is below its critical level the IC goes in Hard Power-Down mode.

When VEN is high and sufficient battery power is available, the chip is in full power mode. It can then switch to Stand-by mode if this mode has been enabled (Software configuration) and no activity has occurred on the host interface during a configurable duration.

The PN7120 resumes from stand-by to full power mode when an external or internal event occur (e.g. host interface communication, external field entry, internal discovery loop…)

9. Booster Control

In order to increase the RF performances, to achieve better communication distance for instance, an external booster can be added to the hardware design. The PN7120 offers a control of the booster circuitry to optimize the overall power consumption. This is done via the PN7120 BOOST_CTRL pin.

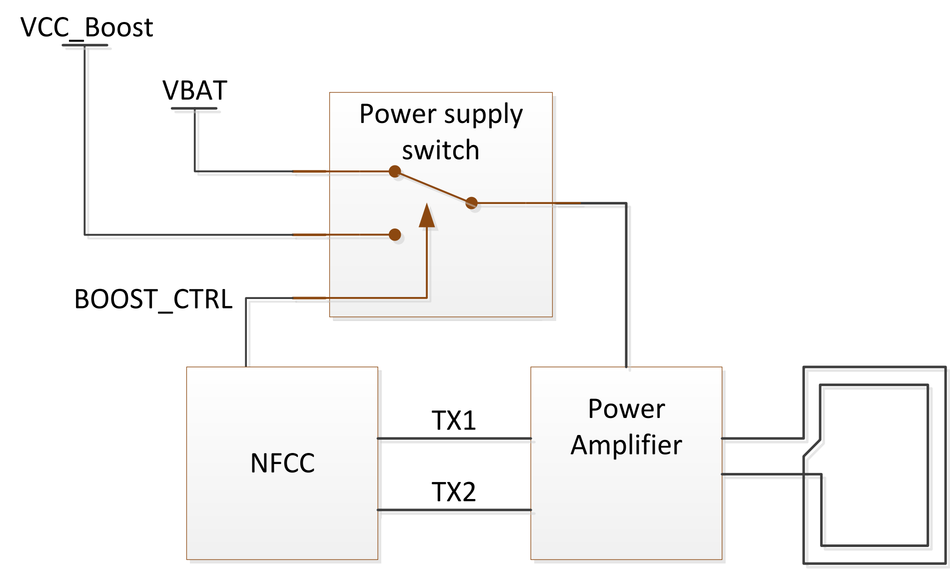


Fig 17. Booster enable/disable principle

The BOOST_CTRL pin is generally used as input for the host interface (default behavior) but it can be configured as Booster Control output with an EEPROM configuration.

The configuration register is the tag bBoosterCtrl at address 0xA060 which can be set through the CORE_SET_CONFIG_CMD.

This EEPROM parameter bBoosterCtrl is used as follows:

bit[7]: Use booster for EMVCo polling profile

bit[6]: Use booster for NFCForum polling profile

bit[5]: Use booster for LPCD (Low Power Card Detector = Tag Detector)

bit[4]: Reserved

bits[0:3]: Booster startup time in 128us steps, 16 steps, max. 1920us

For each enabled mode, the NPC100 fully handles the Booster Control pin HIF2 to enable the booster when RF is required.

If bBoosterCtrl is not 0x00, then the HIF2 pin is configured as output (Default value is 0x00)

The booster startup time depends on the booster implementation.

The following diagrams show different booster behavior depending on the booster control register configuration.

bBoosterCtrl = 0x8X: EMVCo Polling

Fig 18. Booster only used during EMVCo application

bBoosterCtrl = 0x4X: Booster enabled during NFC Forum polling

- Example with no tag detector

Fig 19. Booster NFC Forum – No tag detector

- Example with no tag detector

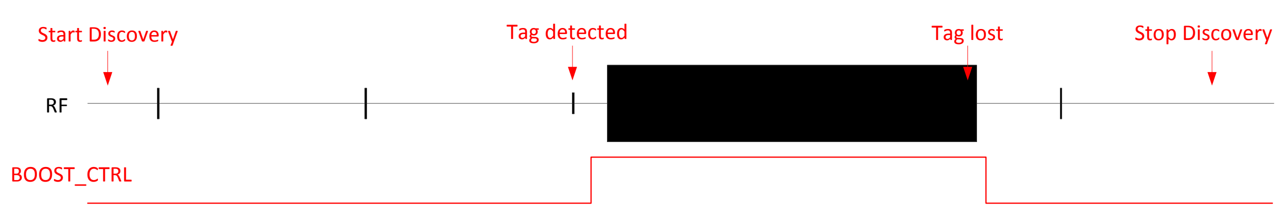


Fig 20. Booster NFC Forum – Tag detector enabled

bBoosterCtrl = 0x6X: Booster enabled during NFC Forum polling and during tag detector.

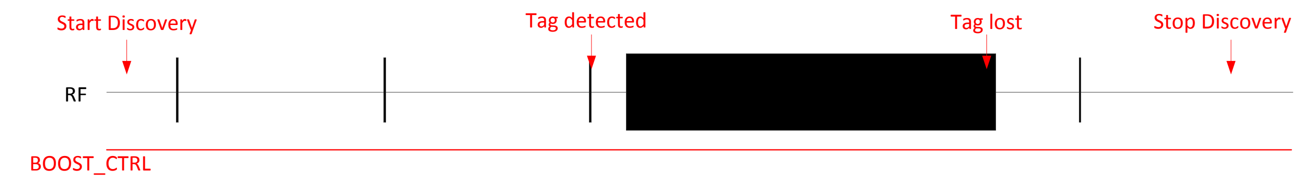


Fig 21. Booster NFC Forum – Tag detector enabled

Based on this PN7120 control of the booster, proposed implementation is depicted in below schematics:

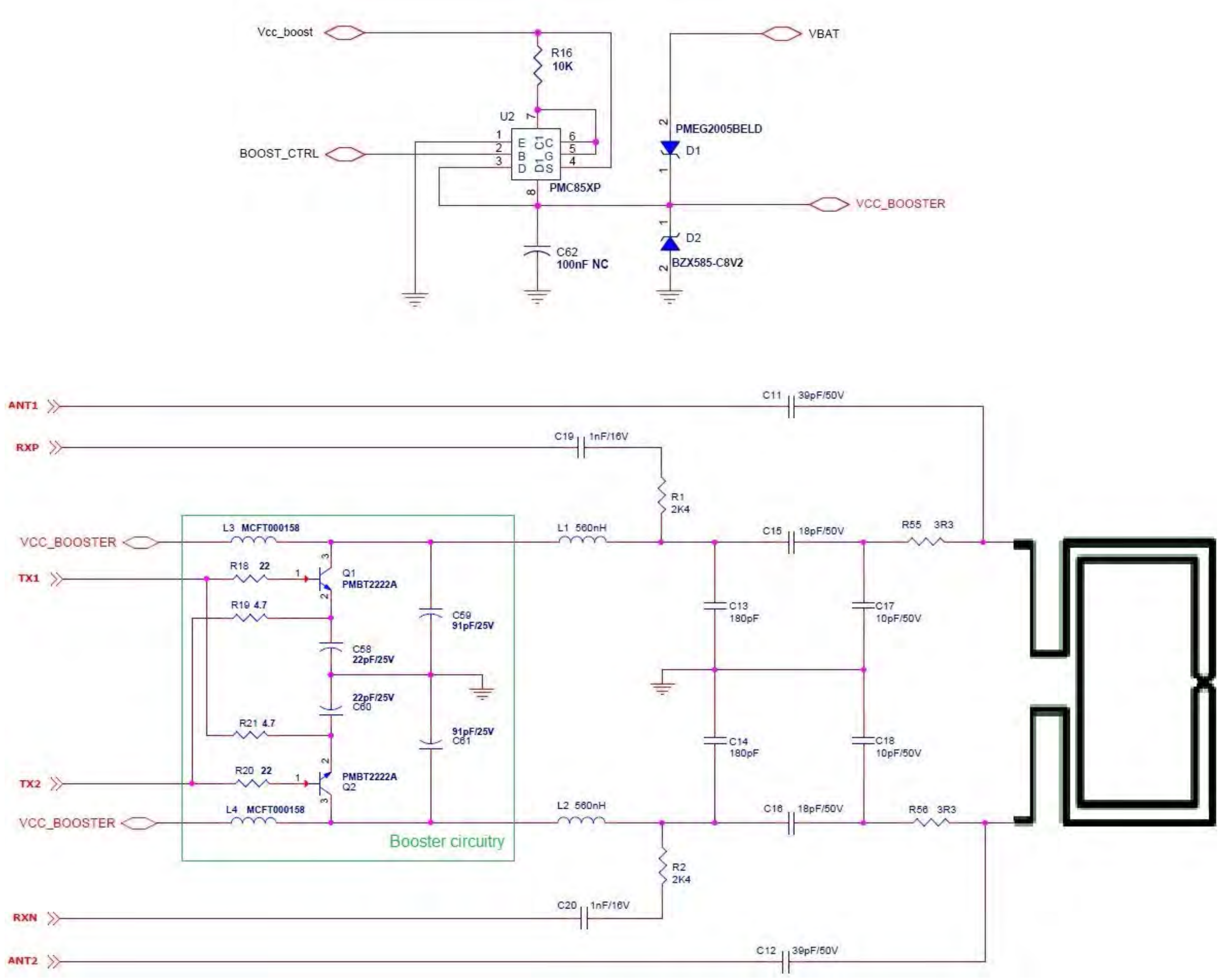


Fig 22. Booster implementation example

10. Layout guidelines

10.1 Antenna EMC inductors

The selection of the EMC inductors is key for best performance. There are several parameters to take into account when selecting a reference, as described below:

- High-Q factor (@ 13.56MHz) is preferred. Its dependencies are:
  - Size (e.g. 603)
  - Inductance value (e.g.160nH)
- AC Current Characteristics (depending on µ saturation vs. H value)
  - The flat test inductance variation vs. AC current increase (Ip-p) is preferred.
  - Still, the inductance might be rather flat until a certain amount of Ip-p current (e.g. 100mA), which can be good enough for an application
- Coupling effect
  - The lowest coupling factor vs. distance between coils is preferred

Suppliers generally provide two types of technology, Wire-wound and Multi-layer inductors. The following table summarizes the benefits of each technology. One shall select the best compromise vs. all parameters.

Table 5. Inductance characteristics

	Q-Factor	AC current µ saturation	Coupling
Wire-wound		✓	
Multi-layer	✓		✓

To minimize the coupling effect, there can be several inductance placements as depicted in the below Fig 22:

- Parallel
  - When the field lines are parallel, they can couple each other and the system gets potentially de-tuned
- 90° or T-mount
- Symmetrical or series mounted

Please take care of the rules provided by your supplier for the optimal placement. During the matching process this might not be directly seen as an impedance analyzer typically delivers some few mW of power. During operation, the PN7120 can introduce far more than few mW which causes a very much different field distribution compared to the one captured with the impedance analyzer.

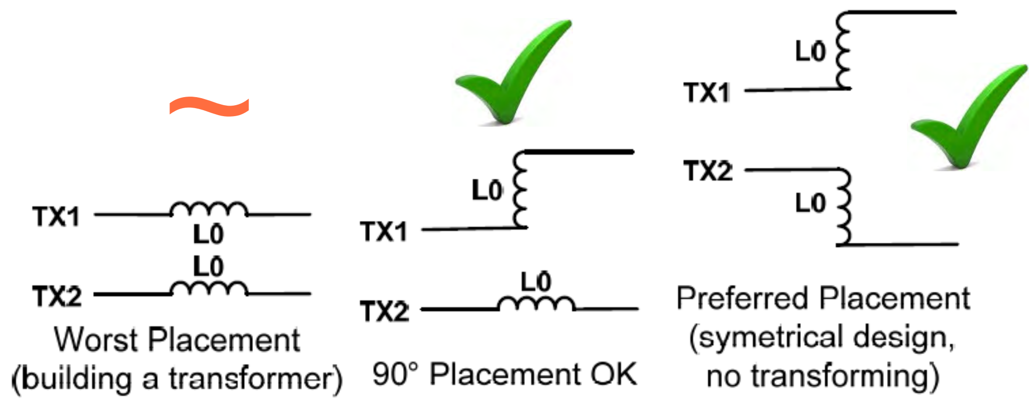


Fig 23. Recommended EMC Inductances Placement

PN7120 EMC inductors have been verified with several references as given below. Other references might be suitable, but only the ones below have been properly checked by NXP.

- TDK
    - MLF series: e.g. MLF1608
- MURATA
    - Multi-layer parts: LQB18 series
    - Wire-wound parts: LQW18 series

10.2 RF paths

All the signals are quite sensitive to noise hence some ground plane shall be applied all around these paths to minimize radiation from the circuit towards other system components and vice versa.

In particular, RF paths must be kept away from clock lines.

Track length must be minimized and a symmetrical routing must be used wherever possible.

Line crossing must be avoided as it would imply some voltage/current induction between the different paths.

A possible top level implementation of the Antenna matching circuit is shown below:

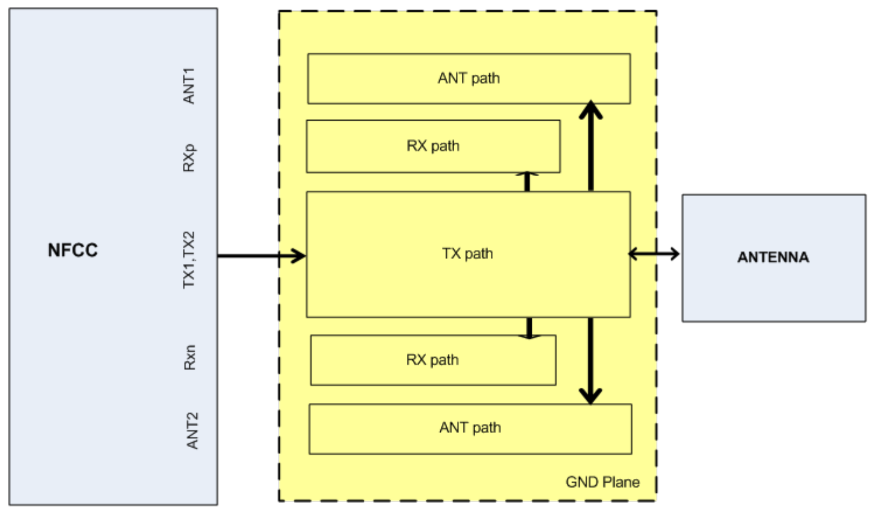


Fig 24. RF paths floorplan

The PN7120 reference design layout depicted below can be used as an example of proper antenna components routing.

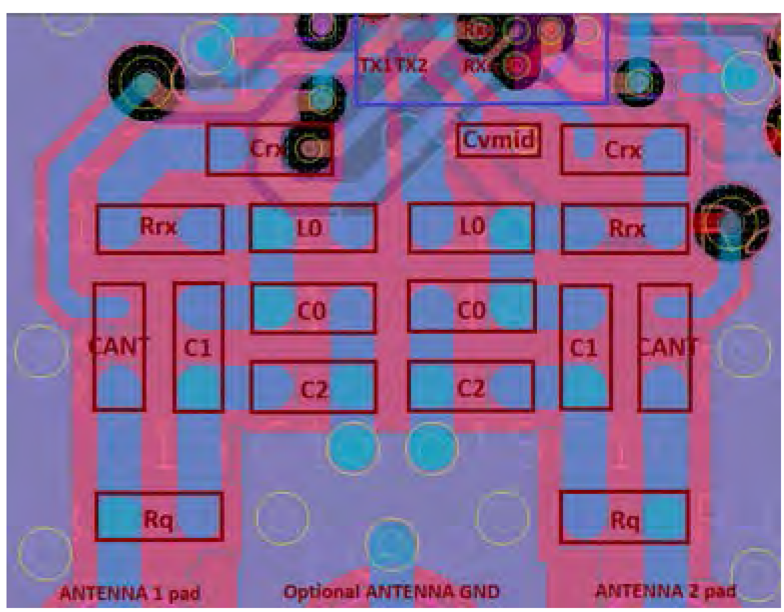


Fig 25. Antenna matching layout example

Please note that you shall take care of having multiple vias to connect different ground layers in order to avoid too resistive bottleneck, especially on the TX path grounding.

10.3 XTAL layout recommendations

The XTAL must be connected as close as possible to the CLK1 and CLK2 pins from the PN7120 to achieve the best performances as possible.

Please follow these guidelines for the layout of the XTAL connections:

- As the XTAL is very sensitive to parasitic capacitance and noise, we advise to:
    - put the XTAL far from other signals (especially other CLK lines or signals with frequent switching)
    - limit the crosstalk between CLK lines and other signals
- Load capacitor connections:
    - Choose capacitor with a good temperature stability like COG
    - Place the capacitors closed to each other and close to the XTAL
    - Avoid to connect them to a dirty ground (perturbed by return current from others functionalities on the board like USB, PWM or power supply lines)

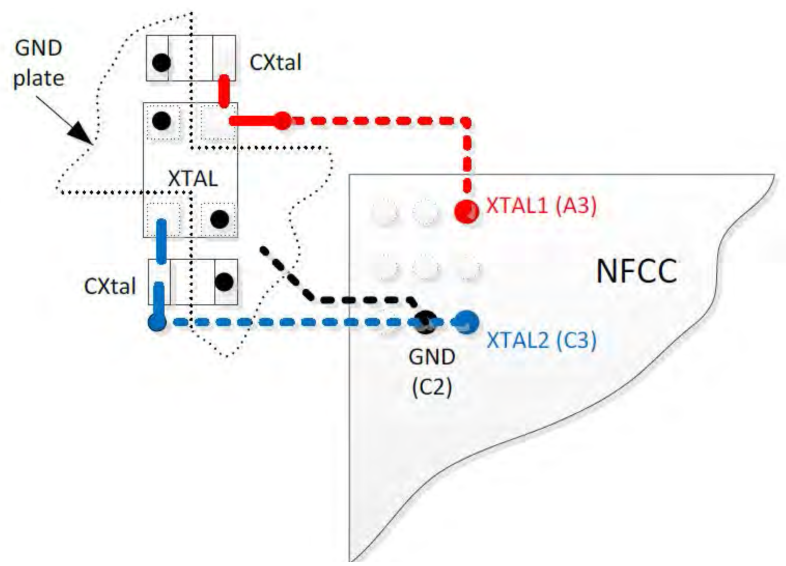


Fig 26. XTAL connection example

10.4 Input clock

Clock signal must be:

- Shielded from the rest of the board
- Kept as short as possible

10.5 De-Coupling (blocking) capacitors

Standard layout rules consisting in decoupling capacitors being placed as close as possible to the chip apply.

11. Q&A

- **How to optimize the NFC controller power consumption when the host controller is shutdown or enters stand-by mode?**

  The PN7120 can be configured to enter into standby mode when there is no activity from the host controller side after a programmable timeout (see configuration details in the *PN7120 User Manual [2]*).

  Standby mode can be activated by setting the proper EEPROM configuration and it is retained (so only need to be activated once if not disabled afterwards).

- **When using the PN7120, is it mandatory to connect VBAT2 to VBAT?**

  When using PN7120 a connection is made on the substrate between VBAT and VBAT_DCDC. It is not necessary to connect VBAT2 to VBAT. Only a decoupling capacitor must be placed.

12. References

[1] PN7120 Product Datasheet

[2] UM10819 – PN7120 User Manual

[3] I²C Bus Specification

[4] AN11564 – PN7120 Antenna Design Guide

13. Abbreviations

Abbr.	Meaning
AN	Application Note
BoM	Bill of material
CLK	Clock
EEPROM	Electrically Erasable Programmable Read Only Memory
GND	Ground
GPIO	General Purpose Input Output
HW	Hardware
I²C	Inter-Integrated Circuit (serial data bus)
IC	Integrated Circuit
IO	Input / Output
IRQ	Interrupt Request
ISO/IEC	International Standard Organization / International Electrotechnical Community
mA	milli Ampere
MHz	Mega Hertz
mW	milli Watt
NFC	Near Field Communication
NFCC	NFC Controller (i.e. PN7120)
OS	Operating System
PCD	Proximity Coupling Device (Contactless reader)
PICC	Proximity Integrated Circuit Card (Contactless card)
PMU	Power Management unit
RF	Radiofrequency
RST	Reset
VEN	V ENable pin (Hard reset control)

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15. List of figures

16. List of tables

17. Contents

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