

# AN11738

## PN7462AU - Contact Smart Card application

Rev. 1.1 — 13 February 2017  
344211

Application note  
COMPANY PUBLIC

### Document information

Info	Content
Keywords	PN7462AU, Contact Smart Card, ISO7816
Abstract	How to use contact smart card interface on PN7462AU



## Revision history

Rev	Date	Description
1.1	20170213	Card activation chapter updated
1.0	20160309	First release

## Contact information

For more information, please visit: <http://www.nxp.com>

## 1. Introduction

### 1.1 Presentation

The PN7462AU is a contact + contactless smart card interface. This document focuses on contact interface only.

This device supports asynchronous cards (micro controller-based IC cards) as well as synchronous cards.

The electrical characteristics of the PN7462AU are in accordance with ISO7816-3 for class A, B and C cards.

The PN7462AU can be used in various applications such as USB readers, Point-Of-Sale terminals (POS), SAM reader, vending machines, and many conditional access applications (i.e. Internet,...).

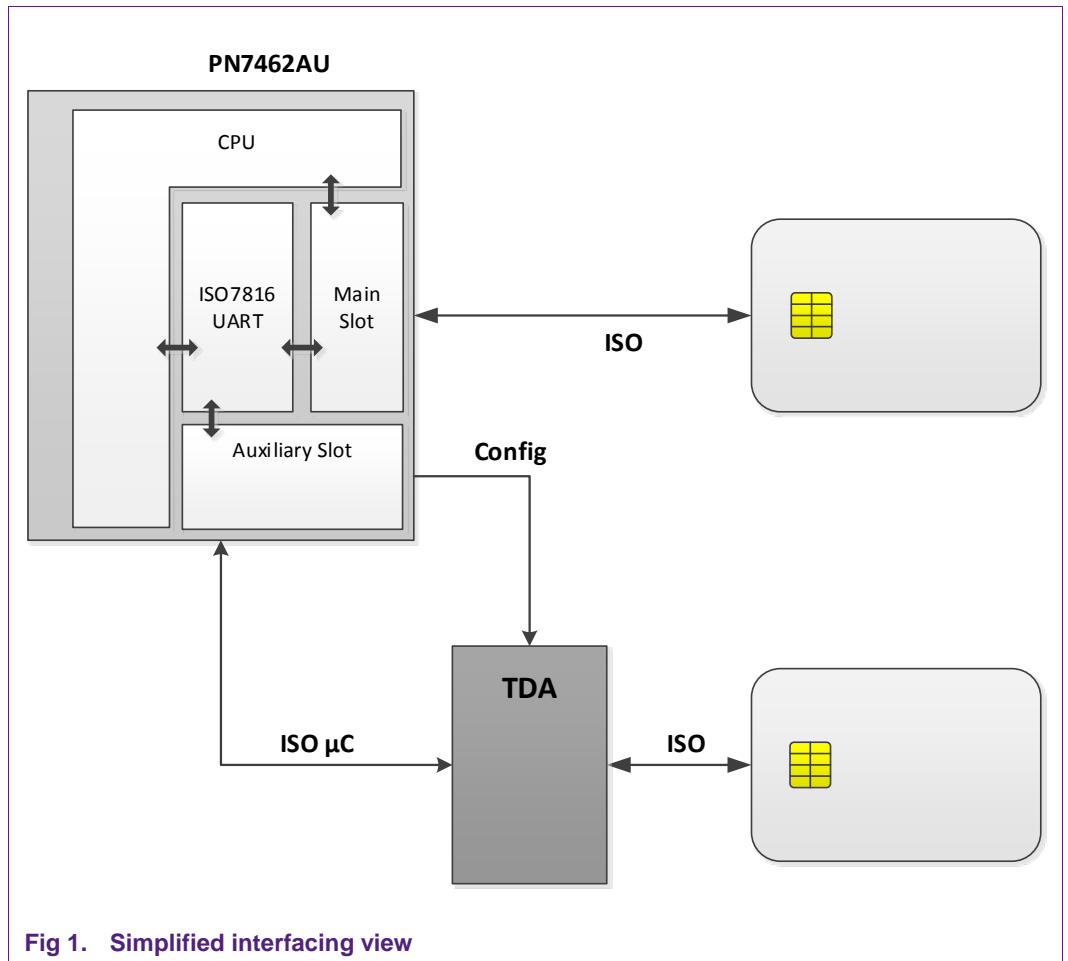


Fig 1. Simplified interfacing view

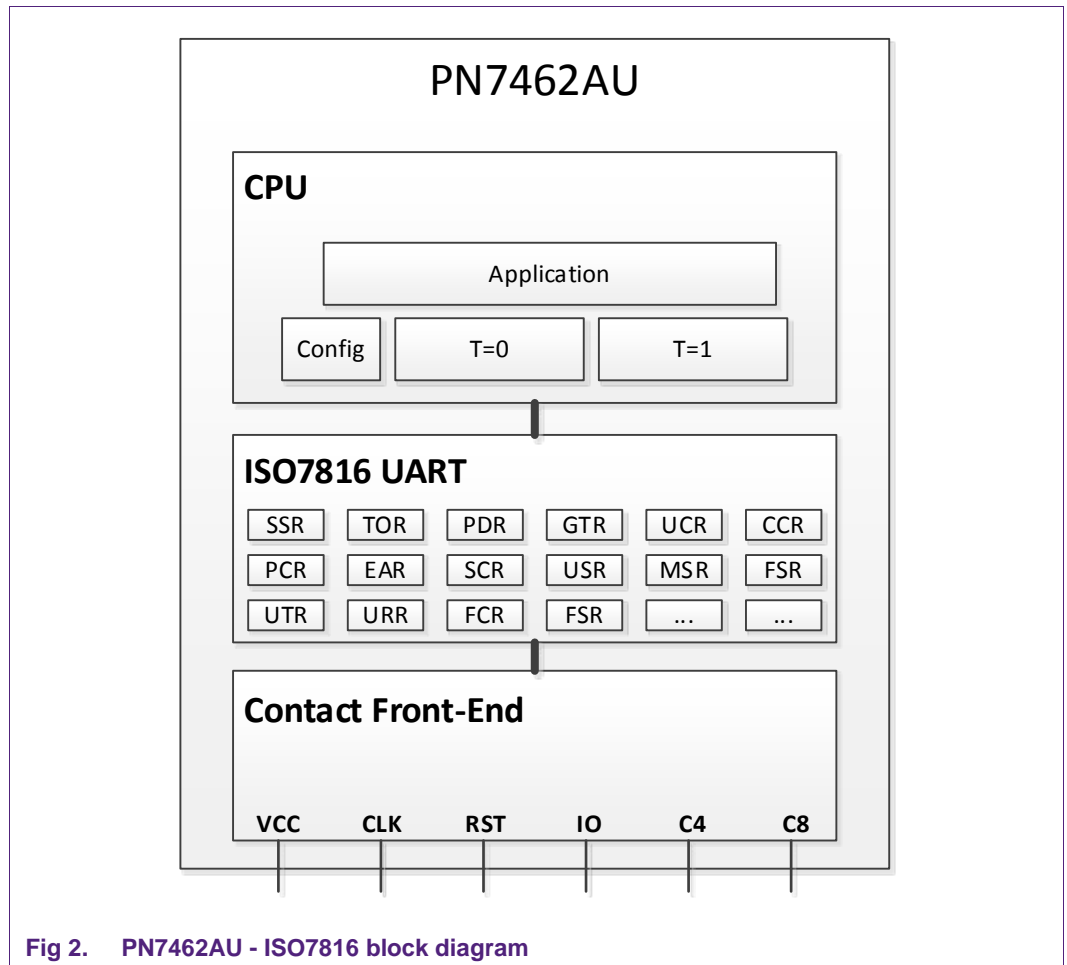
The current documentation will mainly focus on the main slot.

## 1.2 ISO7816 Management

The PN7462AU fully handles ISO7816 standard:

Electrical interface is handled by the Contact Front-End

Digital management is performed thanks to an embedded ISO7816 UART for the low level protocol part, and the host SW running in the CPU for the high level protocol.



The ISO7816 UART block is a set of registers and digital management. It fully handles ISO7816 low level as specified in ISO7816-3.

This block is responsible for configuration of the communication with the smart card, and the management of bytes exchanged over I/O line.

The next figure summarizes the task of each block within data exchange.

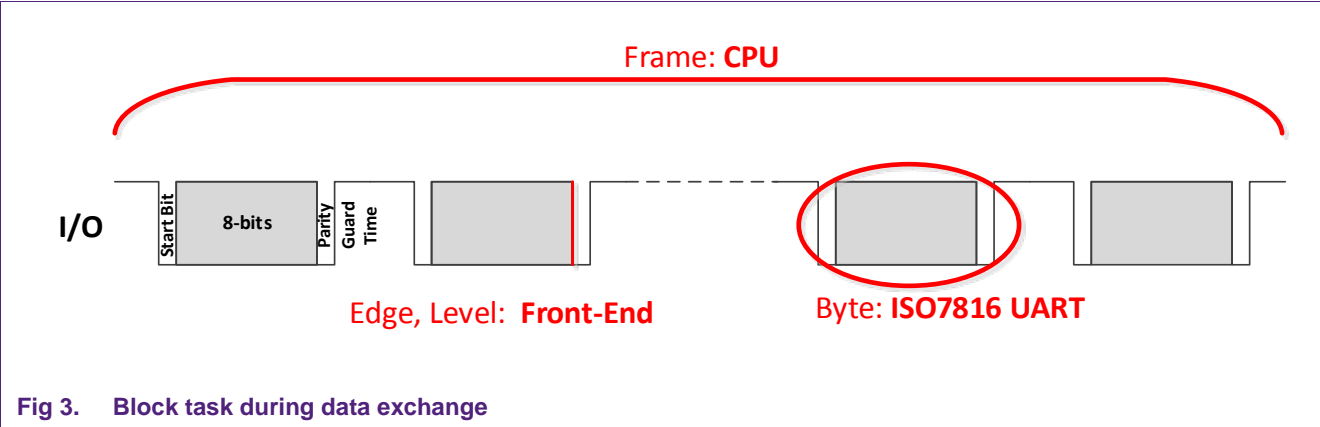


Fig 3. Block task during data exchange

## 2. Power supply

---

### 2.1 Power supply pins

The Power Supply strategy of the PN7462AU is defined in the User Manual. The document describes the main way to provide power supply to the chip, as well as the specific power supply for the contact interface.

As an example, in case PN7462AU contact interface only is used, below power supply must be present:

- VBUS (Main power supply of PN7462AU)
- PVDD\_IN (GPIO power reference)
- VBUS\_P (Input for the Contact Card Power supply generation)

### 2.2 DC/DC Converter

The PN7462AU embeds a DC/DC converter that allows converting a voltage level as low as 3 V to an output on the card side up to 5 V.

The DC/DC input power supply can go down to 2.7 V for Class B and C cards (3 V and 1.8 V)

This block is supplied through VBUS\_P, and its reference ground is GNDP.

2.2.1 Schematics

This DC/DC converter works with a capacitor step-up mechanism, and uses 2 capacitors on SAM-SAP, and VUP

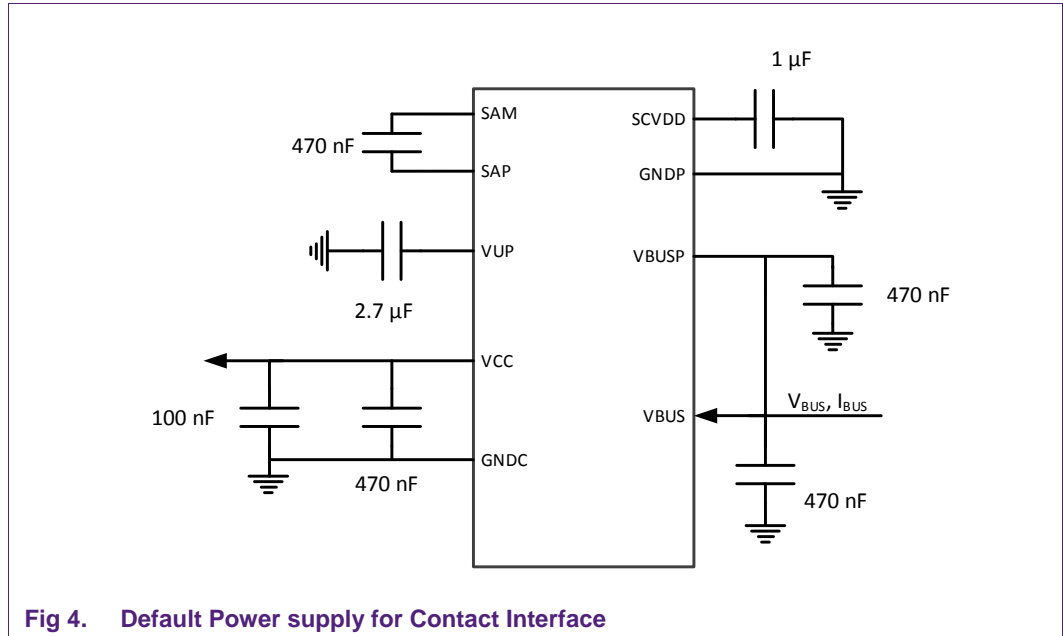


Fig 4. Default Power supply for Contact Interface

The DC/DC converter operates as a charge pump using capacitors on Sx pins, and Vup. With these pins the converter can operate as a voltage follower or doubler. This allows to use a VDDP down to 3 V to generate 5V, or down to 2.7V to generate 3V, and then allows to use the same voltage level for VBUS and VBUS\_P.

2.2.2 Layout

The DC/DC converter components layout must be designed respecting the following guidelines:

- The capacitor on VBUS\_P has to be routed close to the VBUS\_P pin and with a very short and low resistive connection to the GNDD pin.
- The capacitor on VUP has to be placed close to VUP and with a very short and low resistive connection to the GNDD pin.
- The capacitor on SAP/SAM must be placed close to the pins.
- The connection between GNDD and the main Ground has to be very short and direct. It is important that the shortest track for GNDD back signal doesn't flow through the PN7462AU, but directly to the main power supply input, through low resistive PCB tracks (ground plan).
- Routings of VBUSP (from battery), VUP and SAP/SAM should also be of very low resistance.
- Using VIAs to route these DC/DC signals must be avoided.
- It must be ensured that no critical routing passes over or underneath SAM/SAP routings.

### 3. Contact Clock

The Contact clock generation relies on the external clock provided to the PN7462AU. This external clock is the 27.12 MHz crystal connected on XTAL1 and XTAL2.

Refer to the User Manual for all details about general clock configuration for PN7462AU.

#### 3.1 Clock selection for contact interface

The Contact interface uses the system clock. This clock is necessary to generate the clock for the smart card and manage the data exchange over I/O line.

In order to get the clock available for the clock interface, two register bits have to be set:

CLOCK\_CTIF\_ENABLE in PCR\_CLK\_CFG\_REG

And

IPCLOCK\_CTIF\_ENABLE in PCR\_CLK\_CFG\_REG

The default system clock frequency is set to 27.12 MHz.

Refer to the User Manual for information on how to change the system clock. The examples in this document are based on this system clock set to default.

#### 3.2 Generation of Smart Card CLK

The clock is automatically provided by the PN7462AU to the smart card over the CLK pin when the card activation is requested.

The Host action on this clock is to define its frequency. This can be done using Contact Interface registers CT\_CCR1\_REG:

CT\_CCR1\_REG defines the divider for the system clock to generate the card clock thanks to the ACC bits (bits 0, 1 and 2):

System clock can be divided by 1, 2, 3, 4, 5, 6, 8, 16.

With a default system clock of 27.12 MHz, this gives possible output frequencies of:

27.12 MHz, 13.56 MHz, 9.04 MHz, 6.78 MHz, 5.42 MHz, 4.52 MHz, 3.39 MHz or 1.69 MHz.

For standard ISO7816 or EMVCo operation, it is mandatory to use a card clock frequency lower than 5MHz for card activation. The recommended value is Clk/6 → ACC[2:0] = 101b.

This has to be done prior to the card activation so that the automatic activation uses the right parameters.

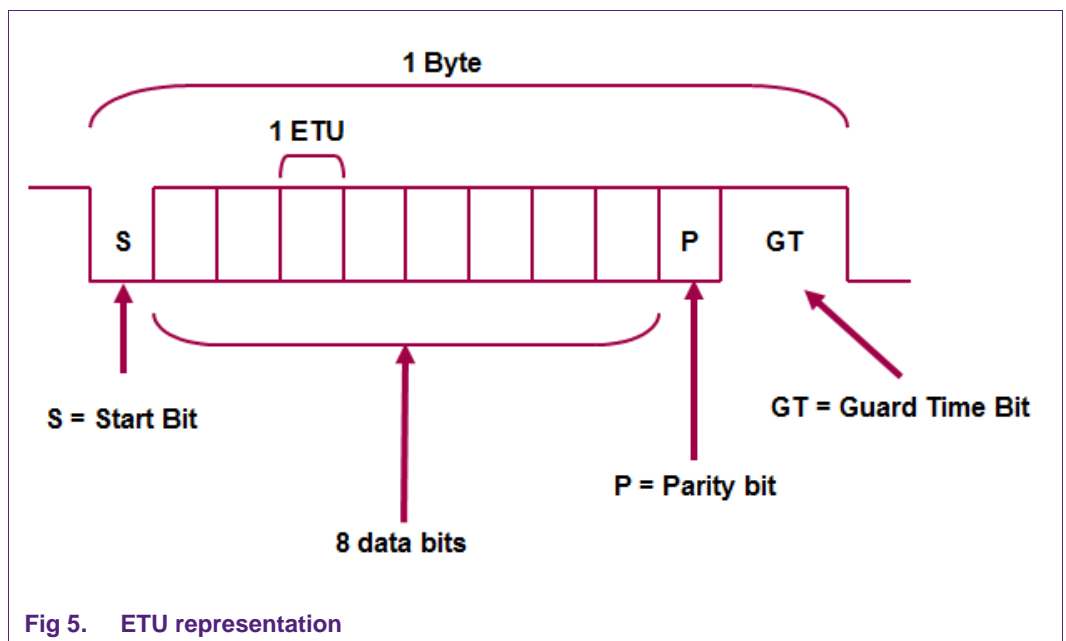


### 3.3 ETU management

The system clock is also used to handle the data sent and received over the I/O line. The principle here is to generate the ETUs based on a defined number of clock cycles.

#### 3.3.1 ETU definition

As a reminder, the data baudrate is defined in ISO7816 with the ETU length. ETU stands for Elementary Time Unit and represents one bit of communication:



The default length for one ETU is set by ISO7816 to 372 Clock cycles (referenced to the clock sent to the smart card). This is the value to be used during card activation (ATR reception).

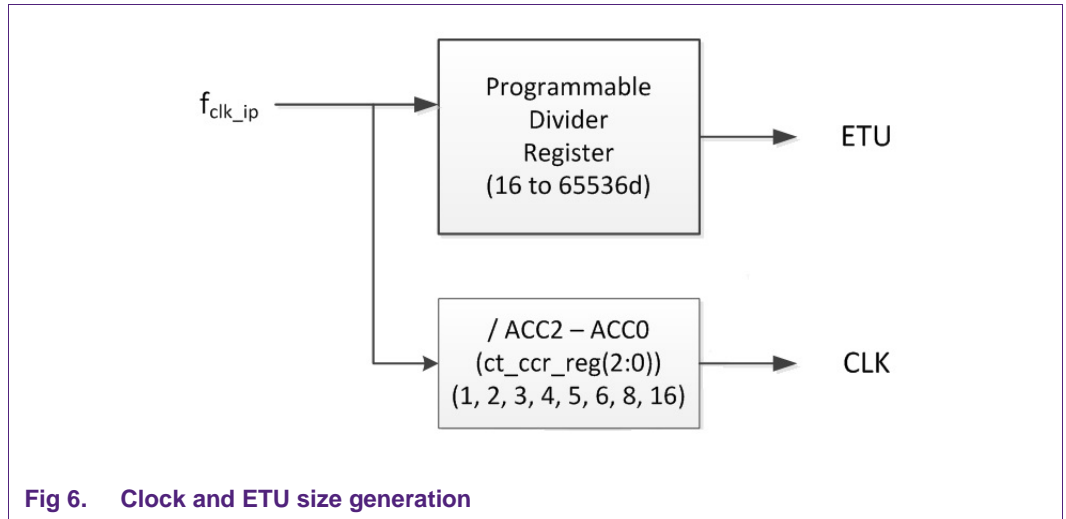
Due to this definition (ETU length set as a number of clock cycle), the exact time will always depend on the clock frequency.

#### 3.3.2 ETU size configuration

The PN7462AU defines ETU size as a specified number of clock cycles.

**Important Note:** The reference clock for this ETU size definition is not the clock sent to the smart card, but the input clock of the Contact Interface. Here it is the system clock set to 27.12 MHz.

The following figure shows this specific management: Card clock and ETU management use the same input.



Two registers are used to define the ETU size:

CT\_PDR1\_LSB\_REG and CT\_PDR1\_MSB\_REG. This two registers allow to define an ETU size set from 16 to 65536 clock cycles.

The minimum size is set to 16 in order to give enough margin for the digital interface to compute the data.

The advantage of this mechanism is that it allows more precision and flexibility in computation of the ETU. Also it allows to reach non integer value of clock cycles.

For example, when a card FiDi is set to 0x19 (Fi = 1, Di = 9 ; F = 372, D = 20), the number of clock cycles per ETU must be 18.6. If the input clock for ETU computation is the clock sent to the card, it is only possible to define ETU size of 18 or 19. This would lead to an out-of-spec operation.

Thanks to this mechanism, it is possible to set the Card clock frequency to  $f_{CLK}/6$  and PDR set to 112.

Then the real ETU size becomes equal to 18.67 clock cycles:  $(= 112 / 6)$ . This is within the ISO specification as the maximum allowed deviation for 10 ETUs is 0.2 ETU.

This 18.67 instead of 18.60 gives a deviation of 0.04 ETU.  $(= 10 * \frac{18.67 - 18.60}{18.60})$

For even more precision, it is possible to set the card clock frequency to  $f_{CLK}/8$ , and PDR to 149. The ETU size then becomes 18.63, and the deviation is only 0.01 ETU.

Of course there is more precision, but the baud rate changes: With PDR 112 and clock division set to 6, the clock frequency is 4.52 MHz and the baud rate is 243.01 kbps.

With PDR 149 and clock division set to 8, the clock frequency becomes 3.39 MHz and the baud rate is now 182.26 kbps.

## 4. Card connector

---

### 4.1 Presence pin

One input pin is available to detect the card presence: PRES.

This pin is active LOW by default, but this can be changed with configuration registers, depending on the card connector type which is used (normally open or normally closed).

It can be configured to have an internal resistor either to GND or to PVDD\_IN.

The configuration bits to set the mode of PRES are PRES\_CON\_NO and PRES\_PUP\_EN from register CT\_SSR\_REG.

Depending on the type of card connector used, these register bits have to be configured prior to any action on the card interface.

The goal of this configuration possibility is to be able to use any card connector type, without the need of any external component.

The next chapters present all the different ways to configure the smart card connector presence switch, depending on the switch type. There are 4 possibilities: 2 for each configuration.

It is recommended to use the configuration with Pull-up enable bit is set to 0 for each type. The reason is that this is the default configuration for this bit. Using this value will then help to avoid any false card presence detection at chip boot-up.

**4.1.1 Normally open presence switch**

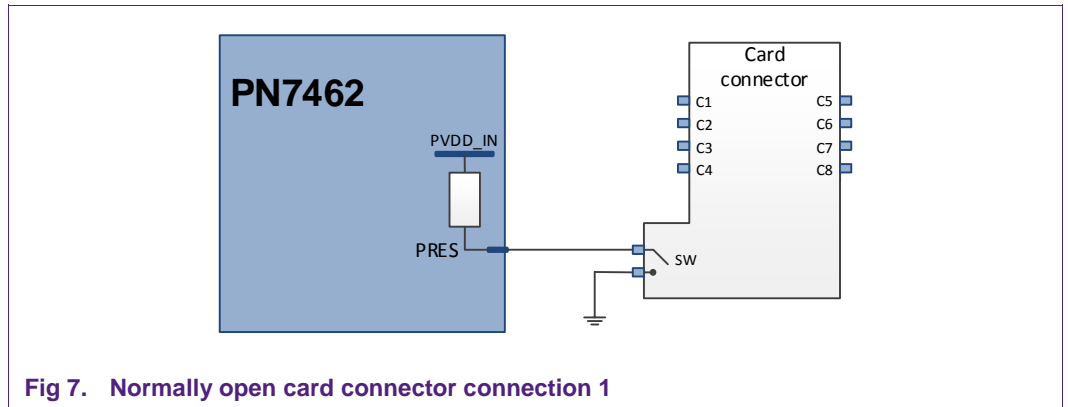
When such a card connector is to be used, the PN7462AU has to be configured in one of the two following ways to allow a direct connection without external pull-up or pull-down resistor.

**4.1.1.1 Normally open configuration 1**

PRES\_PUP\_EN = 1 → to set an internal Pull-up on PRES

PRES\_CON\_NO = 1 → to configure internal management for normally open connector.

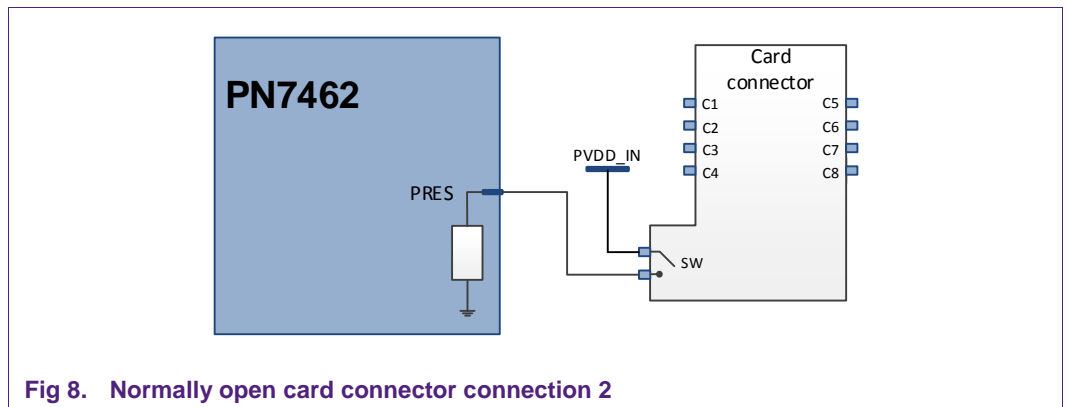
When configured this way, the following schematics can apply:



**4.1.1.2 Normally open configuration 2 (recommended configuration)**

PRES\_PUP\_EN = 0 → to set an internal Pull-Down on PRESN

PRES\_CON\_NO = 1 → to configure internal management for normally open connector.



**This is the recommended configuration for normally open card connector presence switch.**

**4.1.2 Normally closed presence switch**

To use this type of card connector, the PN7462AU has to be configured in one of the following 2 ways:

**4.1.2.1 Normally closed configuration 1**

PRES\_PUP\_EN = 1 → to set an internal Pull-Up on PRESN

PRES\_CON\_NO = 0 → to configure internal management for normally closed connector.

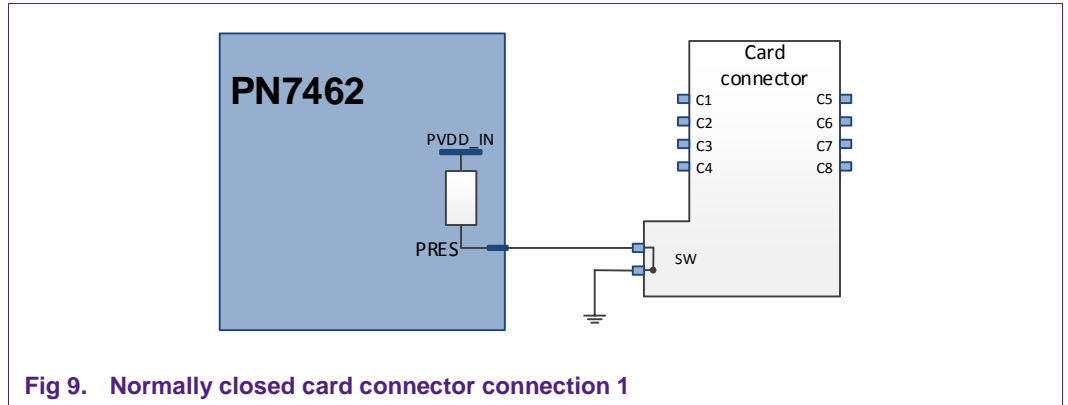


Fig 9. Normally closed card connector connection 1

**4.1.2.2 Normally closed configuration 2 (recommended configuration)**

PRES\_PUP\_EN = 0 → to set an internal Pull-Down on PRESN

PRES\_CON\_NO = 0 → to configure internal management for normally closed connector.

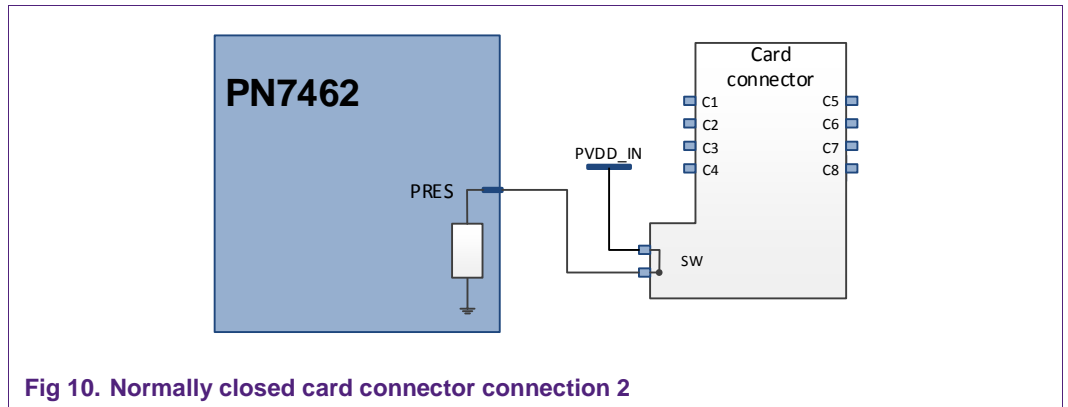


Fig 10. Normally closed card connector connection 2

**This is the recommended configuration for normally closed card connector presence switch.**

### 4.1.3 Debouncing

With some card connectors, depending on the mechanical characteristics of the switch, bouncing may be seen on the PRES pin when a card is inserted or extracted. This bouncing is managed by the PN7462AU which does not transfer exactly the PRES state to the internal presence management signal.

When the card is inserted, the PN7462AU waits for the PRES pin to be stable for typ. 6 milliseconds before assuming that the card is inserted. When the card is extracted, the chip acts as soon as the presence is not active. This behavior is summarized in Fig 11:

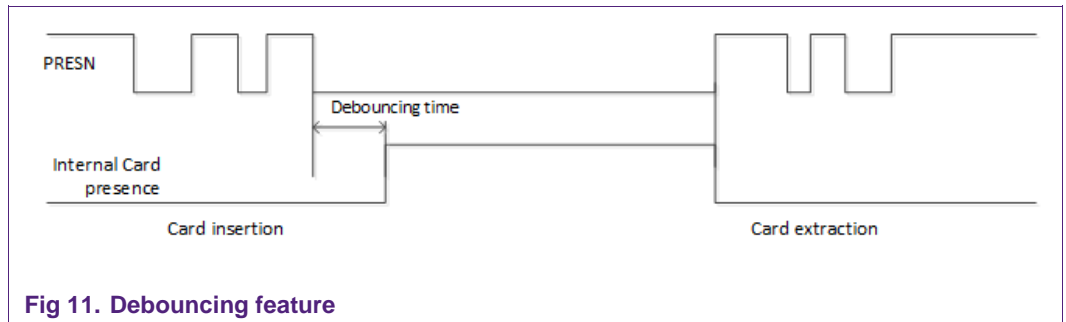


Fig 11. Debouncing feature

4.2 Schematics

To connect the smart card connector to the PN7462AU, only two capacitors are mandatory as external components. The schematic reference is given in Fig 12.

The C1 capacitor must be placed near the PN7462AU and C2 must be connected close to the card connector.

The advised values for C1 and C2 are respectively 220 nF and 220 nF. These values are mandatory to have a ripple on VCC in the specified limits.

Pins C4 and C8 of the card connector (connected to pins AUX1 and AUX2) are optional. They can be left unconnected unless some specific operation using these pins is required.

It is not advised to leave pin VPP (C6) unconnected. It can be connected directly to VCC or GND in accordance with latest ISO 7816 standards. Connecting it to VCC allows it to be compliant with older cards which might not support VPP connected to the Ground.

For more flexibility, the design should include a 0 ohm serial resistor between VPP and VCC. Then the application can be easily adapted if needed.

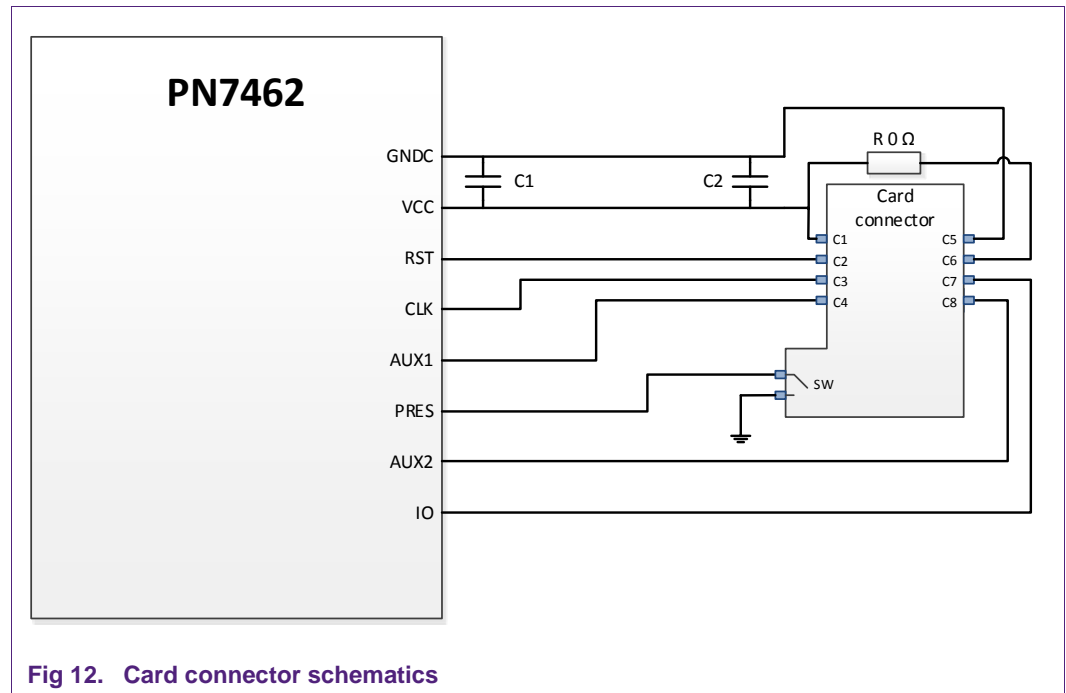


Fig 12. Card connector schematics

Note: In case the contact reader is used for EMVCo application, a change in this schematics is required. See section 7 EMVCO Certification.

## 5. Card configuration

The chip can be configured dynamically to operate with the connected card.

### 5.1 Card voltage

The voltage level can be set to 5V, 3V or 1.8V.

This configuration uses bits [VCCSEL1:VCCSEL0] from register CT\_PCR\_REG (= bits [3:2]).

The voltage level has to be configured before activation. The application **MUST NOT** change the value of these pins when the card is activated.

To change the voltage level of the card, the host must deactivate the card, change the voltage level value and then re-activate the card.

**Table 1. Select voltage pin behavior**

Command	VCCSEL0	VCCSEL1
VCC = 1,8V	X	1
VCC = 3V	1	0
VCC = 5V	0	0

### 5.2 Card clock frequency

To configure the frequency of the card clock, refer to the dedicated chapter: 3.2 Generation of Smart Card CLK.

### 5.3 Card Protocol

The card protocol, T=0 or T=1, can be chosen by the host using the bit PROT from register CT\_UCR11\_REG.

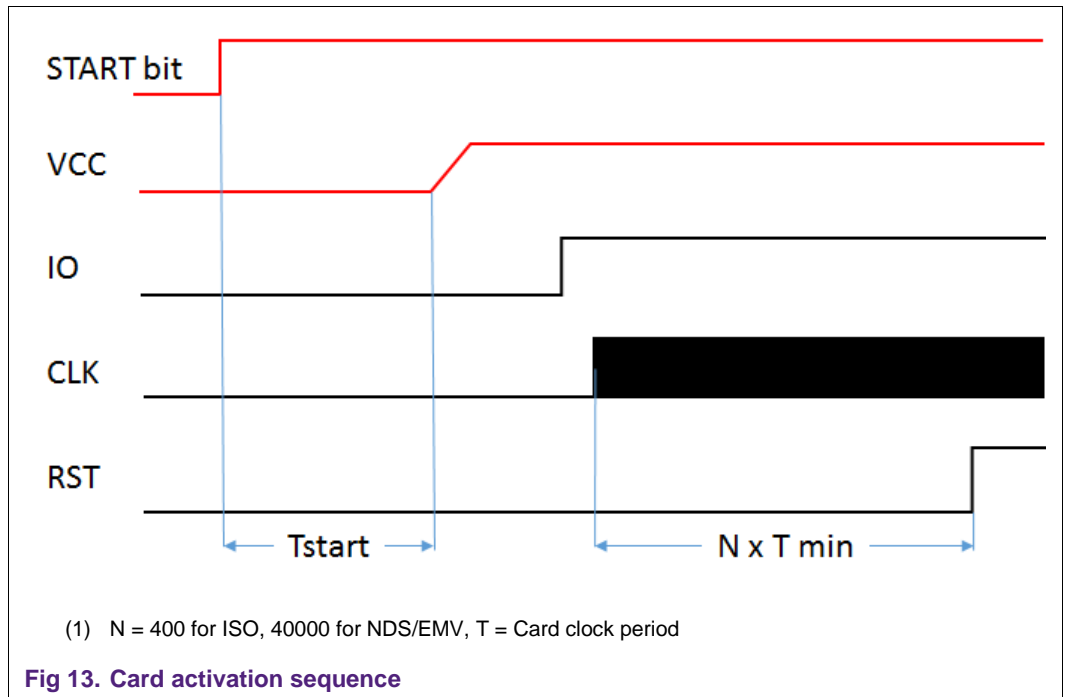


## 6. Card Activation / Deactivation

### 6.1 Activation

#### 6.1.1 Activation Sequence

The card activation is automatically handled by the PN7462AU as soon as it is requested through the bit START in register CT\_PCR\_REG.



The delay Tstart is a PN7462 internal delay: this time is used by the DC/DC to start, and is approximately 20 ms.

In asynchronous mode, this delay is transparent as the application has to wait for the ATR to be received before proceeding to the next operation.

In synchronous mode, this delay has to be respected: IO, CLK and RST must not be changed before VCC has reached its high level. To respect this condition, it is necessary to wait for 20 ms minimum after the bit START has been set to 1, before any operation on the other contact lines.

### 6.1.2 ATR Timings

When the PN7462AU activates a card, it checks the timings for the ATR reception. The timings described in next figure are monitored by the PN7462AU.

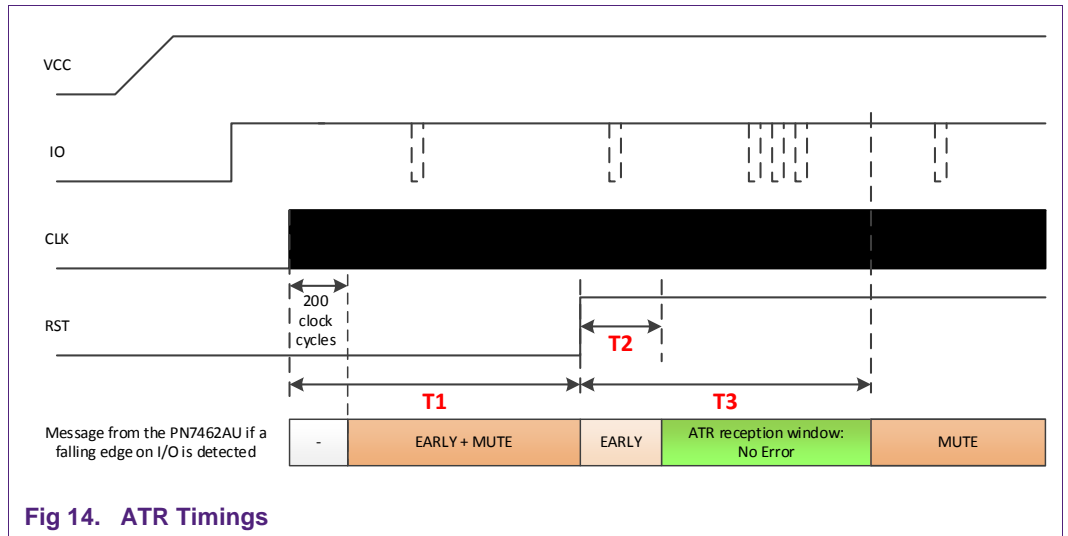


Fig 14. ATR Timings

T1, T2 and T3 timers are configurable through Contact Registers:

T1 is set by the registers CT\_MCLR\_LSB\_REG and CT\_MCLR\_MSB\_REG

T2 is 200 clock cycles plus the value configured through CT\_ECR\_REG

T3 is set through CT\_MCHR\_LSB\_REG and CT\_MCHR\_MSB\_REG

Each value is set in number of clock cycles.

The default value for each counter is set to common value for EMVCo management:

T1 = T3 = 42100 clock cycles.

T2 = 200 + 170 = 370 clock cycles.

### 6.1.3 Mandatory settings

#### 6.1.3.1 VCC Slew Rate

In register CT\_SRR\_REG, it is mandatory to set bits vcc\_rise\_sel1 and vcc\_rise\_sel0 to 1. If any other value is set, the VCC will not load in time which will cause a current overflow.

## 6.2 Deactivation

The deactivation is managed entirely by the PN7462AU sequencer. Deactivation occurs when one of the following events happens:

- Bit START in CT\_PCR\_REG is cleared
- A fault is detected:
  - Card removal
  - Overheating
  - Short-circuit or high current on VCC
  - Power Supply drop (If bit AUTOMATIC\_CT\_DEACT within register PCR\_SYS\_REG is set)
  - High current detected on DCDC or SCLDO

The deactivation sequence is automatic and fully compliant with the standard. For more details on the activation or deactivation sequence and their timings, refer to the PN7462AU data sheet and ISO 7816-3 standard.

## 7. EMVCO Certification

PN7462 can be used as a Contact Smart card reader for Payment application. It is compliant with EMVCo specifications.

Full EMVCo level 1 Digital SW code is available in PSP source code examples. This code allows to run the EMVCo Loopback and go through the Digital and Analog certifications.

### 7.1 EMVCo specific HW implementation

In order to be compliant with EMVCo Analog specification and pass all tests, a 300 ohms resistor is to be added in series with I/O line. See below:

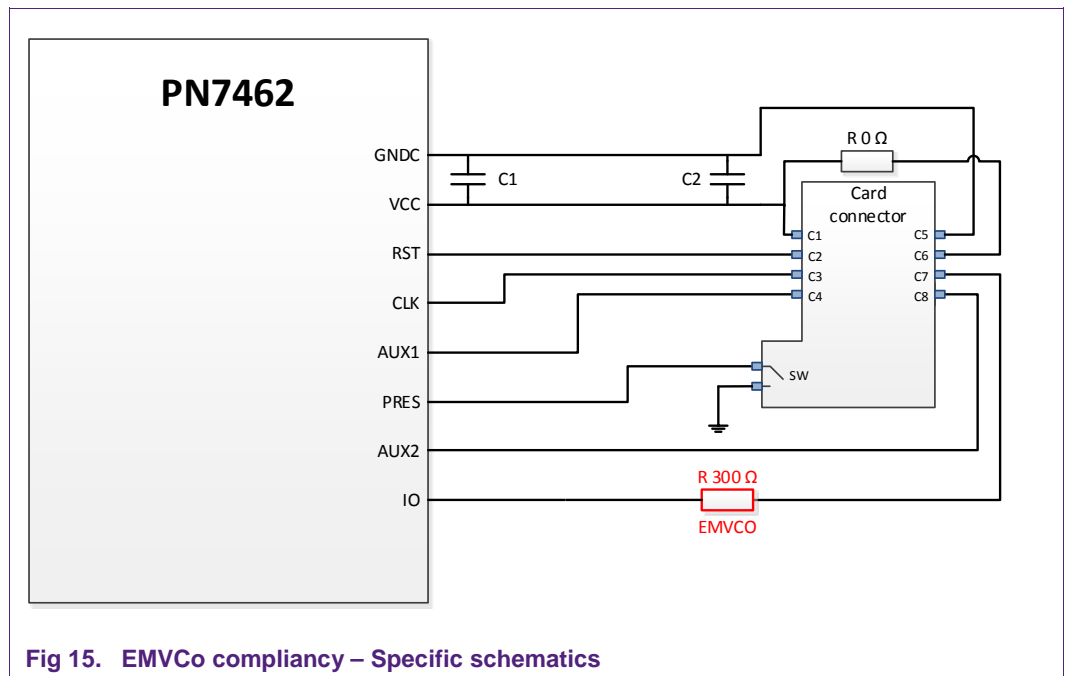


Fig 15. EMVCo compliancy – Specific schematics

The reason to add this Resistor is to be compliant with the IO current limitation specification:

## 8. Electrical design recommendations

### 8.1 Decoupling

To ensure proper behavior of the PN7462AU, some external components have to be used. All supply pins must be protected against noise.

VCC pin (card contact) needs to be connected to two capacitors: twice 220 nF as described in chapter 4.2: one near the PN7462AU chip and one near the card connector. These capacitors type must be low ESR.

VBUSP must be protected by two capacitors: one 100 nF to protect particularly against high frequency noise and one 10  $\mu$ F to absorb slower variations.

### 8.2 Layout

For noise reduction optimization, the layout of the design must adhere to the following guidelines.

#### 8.2.1 Decoupling capacitors

Capacitors are mandatory to protect the supply pins as well as the VCC pin (TDA8035 pin and Card connector pin).

Place decoupling capacitors as close as possible to the pin that they protect.

This means that the capacitor must be physically soldered near the chip or the card connector pin, but also with a short and good connection (low resistance) between the protected pin and its capacitor.

The connection between the capacitor pin and the ground must be short and low resistive as well.

#### 8.2.2 DC/DC capacitors

The capacitors dedicated to the DC/DC converter (decoupling for VBUSP, or pump capacitors on SAP/SAM and VUP), must be physically placed close to their dedicated pin.

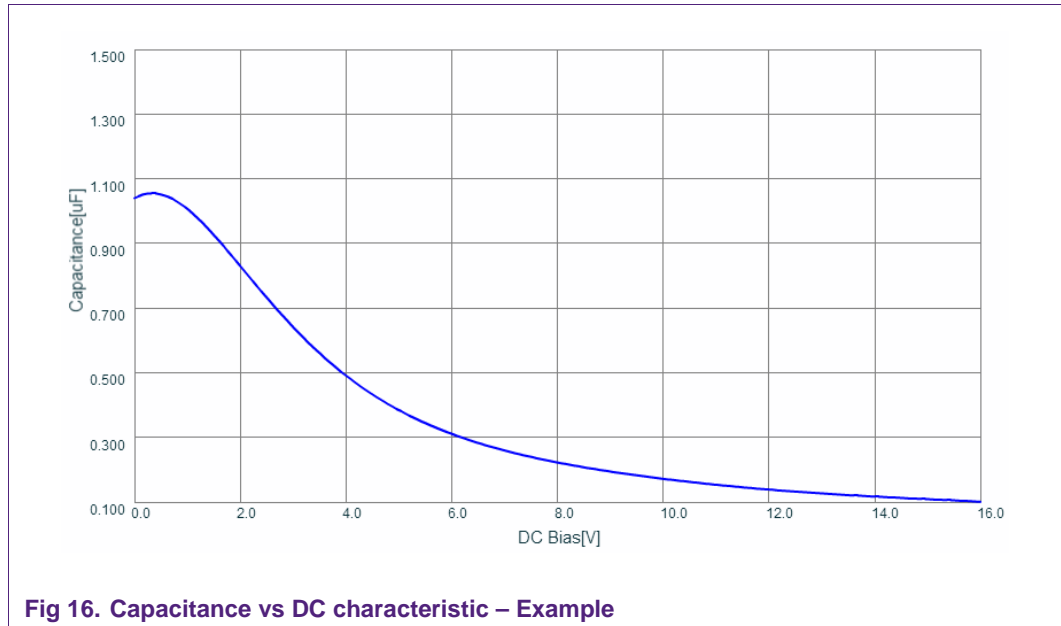
In addition, the capacitors on VBUSP and VUP must have a short and low resistive connection to the GNDP pin, which is the ground pin dedicated to the DC/DC converter.

The nominal capacitance values must follow NXP recommendations: 470 nF between SAP and SAM, and 2.7  $\mu$ F on VUP.

Warning: The nominal capacitor value must be guaranteed at the operating voltage.

Depending on the capacitor quality, the nominal capacitor can drop when the DC voltage on the capacitor increases.

As an example, the following chart shows the behavior of a specific 1 $\mu$ F capacitor with a size 0402 (inch):



**Fig 16. Capacitance vs DC characteristic – Example**

This capacitor has a nominal value of 1µF at 0V, but falls to 300nF at 6V, which is the operating voltage on VUP. Then the behavior of the DC/DC is not the expected one.

In order to grant the correct behavior of the DC/DC it is mandatory to limit the drop on the VUP capacitor to less than 30%.

This behavior (nominal value drop with DC Bias) can be seen with high capacitor values in small packages. It is then recommended to use at least 0603 package for VUP capacitor.

**8.2.3 Clock wires**

Clock (card) or oscillator signals can cause noise on other signals due crosstalk. It is advised to isolate these signals: make the connections as short as possible and keep them far from other signals.

The best is to shield these signals with ground.

**8.2.4 Card ground connection**

Pin GNDC of the PN7462AU is dedicated to the smart card connector. It is advised to connect the C5 (GND) pin of the smart card connector to this pin before connecting it to the main ground.

But it is mandatory to have this pin always connected to the main ground of the board, as well as the card connector ground pin.

**8.2.5 General recommendations**

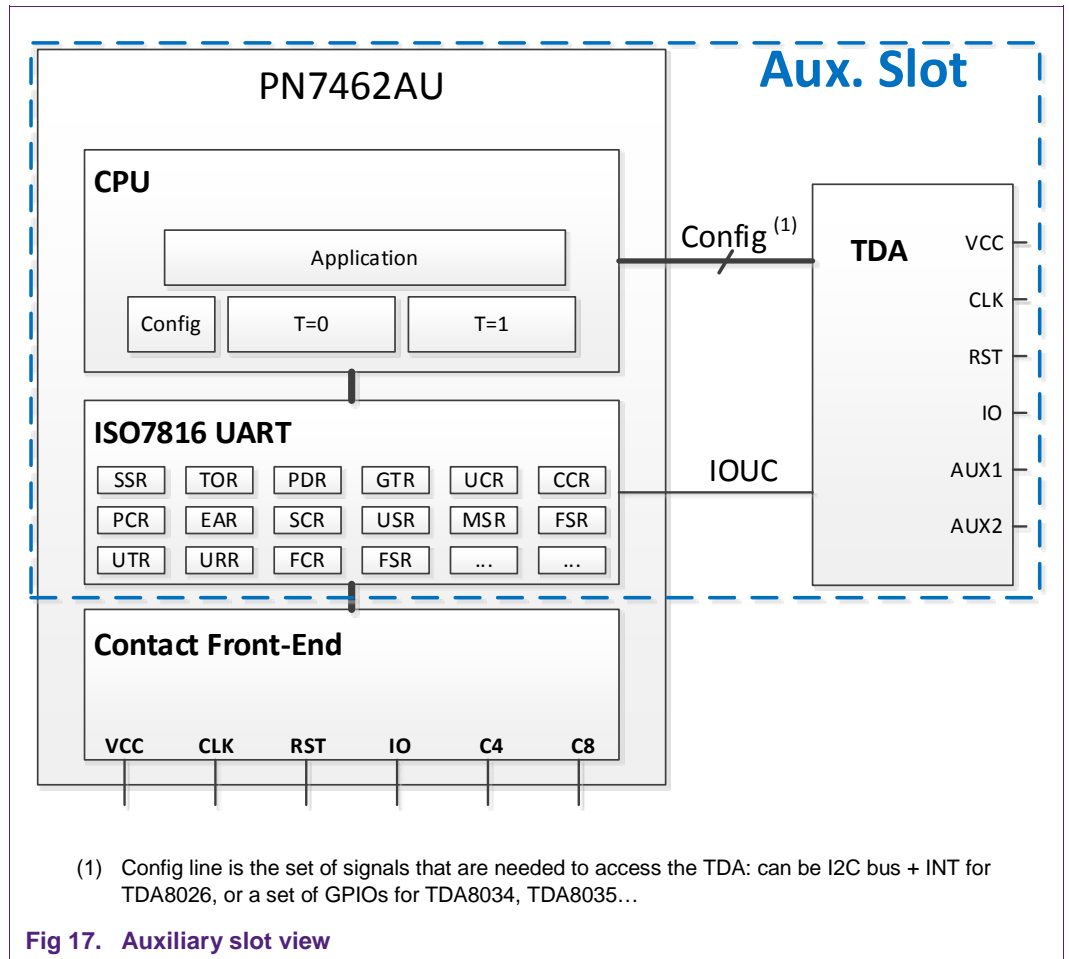
All Contact Smart Card signal lines must be kept far from any RF line, in order to avoid crosstalk on Contact line.

## 9. Auxiliary Slot

### 9.1 Introduction

The PN7462AU is able to manage an auxiliary slot, through an external contact Front-end (typically TDA8035 from NXP).

In this configuration, the CPU and ISO7816 UART from PN7462AU are used, while the electrical management is handled by the external contact front-end.



In ISO7816 UART block within the PN7462AU, the auxiliary slot is generally called slot 2, while the main slot is called slot 1.

## 9.2 Operation with Auxiliary slot

### 9.2.1 Switching

Auxiliary slot is supposed to be used when 2 or more cards must be accessed in the system. In the case only one card is necessary, only slot 1 is required.

The ISO7816 UART is built to be able to support 2 cards activated at the same time. However, data have to be exchanged sequentially: data exchange with one slot (transmission + reception), then with the other slot.

In order to be able to control 2 slots at the same time, some registers of the ISO UART are duplicated: one for slot 1, and one for slot 2. These registers are:

- CT\_PDRx\_LSB\_REG
- CT\_PDRx\_MSB\_REG
- CT\_GTRx\_REG
- CT\_UCR1x\_REG
- CT\_UCR2x\_REG
- CT\_CCRx\_REG

Where 'x' represents the slot number: 1 or 2.

Some registers share the same address, then when accessing the address, the actual register accessed will depend on the slot which is currently selected.

The selection between Slot 1 and Slot 2 is done thanks to the bit IOAUXen from register CT\_SSR\_REG. Set to 1 it selects slot 2.

When the CPU switches the slot number from 1 to 2 or from 2 to 1, i.e. changing the IOAUXen bit, the ISO UART block is reset. This allows to clear the status when switching to another slot.

At the same time, the FIFO output/input is switched between I/O line of main slot to IOAux line connected to the auxiliary slot. Due to this, anything which is received on an IO line not selected will be lost.

For this reason, it is recommended to avoid switching slots between transmission and reception on one slot. The switch must happen after reception is over so that it is known that nothing will be received on IO line.

### 9.2.2 Card activation

There is no PCR register for slot 2. The reason is that the card activation/deactivation is handled by the external front-end.

To control card activation on slot 2, it is required to refer to the dedicated front-end documentation, which has to be controlled directly from the CPU, through GPIOs and/or I2C master block.



## 10. Legal information

### 10.1 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

### 10.2 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Evaluation products** — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out of the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US\$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

### 10.3 Licenses

#### Purchase of NXP ICs with NFC technology

Purchase of an NXP Semiconductors IC that complies with one of the Near Field Communication (NFC) standards ISO/IEC 18092 and ISO/IEC 21481 does not convey an implied license under any patent right infringed by implementation of any of those standards. Purchase of NXP Semiconductors IC does not include a license to any NXP patent (or other IP right) covering combinations of those products with other products, whether hardware or software.

#### Purchase of NXP ICs with ISO/IEC 14443 type B functionality



This NXP Semiconductors IC is ISO/IEC 14443 Type B software enabled and is licensed under Innovatron's Contactless Card patents license for ISO/IEC 14443 B.

The license includes the right to use the IC in systems and/or end-user equipment.

#### RATP/Innovatron Technology

### 10.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

**PC-bus** — logo is a trademark of NXP B.V.

**MIFARE** — is a trademark of NXP B.V.

**ICODE and ICODE** — is a trademark of NXP B.V.

## 11. List of figures

---

Fig 1.	Simplified interfacing view.....	3
Fig 2.	PN7462AU - ISO7816 block diagram .....	4
Fig 3.	Block task during data exchange .....	5
Fig 4.	Default Power supply for Contact Interface.....	7
Fig 5.	ETU representation .....	9
Fig 6.	Clock and ETU size generation.....	10
Fig 7.	Normally open card connector connection 1 ...	12
Fig 8.	Normally open card connector connection 2 ...	12
Fig 9.	Normally closed card connector connection 1.	13
Fig 10.	Normally closed card connector connection 2.	13
Fig 11.	Debouncing feature.....	14
Fig 12.	Card connector schematics.....	15
Fig 13.	Card activation sequence.....	17
Fig 14.	ATR Timings .....	18
Fig 15.	EMVCo compliancy – Specific schematics .....	20
Fig 16.	Capacitance vs DC characteristic – Example .	22
Fig 17.	Auxiliary slot view.....	23

12. List of tables

---

Table 1. Select voltage pin behavior ..... 16

## 13. Contents

<b>1. Introduction</b> .....	<b>3</b>	6.1.3.1 VCC Slew Rate .....	18
1.1 Presentation .....	3	6.2 Deactivation .....	19
1.2 ISO7816 Management .....	4	<b>7. EMVCO Certification</b> .....	<b>20</b>
<b>2. Power supply</b> .....	<b>6</b>	7.1 EMVCo specific HW implementation .....	20
2.1 Power supply pins .....	6	<b>8. Electrical design recommendations</b> .....	<b>21</b>
2.2 DC/DC Converter .....	6	8.1 Decoupling .....	21
2.2.1 Schematics .....	7	8.2 Layout .....	21
2.2.2 Layout .....	7	8.2.1 Decoupling capacitors .....	21
<b>3. Contact Clock</b> .....	<b>8</b>	8.2.2 DC/DC capacitors .....	21
3.1 Clock selection for contact interface .....	8	8.2.3 Clock wires .....	22
3.2 Generation of Smart Card CLK .....	8	8.2.4 Card ground connection .....	22
3.3 ETU management .....	9	8.2.5 General recommendations .....	22
3.3.1 ETU definition .....	9	<b>9. Auxiliary Slot</b> .....	<b>23</b>
3.3.2 ETU size configuration .....	9	9.1 Introduction .....	23
<b>4. Card connector</b> .....	<b>11</b>	9.2 Operation with Auxiliary slot .....	24
4.1 Presence pin .....	11	9.2.1 Switching .....	24
4.1.1 Normally open presence switch .....	12	9.2.2 Card activation .....	24
4.1.1.1 Normally open configuration 1 .....	12	<b>10. Legal information</b> .....	<b>25</b>
4.1.1.2 Normally open configuration 2 (recommended configuration) .....	12	10.1 Definitions .....	25
4.1.2 Normally closed presence switch .....	13	10.2 Disclaimers .....	25
4.1.2.1 Normally closed configuration 1 .....	13	10.3 Licenses .....	25
4.1.2.2 Normally closed configuration 2 (recommended configuration) .....	13	10.4 Trademarks .....	25
4.1.3 Debouncing .....	14	<b>11. List of figures</b> .....	<b>26</b>
4.2 Schematics .....	15	<b>12. List of tables</b> .....	<b>27</b>
<b>5. Card configuration</b> .....	<b>16</b>	<b>13. Contents</b> .....	<b>28</b>
5.1 Card voltage .....	16		
5.2 Card clock frequency .....	16		
5.3 Card Protocol .....	16		
<b>6. Card Activation / Deactivation</b> .....	<b>17</b>		
6.1 Activation .....	17		
6.1.1 Activation Sequence .....	17		
6.1.2 ATR Timings .....	18		
6.1.3 Mandatory settings .....	18		

Please be aware that important notices concerning this document and the product(s) described herein, have been included in the section 'Legal information'.