AN11761

Flip chip

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Document information

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Abstract	This application note provides guidelines for the use of flip chips using plated solder bumps with bump pitches of 200 μm and larger.

Revision history

Rev	Date	Description
3	20161003	added additional remark in Section 2
2	20160510	replaced “bump pitch of 220 μm” by “bump pitch of 200 μm” throughout the document
1	20151207	initial version

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1. Introduction

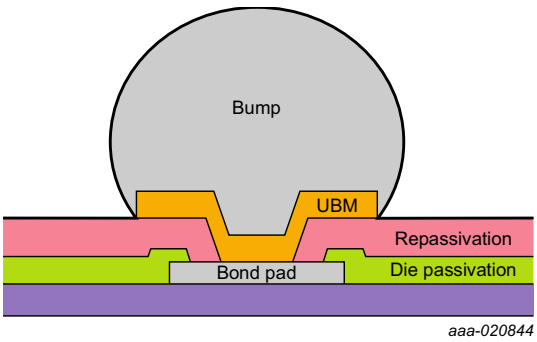
This application note provides guidelines for the use of flip chips with plated solder bumps with bump pitch of 200 μm or larger.

2. Package description

As with wafer level chip scale packages, flip chips offer the smallest package size possible with package size equal to die size. Solder bumps provide the interconnect means to the outside world. The difference between Wafer Level Chip Scale Packages (WLCSP) and flip chips is the application area. Whereas WLCSPs are mounted on a standard Printed-Circuit Board (PCB), flip chips are only used on high definition substrates, typically for interposers in modules and packages. Therefore, the bump diameter of flip chip bumps is smaller than that of WLCSP bumps. Also bump pitch can be smaller. Application notes for WLCSP are given in *AN10439* Ref. 1. The interposer is the substrate that is used within a package or module.

To guarantee that board level reliability requirements are met, flip chips might require application specific measures. Please note flip chips are also referred to as WLCSPs by some end customers.

In the case of flip chips, the Input/Outputs (IO)s on the die are designed such that they are already at the bump position. An Under Bump Metallization (UBM) provides adhesion, acts as barrier layer and ensures solder wetting. A repassivation layer is added to provide improved board level reliability behavior and to decouple the Under Bump Metallization (UBM) and bump from the die passivation. This prevents cracking of the die passivation during temperature cycling. Figure 1 shows the construction.



Repassivation

Fig 1. Flip chip bumping construction

Table 1. Flip chip plated solder bump dimensions

Solder bump height	Solder bump diameter	Bump pitch	Solder bump composition	Si thickness
100 μm ± 15 μm	125 μm ± 15 μm	minimum 240 μm	SnAg1.8	280 μm ± 25 μm
80 μm ± 11 μm	100 μm ± 14 μm	minimum 200 μm	SnAg1.8	200 μm ± 25 μm
70 μm ± 11 μm	95 μm ± 14 μm	minimum 200 μm	SnAg1.8	200 μm ± 25 μm

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3. Interposer design and considerations

A good interposer design ensures high electrical reliability performance when using a flip chip. This applies not only to the footprint design, but also to the location of the flip chip product on the board.

3.1 Footprint layout

Figure 2 shows the commonly used Solder Mask Defined (SMD) solder pad for flip chip. SMD solder pads are used to avoid solder flow out on the part of the tracks. The recommended interposer solder pad dimensions are given in Table 2. Non-Solder Mask Defined (NSMD) solder pads are only used for 400 μm pitch.

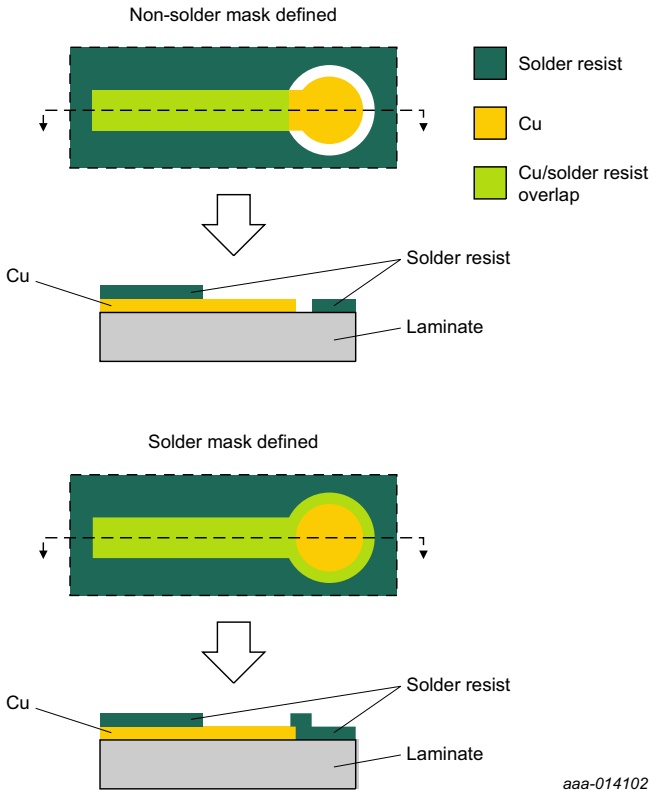

Fig 2. Recommended flip chip solder pads

Table 2. Interposer solder pad dimensions

Bump pitch (μm)	Pad type	Cu pad shape	Cu solder pad (μm)	Solder resist opening shape	Solder resist (μm)
≥ 400	NSMD	circular	130 ± 15	circular	170 ± 15
400 ≥ pitch ≥ 350	SMD	circular	170 ± 15[1]	circular	130 ± 15
350 ≥ pitch ≥ 220	SMD	circular	170 ± 15	circular	110 ± 15
220 ≥ pitch ≥ 200	SMD	circular	140 ± 15	circular	90 ± 10

[1] 200 μm allowed in the case of micro-vias.

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It is recommended that the whole internal area of the pad be flat. This means that the use of vias under the bumps should be avoided wherever possible, as non-flat surfaces can create voids in the solder joint and affect the reliability. If via-in-pad structures (micro-via) are employed, filled micro-vias are preferred. The connection of single pads directly to large areas of solid metal (e.g. ground planes), should be avoided as this could potentially cause an unbalanced thermal profile.

For NSMD pads, the maximum advisable trace width is 75 μm. Reducing copper (Cu) thickness of the top layer of the PCB is recommended to improve tolerances.

3.2 Interposer surface finish

For internal qualification, Cu-pad finishes on the board used are Cu-OSP (Organic Surface Preservatives (OSP)) and NiAu (Electroless Nickel Immersion Gold (ENIG)). These finishes ensure good reliability of the flip chip product.

3.3 Clearances/location

For a typical advanced interposer used in modules, clearance around the maximum size of the component should be considered. This clearance is to ensure pick and placement accuracy of the flip chip component, as well as taking into account the surrounding components.

When underfill is applied, room should be available for dispensing. As with all other surface-mounted components, the placing of flip chip products near mounting holes, connectors, clamps etc. is not recommended. It is not recommended because of the increased amount of bending stress on the bumps. There is also the chance of hitting the product during assembly or during use of the end product. Usually during module/package assembly, multiple interposers are part of a larger panel. The separation of this panel in single interposers can result in mechanical stress to components that are mounted near the separation lanes. The amount of clearance from the separation lane depends on the separation process.

4. Assembly

4.1 Stencil printing of solder paste

Table 3 gives an overview of the recommended stencil dimensions for flip chips. For bump pitches below 220 μm advise is to use flux dipping or dispensing instead of solder paste printing.

Table 3. Recommended stencil dimensions

Bump pitch (μm)	**Stencil**		
	Thickness (μm)	**Shape**	**Opening (μm)**
≥ 350	60	circular	140
≥ 350 ≥ 220	60	circular	130

An electroformed stencil can be used. Before using the stencil, the dimensional accuracy should be checked.

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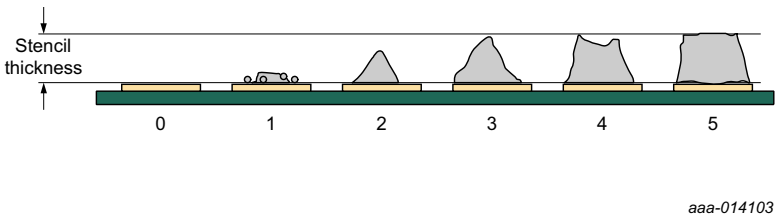
Guideline for stencil opening dimensions:

- Top (print) side: design value +0/−20 μm
- Substrate side: design value ±12 μm

It is advised that a lead-free SAC solder paste is used. Type 5 solder particles or smaller should be used for best print definition. Storage and use conditions as specified by the solder paste supplier should be followed. A solder ball test can be used to verify the reflow properties of the solder paste (IPC-TM-650, Solder Ball Test; see Ref. 2). Before applying the paste on the stencil, it should be allowed to reach room temperature and be thoroughly mixed.

Adjust print speed and pressure so that the stencil is wiped clean of paste, and the solder paste rolls smoothly in front of the squeegee. If needed, the bottom side of the stencil can be cleaned regularly to avoid smearing. Criteria for print definition and smearing are given in Figure 3 and Figure 4.

The print result depends on the rheology of the solder paste, the dimensions of the stencil opening, the print parameters and the solder land definition on the interposer. A larger aperture gives a better definition, but worse smearing.



(0) No solder paste
(1) Irregular shape (few balls)
(2) Pyramid, lower than stencil thickness
(3) Pyramid, height equal to stencil thickness
(4) Beginning flat top with ‘dog ears’
(5) Flat top side
3, 4 and 5 are acceptable rankings

Fig 3. Ranking for definition of solder paste deposits

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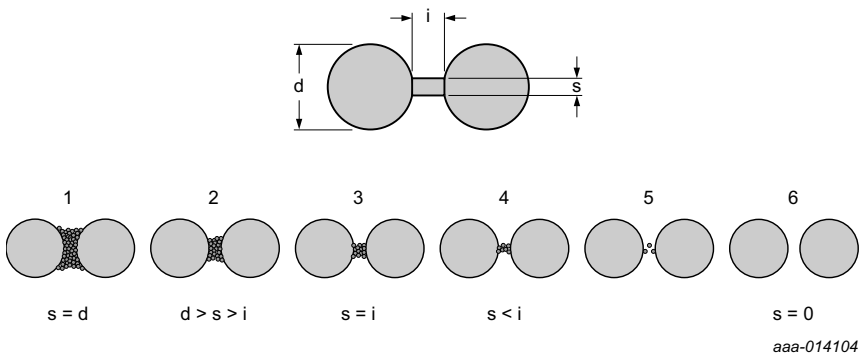

5 and 6 are acceptable rankings

Fig 4. Ranking for definition of solder paste deposits

Alternatively, solder paste printing can be replaced by flux dipping, dispensing or printing. The flux should provide sufficient tackiness to keep the flip chip in place during reflow. Flux is either applied onto the interposer (dispensing, printing), or the flip chip (dipping). The rheology of the flux is optimized for the particular application method. Flux can be applied onto the complete flip chip area or in individual dots per bump. Flux dipping, dispensing, or printing should preferably not be used in combination with NSMD pads.

The maximum advised component displacement is 30 % of metal pad diameter. As an alignment method, use local fiducials and a vision system that uses the bumps for alignment instead of the component outline.

4.2 Reflow

A general reflow profile consists of four steps (see Figure 5):

1. Heating zone: fast heating to reach a certain minimum temperature across the whole board
2. Equalization zone: equalization of the temperatures across the board up to a certain temperature range to avoid large temperature differences in the reflow zone; depending on the component mix
3. Reflow zone: zone in which the actual soldering is done
4. Cooling zone: ramp down zone

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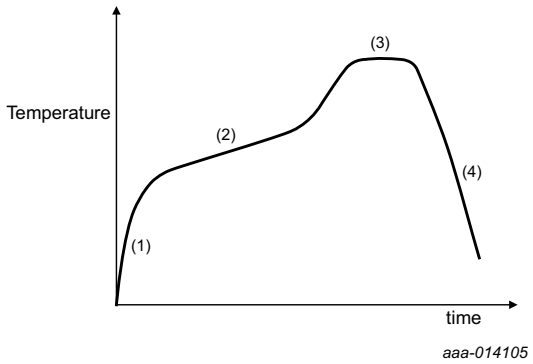

Fig 5. Zones in reflow profile

Follow the recommendations of the solder paste or flux supplier on the optimum shape of the reflow curve, taking into account the mix of components on the board. At the same time, the profile should not be more stringent than the JEDEC profile requirements for MSL assessment (see Ref. 3). For good wetting, typical minimum temperature in the peak zone is 235 °C for SAC or SnAg1.8 solder.

Proper board support during all steps of the reflow profile is essential to avoid board sagging resulting in stress on the soldered joints.

4.3 Underfilling

Underfill improves the board level reliability behavior, however, it might influence electrical performance of the product. A careful assessment is therefore advised. The type to be used depends on the application, and the advice from the underfill supplier should be followed. The larger flip chips, especially, need underfill to meet portable board level reliability requirements.

When selecting an underfill, aspects to be considered:

- The solder flow behavior
- The adhesion to the particular solder mask used on the interposer and to the die surface, voiding behavior
- The adhesion to the die surface, voiding behavior
- The potential impact on (biased) humidity reliability performance

Ultimately board level reliability results determine which is the best underfill to use. The underfill storage and use conditions as defined by the supplier should be followed.

For underfill curing, the recommendations of the underfill vendor should be followed.

The underfill should fill the complete gap between the flip chip WLCSP and the board. No underfill is allowed on the top of the die. In general, there should be no voids, although an occasional void is allowed, but should not be in contact with a bump.

As an alternative, Molded UnderFill (MUF) can be used. The same remarks are valid. In that case MUF covers the top of the die.

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5. Rework process

For rework, use a BGA rework system. Manual handling of flip chips should be reduced to the absolute minimum. However, if it is necessary, a vacuum pick-up tool should be used. Flip chip removal damages the solder bumps, and therefore removed flip chips cannot be reused. Rework consists of the following steps:

- Device removal
- Site preparation
- Application of solder paste to the site
- Device placement
- Device attachment

Refer to the 'Repair' section in *Application note AN10365* Ref. 4 for information on board cleaning and site preparation.

Underfilled samples can only be reworked when reworkable underfill is used. Molded samples cannot be reworked.

6. Returning flip chips to NXP

If flip chips are sent to NXP for analysis, the whole module or package should be returned.

Removing the flip chips from the interposer damages the solder balls and most probably also the part. If the whole module or package cannot be sent to NXP, cut out a part around the device as large as possible by sawing.

During sawing the interposer, clamps should not be placed on top of the flip chip. Clamping too tightly should be avoided, because it can cause the interposer to warp and damage the device.

If the flip chip has to be removed from the interposer, follow the rework guidelines for device removal.

The best packing medium for shipment of devices on interposers is gel pack. If the interposer is too large for a gel pack, place between two ElectroStatic Discharge (ESD) hard foam materials, securing with tape along all edges. Demounted flip chips are best packed in gel pack. Both flip chips on interposers and demounted flip chips should be packed in ESD-bags and preferably in dry pack for shipping.

7. Reliability

NXP has carried out extensive testing of flip chip packages to provide the optimum manufacturing conditions for assembly and to ensure the necessary quality and reliability over the life time of the product in consumer equipment.

During the qualification, reliability tests are performed on wafer level, standalone device level and on board level to ensure the quality level. Product-related reliability data are included in the product qualification report.

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The board level reliability tests are done to ensure the solder joint reliability. These tests are performed on daisy chain components (similar to related products) and electrical resistance is continuously monitored during the test. The board design and the assembly are in accordance with Section 3 and Section 4.

A board level temperature cycling test is performed according to JEDEC condition G (−40 °C and +125 °C), soak mode 2 and a low ramp rate (lower than 20°C/min for any portion of the cycle); see Ref. 5.

Board level drop tests are performed using 1.0 mm board, and the following test conditions: Peak acceleration: 1500 g ± 10 %, Pulse duration: 1 ms ± 10 %.

The board level reliability test results are provided per product due to specific dependence on dimensions such as array, pitch, etc.

When a flip chip product is a particular design for a specific customer, or application that uses a non-standard mounting technique (e.g. thermos-compression and/or interposer type (e.g. flex foil or ceramic), NXP does not perform board level reliability tests.

8. Moisture sensitivity level

The default Moisture Sensitivity Level (MSL) for flip chips is 1.

9. Storage conditions

The label on the packing specifies the shelf life and floor life conditions.

After expiration date, or when the humidity indicator shows > 10 %, solderability should be checked. See Ref. 7 J-STD-002D, solderability tests for component leads, terminations, lugs, terminals and wires.

Baking is not allowed for flip chips.

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10. References

[1] **AN10439 —** Wafer Level Chip Size Package, Application Note

[2] **IPC-TM-650 —** Solder Ball Test

[3] **J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[4] **AN10365 —** Surface Mount Reflow Soldering, Application Note

[5] **JESD22-A104 —** Temperature Cycling

[6] **J-STD-033 —** Standard for Handling, Packing, Shipping and use of Moisture/Reflow Sensitive Surface Mount Devices

[7] **J-STD-002D —** Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

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