AN12055

Schematic guidelines for the PF1550

Rev. 1.0 — 9 April 2018 Application note

1 Introduction

This application note provides guidelines for schematic entry using the PF1550. For an example bill of materials, refer to the PF1550 datasheet.

NXP analog ICs are manufactured using the SMARTMOS process, a combinational BiCMOS manufacturing flow that integrates precision analog, power functions and dense CMOS logic, together on a single cost-effective die.

2 Pin connection guidelines

This section provides recommended pin connections in Table 1. These guidelines help ensure that the PF1550 functions properly.

Table 1. PF1550 pin connection guidelines

Pin	Name	Function	Recommended connection	Recommended connection when not used
1	WDI	Watchdog input from processor	Connect to WDI signal from i.MX series processor. Pull up via 8 kΩ to 100 kΩ to VDDIO	Connect via 100 kΩ to regulator with output voltage < 3.6 V
2	SDA	I^2C data line	Pull-up to VDDIO	Leave floating
3	SCL	I^2C clock line	Pull-up to VDDIO	Leave floating
4	VDDIO	Supply for I^2C bus	Connect to 1.7 to 3.6 V supply. Bypass with 0.1 µF capacitor to ground	Leave floating
5	VDDOTP	Supply to program OTP fuses	Connect to ground for the fuse loading	N/A
6	PWRON	Power on/off from processor	Connect to PMIC_ON_REQ signal from i.MX series processor. Pull up via 8 to 100 kΩ to VSNVS if required	N/A
7	STANDBY	Standby input signal from processor	Connect to PMIC_STBY_REQ signal from i.MX series processor	Connect to ground
8	ONKEY	ONKEY push button input	Connect to push button and pull up via 8 to 100 kΩ to VBATT	Connect via 100 kΩ to VSYS
9	INTB	Open drain interrupt signal to processor	Pull up via 68 to 100 kΩ to VSNVS or other rail at voltage less than or equal to VDDIO	Leave floating
10	RESETBMCU	Open drain reset output to processor	Pull up via 68 to 100 kΩ to VSNVS or other rail at voltage less than or equal to VDDIO	Leave floating

Pin	Name	Function	Recommended connection	Recommended connection when not used
11	VLDO3IN	LDO3 regulator input	Connect to VSYS and bypass with 1.0 µF capacitor to ground	Connect to regulator with output voltage < 4.5 V
12	VLDO3	LDO3 regulator output	Bypass with 4.7 µF capacitor to ground	Leave floating
13	SW3LX	SW3 switching node	Connect to SW3 inductor	Leave floating
14	SW3IN	Input to SW3 regulator	Connect to VSYS and bypass with 0.1 µF + 4.7 µF capacitors to ground	Connect to VSYS
15	SW3FB	Output voltage feedback for SW3	Connect to SW3 output voltage rail near load	Leave floating
16	SW2FB	Output voltage feedback for SW2	Connect to SW2 output voltage rail near load	Leave floating
17	SW2IN	Input to SW2 regulator	Connect to VSYS and bypass with 0.1 µF + 4.7 µF capacitors to ground	Connect to VSYS
18	SW2LX	SW2 switching node	Connect to SW2 inductor	Leave floating
19	VLDO2	LDO2 regulator output	Bypass with 10 µF capacitor to ground	Leave floating
20	VLDO2IN	LDO2 regulator input	Connect to VSYS and bypass with 1.0 µF capacitor to ground	Connect to regulator with output voltage < 4.5 V
21	VREFDDR	VREFDDR regulator output	Bypass with 1.0 µF capacitor to ground	Leave floating
22	VINREFDDR	VREFDDR regulator input	Ensure there is at least 1.0 µF net capacitance from VINREFDDR to ground	Leave floating
23	VDIG	Digital Core supply	Bypass with 1.0 µF capacitor to ground	N/A
24	VCORE	Analog Core supply	Bypass with 1.0 µF capacitor to ground	N/A
25	SW1LX	SW1 switching node	Connect to SW1 inductor	Leave floating
26	SW1IN	Input to SW1 regulator	Connect to VSYS and bypass with 0.1 µF + 4.7 µF capacitors to ground	Connect to VSYS
27	SW1FB	Output voltage feedback for SW1	Connect to SW1 output voltage rail near load	Leave floating
28	VLDO1IN	LDO1 regulators' input	Connect to VSYS and bypass with 1.0 µF capacitor to ground	Connect to regulator with output voltage < 4.5 V
29	VLDO1	LDO1 regulator output	Bypass with 4.7 µF capacitor to ground	Leave floating
30	VSNVS	VSNVS regulator/switch output	Bypass with 0.47 µF capacitor to ground	Bypass with 0.47 µF capacitor to ground
31	LICELL	Coin cell supply input/ output	Bypass with 0.1 µF capacitor. Connect to optional coin cell.	Bypass with 0.1 µF capacitor to ground
32	THM	Battery thermal sense connection	Connect to battery NTC thermistor	Connect to ground
33	VBATT	Battery input	Connect to positive pole of single-cell Lithium Ion/Lithium Polymer battery and connect to VSYS via a 10 µF capacitor only if EOC current threshold setting is less than 20mA	Leave floating
34	VBATT			

Pin	Name	Function	Recommended connection	Recommended connection when not used
35	VSYS	Main input voltage to PMIC and output of charger	Bypass with 2 x 22 µF/10 V capacitors or a 47 µF/10 V capacitor to ground	N/A
36	VSYS			
37	VBUSIN	Charger input	Connect to a valid 5.0 V charger input, bypass with a 2.2 µF/25 V capacitor to ground	Leave floating
38	INT2P7	INT2P7 regulator output as power to the NTC resistor string	Bypass with 1.0 µF capacitor to ground	Leave floating
39	USBPHY	USBPHY regulator output	Bypass with 1.0 µF capacitor to ground	Leave floating
40	CHGB	Charger LED input connection	Connect LED from VSYS to this pin	Connect to ground
—	EP	Expose pad. Functions as ground return for buck and boost regulators	Ground. Connect this pad to the inner and external ground planes through multiple vias to allow effective thermal dissipation.	N/A

3 References

Table 2. References

Document number and description		URL
PF1550	Data Sheet	nxp.com/docs/en/data-sheet/PF1550.pdf

NXP.com support pages	URL
PF1550 product summary page	nxp.com/PF1550

4 Revision history

Revision history

Rev	Date	Description
1.0	20180409	Initial version

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