NXP Semiconductors
Application Note

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Power consumption and measurement of i.MXRT1050

1. Introduction

This document discusses about the power consumption of i.MXRT1050. Mainly includes the following contents:

- i.MXRT1050 overview
- Run Mode definition and configuration
- Low Power Mode definition and configuration
- How to measure power consumption based on MIMXRT1050 EVK Board
- Power consumption under different power modes

The development environment in this application note is IAR Embedded Workbench. The hardware environment is MIMXRT1050 EVK Board (Rev A2).

Contents

2. Chip overview

2.1. i.MX RT chip overview

The i.MX RT chip is a Cortex-M7 based chip that operates at speed up to 600MHz to provide high CPU performance and best real-time response.

- Cortex-M7 based processor which can operate at speed up to 600MHz.
- 512KB on-chip RAM which can be flexibly configured as TCM or general-purpose on chip RAM.
- Advanced power management module with DCDC and LDO to reduce complexity of external power supply and simplifies power sequencing.
- Various memory interfaces, including SDRAM, Raw NAND FLASH, NOR FLASH, SD/eMMC, Quad SPI.
- A wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors.
- Rich audio & video features, including LCD display, basic 2D graphics, camera interface, SPDIF and I2S audio interface.
- Provide rich peripheral modules, such as SPI, I2C, Can, Ethernet, Flex-Timers, ADC, etc.
- Target at Industrial HMI, Motor Control and Home Appliance areas.

3. Low power overview

3.1. Power supply

Table 1 below shows the power supply rails of i.MXRT1050.

Table 1. External power supply rails

Power Rail	Description
DCDC_IN	Power for DCDC.
SOC_IN	Power for SOC.
VDD_HIGH_IN	Power for Analog.
VDD_SNVS_IN	Power for SNVS and RTC.
USB_OTG1_VBUS **USB_OTG2_VBUS**	Power for USB VBUS.
VDDA_ADC	Power for 12-bit ADC.
VDDA_IN	Power for LDO_2P5 and 1P1.

NVCC_SD0	Power for GPIO in SDIO1 bank (3.3V mode).
	Power for GPIO in SDIO1 bank (1.8V mode).
NVCC_SD1	Power for GPIO in SDIO2 bank (3.3V mode).
	Power for GPIO in SDIO2 bank (1.8V mode).
NVCC_GPIO	IO Power for GPIO in GPIO bank.
NVCC_EMC	IO Power for GPIO in EMC bank.

3.2. Run mode

3.2.1. Run mode definition

Table 2. Run mode definition

Run Mode	Definition
Overdrive Run	• CPU runs at 600MHz, overdrive voltage to 1.25V • Bus frequency at full speed • All the peripheral is enabled and runs at target frequency • All PLLs are enabled
Full Speed Run	• CPU runs at 528MHz, full loading, lower voltage to 1.15V • Bus frequency at full speed • All the peripheral is enabled and runs at target frequency • All PLLs are enabled
Low Speed Run	• CPU runs at 132MHz, lower voltage to 1.15V • Internal bus frequency at half speed • Some PLL are powered down • 20% peripheral are active, others are in low power mode
Low Power Run	• CPU runs at 24MHz, lower voltage to 0.95V • Internal bus frequency at 12MHz • All PLLs are powered down, OSC24M powered down, RCOSC24 enabled • High-speed peripherals are power down

In general, we divide RUN mode into those four modes. The Low Speed Run mode uses bus clock in Full Speed Run mode as core clock and Low Power Run mode uses 24MHz internal OSC as core clock source.

3.2.2. Run mode configuration

Table 3. Run mode configuration

	Overdrive Run	Full Speed Run	Low Speed Run	Low Power Run
CCM LPM Mode	RUN	RUN	RUN	RUN
CPU Core	600 MHz	528 MHz	132 Mhz	24 MHz
L1 Cache	ON	ON	ON	ON
FlexRAM	ON	ON	ON	ON
SOC Voltage	1.25 V	1.15 V	1.15 V	0.95 V
Analog LDO	ON	ON	ON	In Weak Mode
24MHz XTAL OSC	ON	ON	ON	OFF
24MHz RC OSC	OFF	OFF	OFF	ON
System PLL	ON	ON	ON	OFF
All Other PLLs	ON	ON	On as needed	On as needed
Module Clock	ON	ON	On as needed	Peripheral clock off
RTC32K	ON	ON	ON	ON

3.3. Low power mode

3.3.1. Low power mode definition

Table 4. Low power mode definition

Low Power Mode	Definition
System Idle	• CPU can automatically enter this mode when no thread running • All the peripheral can remain active • CPU only enter WFI mode, it will have its state retained so the interrupt response can be very short
Low Power Idle	• Much lower power than System Idle mode, with longer exit time

	• All PLLs are shut off, analog modules running in low power mode • All high-speed peripherals are power gated, low speed peripherals can remain running at low frequency
Suspend	• The most power saving mode with longest exit time • All PLLs are shut off, XTAL are off, all clocks are shut off except 32K clock • All high-speed peripherals are power gated, low speed peripherals are clock gated
SNVS	• All SOC digital logic, analog modules are shut off only except SNVS domain • 32KHz RTC is alive

3.3.2. Low power mode configuration

Table 5. Low power mode configuration

	System Idle	Low Power Idle	Suspend	SNVS
CCM LPM Mode	WAIT	WAIT	STOP	-
ARM Core (PDM7)	WFI	WFI	Power Down	OFF
L1 Cache	ON	ON	Power Down	OFF
FlexRAM (PDRET)	ON	ON	ON	OFF
FlexRAM (PDRAM0)	ON	ON	Power Down	OFF
FlexRAM (PDRAM1)	ON/OFF	ON/OFF	Power Down	OFF
VDD_SOC_IN Voltage	1.15V	0.95V	0.925V	OFF
528 PLL	ON	Power Down	Power Down	OFF
Other PLL	Power Down	Power Down	Power Down	OFF
24MHz XTAL OSC	ON	OFF	OFF	OFF
24MHz RC OSC	OFF	ON	OFF	OFF
LDO2P5	ON	OFF	OFF	OFF
LDO1P1	ON	OFF	OFF	OFF
WEAK2P5	OFF	ON	OFF	OFF
WEAK1P1	OFF	ON	OFF	OFF
Bandgap	ON	OFF	OFF	OFF
Low Power Bandgap	ON	ON	ON	OFF

AHB clock	33MHz	12MHz	OFF	OFF
IPG clock	33MHz	12MHz	OFF	OFF
PER clock	33MHz	12MHz	OFF	OFF
Module Clocks	ON as needed	ON as needed	OFF	OFF
RTC32K	ON	ON	ON	ON

3.3.3. Wake-up source

Table 6. Wake- up source

	System Idle	Low Power Idle	Suspend	SNVS
GPIO wakeup	YES	YES	YES	- YES (1 PIN only)[1]
RTC wakeup	YES	YES	YES	YES
USB remote wakeup	YES	YES	YES	NO
Others wakeup source	YES	YES	ON	NO

1.The only pin that can wakeup the system in SNVS is IOMUXC_SNVS_WAKEUP_GPIO5_IO00.

NOTE

No matter in System Idle, Low Power Idle or Suspend mode, user need to enable the wakeup interrupt in GPC module, or, the wakeup fail.

4. How to measure power consumption on MIMXRT1050 EVK

4.1. i.MXRT1050-EVK (REV A2) board overview

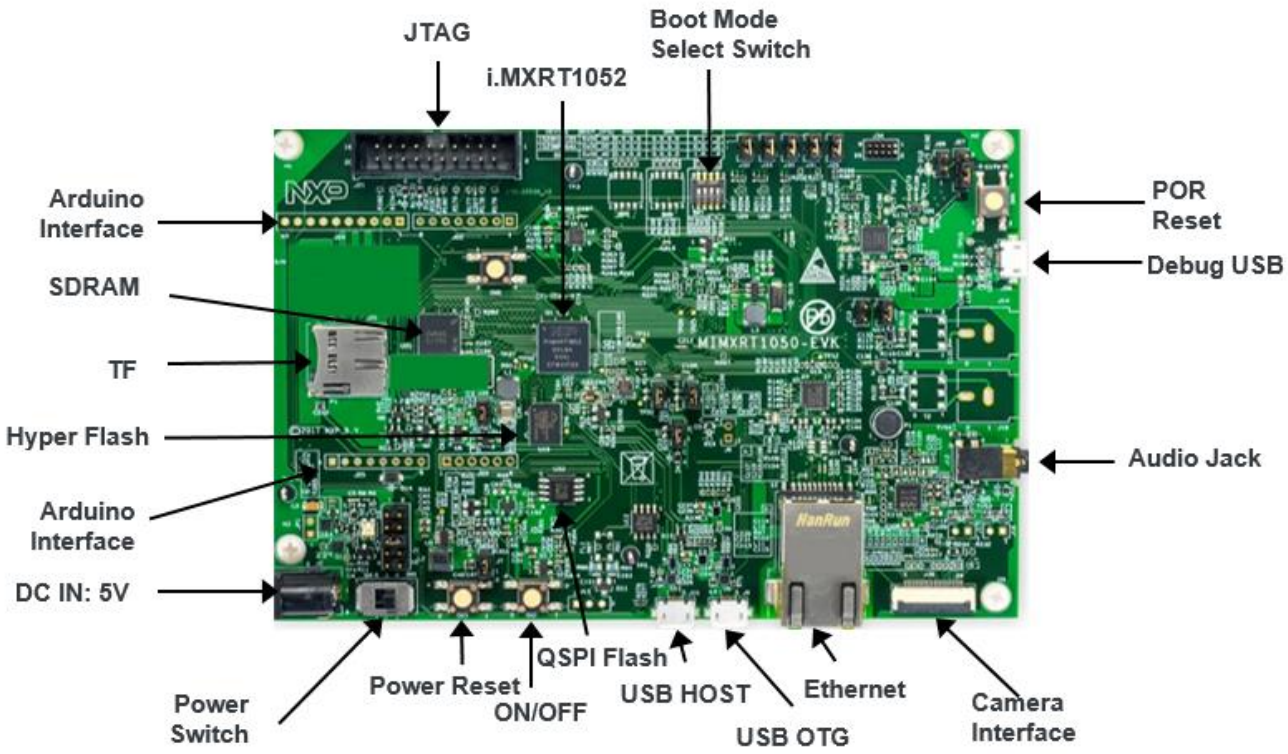

Figure 1. Overview of the MIMXRT1050 EVK Board (Front side)

4.2. Software preparation

1. Install the IAR Workbench 8.11 on your laptop
2. If using IAR Workbench 8.11.2 and lower: Copy the content of the IAR i.MX RT1050 patch into the *IAR Systems\Embedded Workbench 8.0\arm\config* . This will allow you to select the proper device in your IAR project. IAR Workbench 8.11.3 and higher already includes RT1050 patch.
3. Run pre-installed terminal PC application (e.g. Putty)
   Use serial communication configuration:
   - Baud: 115200
   - Data size: 8-bit
   - Stop bit: 1
   - Parity: no

4.3. Download the code into the target memory

The demo prints the power mode menu through the debug console, where the user can set the MCU to a specific power mode. The user can also set the wakeup source by following the debug console prompts. The purpose of this demo is to show how to switch between different power modes, and how to configure a wakeup source and wakeup the MCU from low power modes.

4.3.1. Run IAR based project demo example – Power Mode Switch

1. Open the Demo or simply drag-and-drop it into the opened IAR workbench workspace
   It should appear as:

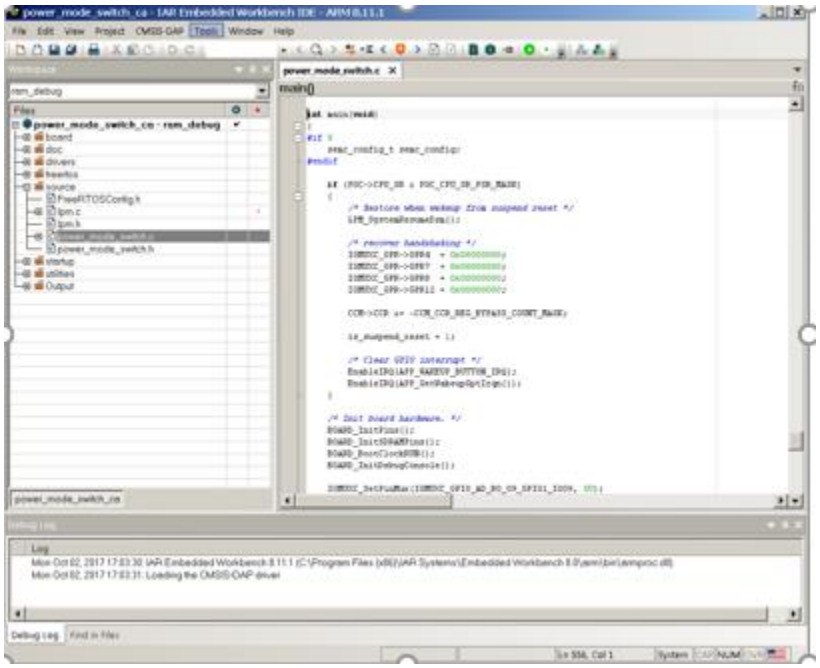

Figure 2. IAR workspace

2. Select the target project configuration from ***Project > Edit configurations…*** and then choose ***debug***.
3. Rebuild All the project (***Project > Rebuild All)***
4. The code will execute from HyperFLASH and data accessed by DTCM. In this case the image cannot be downloaded directly by CMSIS-DAP debugger. We will use OpenSDA to download the image into the HyperFLASH.
5. After build done without error, look for corresponding ***power_mode_switch.bin*** image file.
6. Configure the MIMXRT1050-EVK board into BOOT MODE[1:0] = 00, or 01. It means the serial downloader mode.

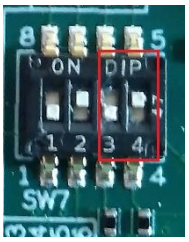

Figure 3. Serial downloader mode

7. Reset the on board iMXRT1050 device by pressing SW3 to get into the serial downloader mode
8. Drag-and-drop (or simply copy) the ***power_mode_switch.bin*** image file into the RT1050-EVK drive
9. Waiting for download done.
10. Configure the MIMXRT1050-EVK board into BOOT_MODE[1:0] = 10. It means the internal boot with boot configuration selected to HyperFLASH 1V8.

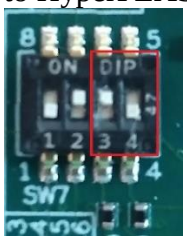

Figure 4. Boot from HyperFlash mode

11. Press SW3 button to reset device and boot from HyperFLASH.
12. In the PC terminal window, the following text message should appear:

```
########## Power Mode Switch Demo (build Oct  2 2017) ###########

    Core Clock = 600000000Hz
    Power mode: Over RUN

******************************************************
CPU:             600000000 Hz
AHB:             600000000 Hz
SEMC:            100000000 Hz
IPG:             150000000 Hz
OSC:             24000000 Hz
RTC:             32768 Hz
ARMPLL:          1200000000 Hz
******************************************************


Select the desired operation

Press  A for enter: Over RUN       - System Over Run mode (600MHz)
Press  B for enter: Full RUN       - System Full Run mode (528MHz)
Press  C for enter: Low Speed RUN  - System Low Speed Run mode (132MHz)
Press  D for enter: Low Power RUN  - System Low Power Run mode (24MHz)
Press  E for enter: System Idle    - System Wait mode
Press  F for enter: Low Power Idle - Low Power Idle mode
Press  G for enter: Suspend        - Suspend mode
Press  H for enter: SNVS           - Shutdown the system

Waiting for power mode select..
```

Figure 5. Terminal window

NOTE

You can take application note How to use i.MXRT1050 Low Power Feature for reference to get more details about this demo.

4.3.2. Current measurements on EVK

In this application note we need to measure the current value of DCDC_IN, SOC_IN(J36), VDD_HIGH_IN (J4) and VDD_SNVS_IN (J5).

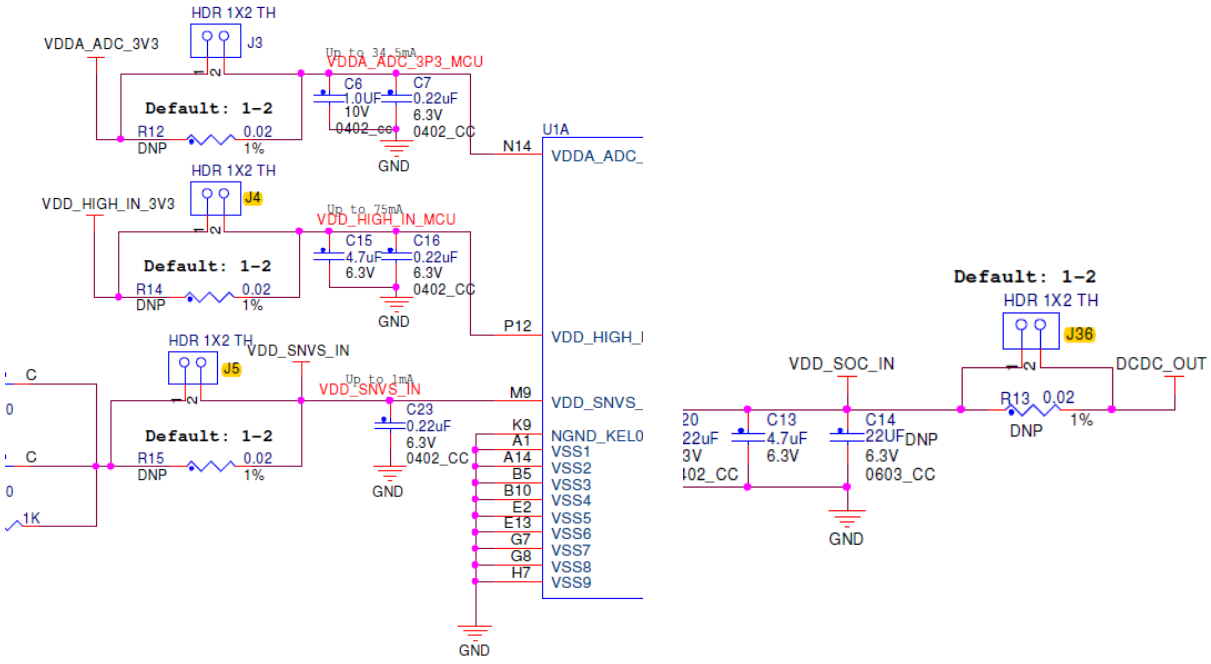

Figure 6. Test Points for SOC_IN, VDD_HIGH_IN and VDD_SNVS_IN

The board reserve the 0ohm resistor for putting the current meter in series, make sure the serial impedance is small, otherwise will impact DCCDC startup. Remove R42 and it will be the test point.

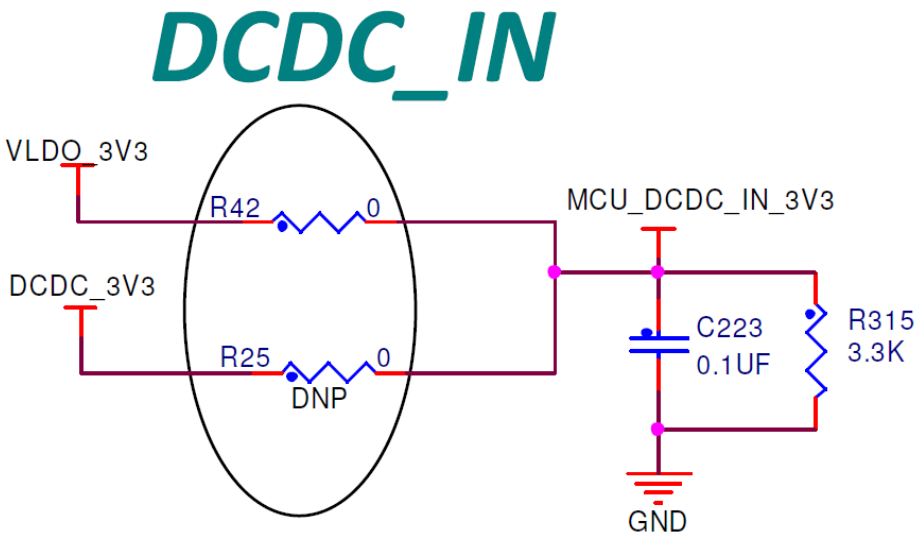

Figure 7. Test point for DCDC_IN

NOTE

For A0 chip, the dead load (R315) help chip restart or fast switching and this is workaround for fast power on/off switching.

For A1 chip, R25 will be mounted, R42 and R315 will be removed.

5. Power consumption results

NOTE

As mentioned above, there is a dead load (R315) so the value of current measured at R42 is greater than the actual value consumed by the chip.

The actual value should be:

$$I_{DCDC\_IN} = I_{R42} - I_{R315}$$

The current results of DCDC_IN at following tables are the actual value.

5.1. Run mode

The power consumption in Table 7 is measured with the coremark benchmark project.

Table 7. Power consumption results

Power Rail	Overdrive (600MHz)			Full Speed Run (528MHz)			Low Speed Run (132MHz)			Low Power Run (24MHz)		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	2.99	75.34	224.88	2.99	56.54	168.76	2.99	13.70	40.89	2.99	2.26	6.74
SOC_IN	1.24	159.00	197.16	1.14	130.00	148.20	1.14	27.00	30.78	0.95	4.36	4.14
VDD_HIGH_IN	3.30	19.80	65.34	3.30	19.23	63.46	3.30	10.02	33.07	3.30	0.31	1.02
VDD_SNVS_IN	2.98	0.00	0.00	2.98	0.00	0.00	2.98	0.00	0.00	2.98	0.00	0.00

- **Overdrive: CPU runs at 600MHz, all peripheral enabled and running at target frequency.**
- **Full Speed Run: CPU runs at 528MHz, all peripheral enabled and running at target frequency.**
- **Low Speed Run: CPU runs at 132MHz, 20% peripheral active.**
- **Low Speed Run: CPU runs at 24MHz, only low speed peripherals active, such as UART/I2C.**
- **All power consumption values are typical silicon at 25C**

5.2. Low power mode

The power consumption in Table 8 is measured with the power mode switch project (The demo project in the attachment).

NOTE

Because discontinuous conduction mode(DCM) can increase the efficiency of DCDC in case of low current loading, it is always recommended.

Table 8. Power consumption results

Power Rail	System Idle			Low Power Idle[1]			Suspend[2]			SNVS[3]		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	2.99	3.17	9.46	2.99	1.44	4.29	2.99	0.14	0.41	0.00	0.00	0.00
SOC_IN	1.15	3.80	4.36	0.95	1.06	1.00	0.93	0.17	0.16	0.00	0.00	0.00
VDD_HIGH_IN	3.30	6.75	22.28	3.30	0.28	0.92	3.30	0.04	0.13	0.00	0.00	0.00
VDD_SNVS_IN	2.98	0.00	0.00	2.89	0.04	0.12	2.84	0.29	0.82	2.90	0.02	0.06

- **All power consumption values are typical silicon at 25C**

NOTE

1.System/Low Power idle: FreeRTOS with System/Low Power IDLE Mode.

2.Suspend: Suspend mode with RAM data in OCRAM/D-TCM (bank0).

3.SNVS: SNVS mode with RTC working. In fact, voltage and current of DCDC_IN can be measured, it caused by Power Supply. Now the DCDC_IN is powered with LDO, which means it shares power supply with VDD_SNVS_IN. More details you can take MIMXRT1050 EVK Board Hardware User's Guide and Hardware Development Guide for the MIMXRT1050 Processor for reference.

NOTE

In order to reduce power consumption, VDD_SNVS_IN will be powered by VDD_HIGH_IN except for Low Power Idle, Suspend and SNVS mode.

5.3. Maximum current use case: camera viewfinder

This use case is a Camera Viewfinder that can record images to an SD card. The use case is based on FreeRTOS. The use case is running on SDRAM as soon as possible. In this use case CSI, PXP, LCD and SD Card are used, it will consume maximum current.

HW configurations:

- Board: EVK A2
- CPU: Overdrive 600MHz
- SDRAM:163.9 MHz
- CSI: YUV, 480x272, 30fps
- PXP: YUV->RGB888
- eLCDIF: 480x272 60Hz

SW working flow:

CSI (YUV) -> PXP (RGB) ->

1) LCD for preview

2) SW JPEG encoding RGB to JPEG and save to SD Card

Those two tasks are running in parallel, and run as faster as it can.

The test result shows in Table 9:

Table 9. Power consumption results

Power Rail	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	2.99	50.134[1]	149.92
SOC_IN	1.24	104[2]	128.96
VDD_HIGH_IN	3.3	14.84	48.97
VDD_SNVS_IN	3.3	0	0

1. Average current for DCDC_IN.
2. Average current for SOC_IN.

6. Conclusion

This document mainly describes how to measure power consumption on i.MX RT based on MIMXRT1050 EVK (Rev A2). For more design details in designing a low power application, you can take the application note How to use iMXRT Low Power Feature for reference.

7. Revision history

Revision number	Date	Substantive changes
0	11/2017	Initial release

8. References

1. i.MX RT 1050 Reference Manual.
2. ARM Cortex M7 Reference Manual.
3. How to use iMXRT Low Power Feature

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