NXP Semiconductors
Application Note

Document Number: AN12245

Power Consumption and Measurement of i.MXRT1060

1 Introduction

This document discusses about the power consumption of i.MXRT10 60 . Mainly includes the following contents:

- i.MXRT1060 overview
- Run mode definition and configuration
- Low-power mode definition and configuration
- How to measure power consumption based on MIMXRT1060 EVK board
- Power consumption under different power modes

The development environment in this application note is IAR Embedded Workbench. The hardware environment is MIMXRT1060 EVK board (Rev A1).

Contents

2 i.MX RT chip overview

The i.MX RT chip is a Cortex-M7 based chip that operates at speed up to 600 MHz to provide high CPU performance and best real-time response.

- Cortex-M7 based processor, which can operate at speed up to 600 MHz.
- 1 MB On-Chip SRAM - up to 512 KB configurable as Tightly Coupled Memory (TCM).
- Advanced power management module with DCDC and LDO to reduce complexity of external power supply and simplifies power sequencing.
- Various memory interfaces, including SDRAM, Raw NAND FLASH, NOR flash, SD/eMMC, Quad SPI.
- A wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors.
- Rich audio & video features, including LCD display, basic 2D graphics, camera interface, S/PDIF, and I2S audio interface.
- Provide rich peripheral modules, such as SPI, I^2C, Can, Ethernet, Flex-Timers, ADC, and so on.
- Target at Industrial HMI, Motor Control, and Home Appliance areas.

3 Low power overview

3.1 Power supply

Table 1. External power supply rails on page 2 below shows the power supply rails of i.MXRT1060.

Table 1. External power supply rails

Power Rail	Description
DCDC_IN	Power for DCDC.
SOC_IN	Power for SOC.
VDD_HIGH_IN	Power for Analog.
VDD_SNVS_IN	Power for SNVS and RTC.
USB_OTG1_VBUS USB_OTG2_VBUS	Power for USB VBUS.
VDDA_ADC	Power for 12-bit ADC.
VDDA_IN	Power for LDO_2P5 and 1P1.
NVCC_SD0	Power for GPIO in SDIO1 bank (3.3 V mode).
	Power for GPIO in SDIO1 bank (1.8 V mode).
NVCC_SD1	Power for GPIO in SDIO2 bank (3.3 V mode).
	Power for GPIO in SDIO2 bank (1.8 V mode).
NVCC_GPIO	IO Power for GPIO in GPIO bank.
NVCC_EMC	IO Power for GPIO in EMC bank.

3.2 Run mode

3.2.1 Run mode definition

Table 2. Run mode definition

Run Mode	Definition
Overdrive Run	• CPU runs at 600 MHz, overdrive voltage to 1.275 V • Bus frequency at full speed • All the peripheral is enabled and runs at target frequency • All PLLs are enabled
Full-Speed Run	• CPU runs at 528 MHz, full loading, lower voltage to 1.15 V • Bus frequency at full speed • All the peripheral is enabled and runs at target frequency • All PLLs are enabled

Table continues on the next page...

Table 2. Run mode definition (continued)

Low-Speed Run	• CPU runs at 132 MHz, lower voltage to 1.15 V • Internal bus frequency at half speed • Some PLL is powered down • 20 % peripheral are active, others are in low-power mode
Low-Power Run	• CPU runs at 24 MHz, lower voltage to 0.95 V • Internal bus frequency at 12 MHz • All PLLs are powered down, OSC24M powered down, RCOSC24 enabled • High-speed peripherals are power down

Run mode can be divided into four modes. The low-speed run mode uses bus clock in full-speed run mode as core clock and low -power run mode uses 24 MHz internal OSC as core clock source.

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3.2.2 Run mode configuration

Table 3. Run mode configuration

	Overdrive Run	**Full Speed Run**	**Low Speed Run**	**Low Power Run**
CCM LPM Mode	RUN	RUN	RUN	RUN
CPU Core	600 MHz	528 MHz	132 MHz	24 MHz
L1 Cache	ON	ON	ON	ON
FlexRAM	ON	ON	ON	ON
SOC Voltage	1.275 V	1.15 V	1.15 V	0.95 V
Analog LDO	ON	ON	ON	In Weak Mode
24 MHz XTAL OSC	ON	ON	ON	OFF
24 MHz RC OSC	OFF	OFF	OFF	ON
System PLL	ON	ON	ON	OFF
All Other PLLs	ON	ON	On as needed	On as needed
Module Clock	ON	ON	On as needed	Peripheral clock off
RTC32K	ON	ON	ON	ON

3.3 Low-power mode

3.3.1 Low-power mode definition

Table 4. Low-power mode definition

Low-Power Mode	Definition
System Idle	• CPU can automatically enter this mode when no thread running • All the peripheral can remain active • CPU only enters WFI mode, it has its state retained so the interrupt response can be very short
Low-Power Idle	• Much lower power than System Idle mode, with longer exit time • All PLLs are shut off, analog modules running in low-power mode • All high-speed peripherals are power gated, low speed peripherals can remain running at low frequency
Suspend	• The most power saving mode with longest exit time • All PLLs are shut off, XTAL are off, all clocks are shut off except 32 K clock • All high-speed peripherals are power gated, low speed peripherals are clock gated
SNVS	• All SOC digital logic, analog modules are shut off only except SNVS domain • 32 KHz RTC is alive

3.3.2 Low power mode configuration

Table 5. Low power mode configuration

	System Idle	Low Power Idle	Suspend	SNVS
CCM LPM Mode	WAIT	WAIT	STOP	-
Arm Core (PDM7)	WFI	WFI	Power Down	OFF
L1 Cache	ON	ON	Power Down	OFF
FlexRAM (PDRET)	ON	ON	ON	OFF
FlexRAM (PDRAM0)	ON	ON	Power Down	OFF
FlexRAM (PDRAM1)	ON/OFF	ON/OFF	Power Down	OFF
VDD_SOC_IN Voltage	1.15 V	0.95 V	0.925 V	OFF
528 PLL	ON	Power Down	Power Down	OFF
Other PLL	Power Down	Power Down	Power Down	OFF
24 MHz XTAL OSC	ON	OFF	OFF	OFF

Table continues on the next page...

Table 5. Low power mode configuration (continued)

24 MHz RC OSC	OFF	ON	OFF	OFF
LDO2P5	ON	OFF	OFF	OFF
LDO1P1	ON	OFF	OFF	OFF
WEAK2P5	OFF	ON	OFF	OFF
WEAK1P1	OFF	ON	OFF	OFF
Bandgap	ON	OFF	OFF	OFF
Low Power Bandgap	ON	ON	ON	OFF
AHB clock	33 MHz	12 MHz	OFF	OFF
IPG clock	33 MHz	12 MHz	OFF	OFF
PER clock	33 MHz	12 MHz	OFF	OFF
Module Clocks	ON as needed	ON as needed	OFF	OFF
RTC32K	ON	ON	ON	ON

3.3.3 Wake-up source

Table 6. Wake-up source

	System Idle	**Low Power Idle**	**Suspend**	**SNVS**
GPIO wakeup	YES	YES	YES	- YES (1 PIN only)[1]
RTC wakeup	YES	YES	YES	YES
USB remote wakeup	YES	YES	YES	NO
Others wakeup source	YES	YES	ON	NO

1. The only pin that can wake-up the system in SNVS is IOMUXC_SNVS_WAKE-UP_GPIO5_IO00.

NOTE

No matter in System Idle, Low-Power Idle or Suspend mode, user need to enable the wake-up interrupt in GPC module, or, the wake-up fails.

4 How to measure power consumption on MIMXRT1060 EVK

4.1 MIMXRT1060-EVK (REV A1) board overview

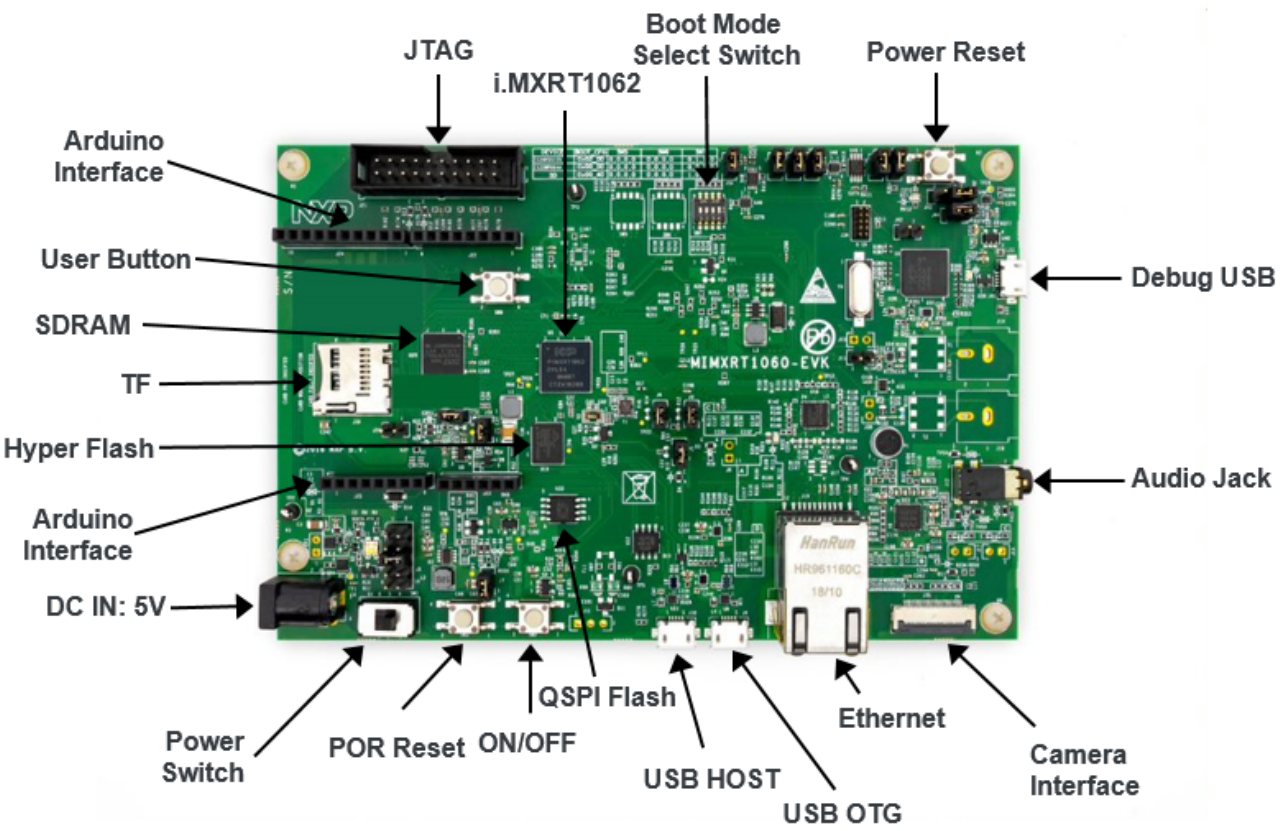

Figure 1. Overview of the MIMXRT1060 EVK board (Front side)

4.1.1 Current measurements on EVK

For this application note, measure the current value of DCDC_IN (J37), VDD_HIGH_IN (J4) and VDD_SNVS_IN (J5).

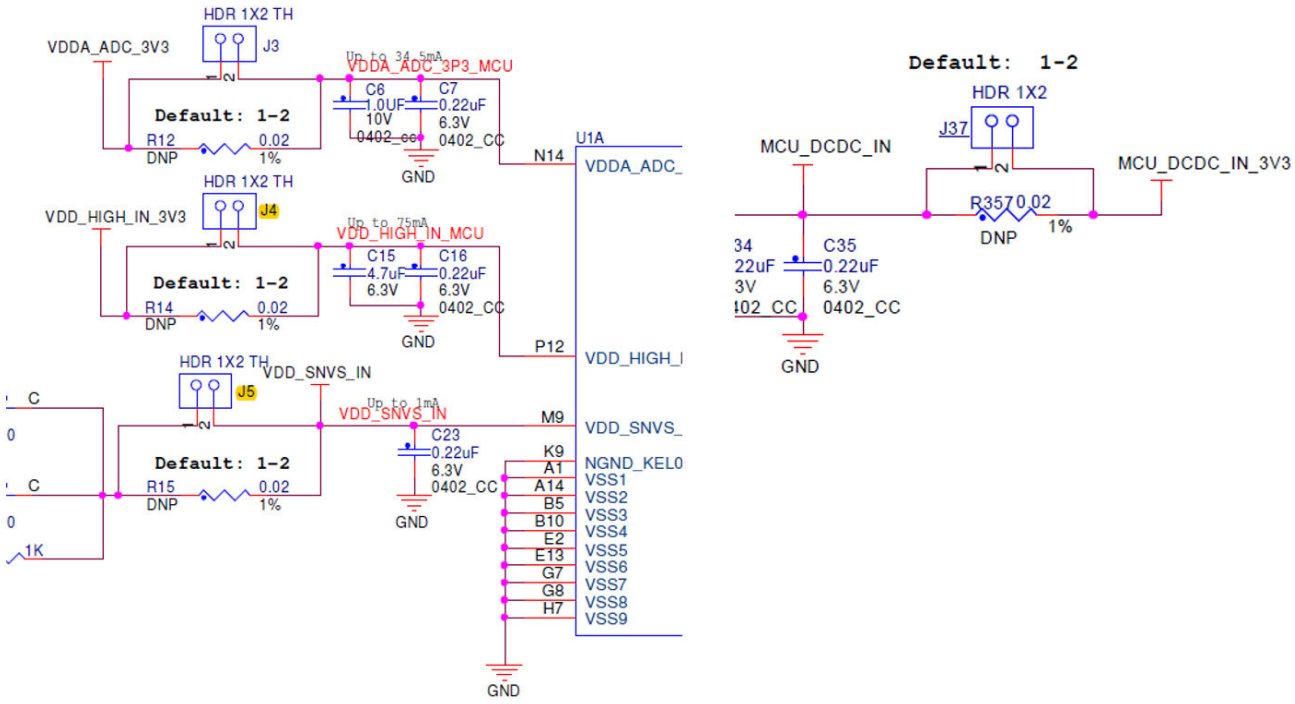

Figure 2. Test Points for DCDC_IN, VDD_HIGH_IN and VDD_SNVS_IN

4.1.2 How to measure the current value under SNVS mode

In SNVS mode, there are changes are required in several settings to measure the accurate current value of SNVS.

Step 1:

Remove resistors: R401, R20. These circuits consume more current.

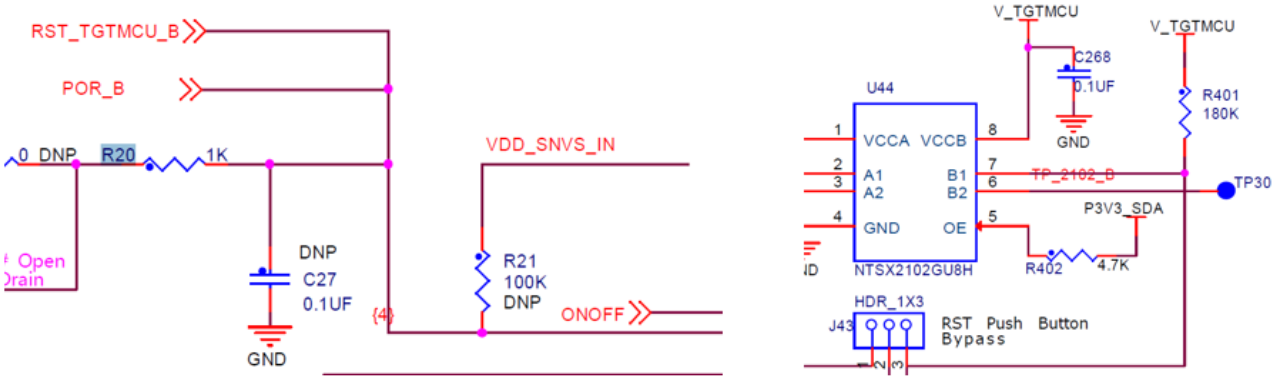

Figure 3. Remove resistors R401 and R20

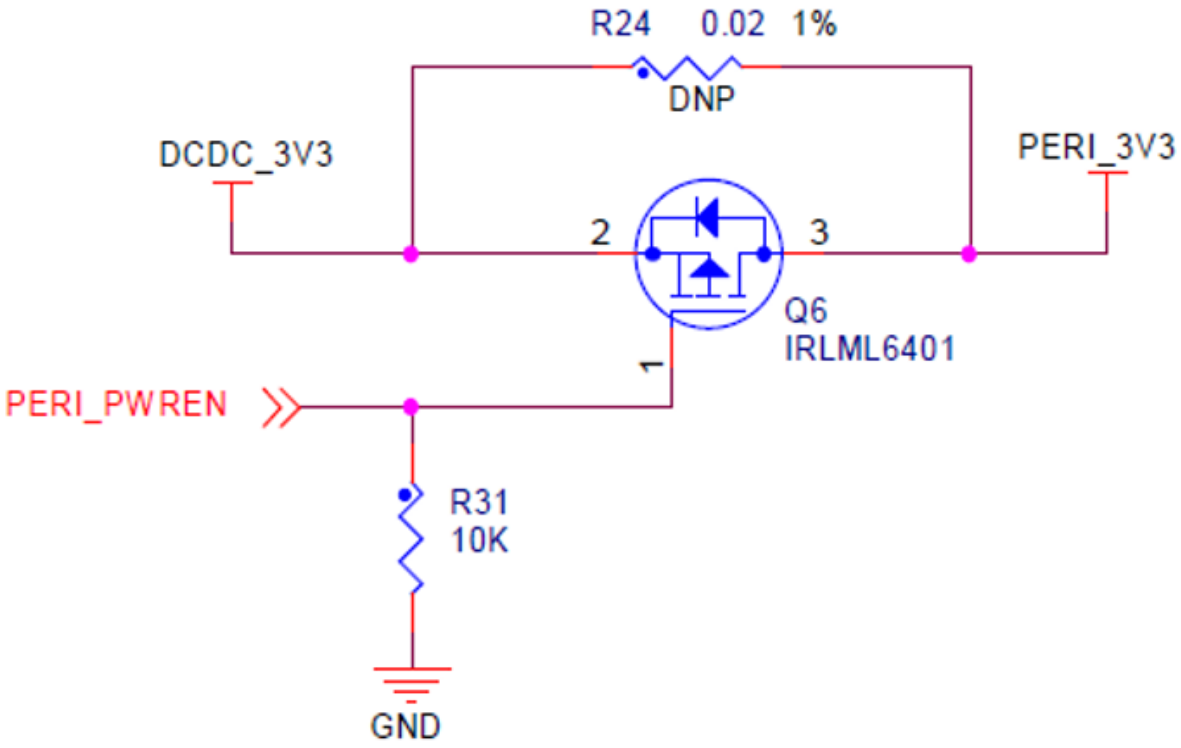

Figure 4. LCD 3V3 power switch circuit

Step 2:

SNVS_PMIC_STBY_REQ_GPIO5_IO02 outputs a high-level signal under Suspend Mode (Stop Mode). On the EVK board, this Pin is used to control LCD Power switch and a resistor R10 is connected to this pin. When the chip is under the Suspend Mode, this resistor consumes more current. To fix this issue, SNVS_PMIC_STBY_REQ is configured as a low-level output GPIO pin.

5 Power consumption results

The power consumption in Table 7. Power consumption results on page 8 is measured with the power mode switch project (The demo project in the attachment).

NOTE

Because discontinuous conduction mode (DCM) can increase the efficiency of DCDC in case of low current loading, it is always recommended.

Table 7. Power consumption results

Power Rail	System Idle			Low Power Idle[1]			Suspend[2]			SNVS[3]		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)

Table continues on the next page...

Table 7. Power consumption results (continued)

DCDC_IN	3.30	3.46	11.42	3.30	1.3 0	4.29	3.30	0.17	0.56	0.00	0.00	0.00
VDD_HIGH_IN	3.30	6.65	21.95	3.30	0.31	1.02	3.30	0.0247	0.08	0.00	0.00	0.00
VDD_SNVS_IN	3.30	0.0238	0.08	3.30	0.041	0.14	3.30	0.016	0.05	3.30	0.0 18	0.06
• All power consumption values are typical silicon at 25 C.												

NOTE

1. **System/Low Power idle:** FreeRTOS with System/Low-power idle mode.
2. **Suspend:** Suspend mode with RAM data in OCRAM/D-TCM (bank0).
3. **SNVS:** SNVS mode with RTC working.

NOTE

In order to reduce power consumption, VDD_SNVS_IN is powered by VDD_HIGH_IN except for Low Power Idle, Suspend, and SNVS mode.

5.1 Run mode

The power consumption in Table 8. Power consumption results on page 9 is measured with the coremark benchmark project.

Table 8. Power consumption results

Power Rail	Overdrive (600 MHz)			Full Speed Run (528 MHz)			Low Speed Run (132 MHz)			Low Power Run (24 MHz)		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	3.30	87.68	289.34	3.30	62.61	206.61	3.30	18.94	62.50	3.30	1.95	6.44
VDD_HIGH_IN	3.30	19.46	64.22	3.30	18.91	62.40	3.30	9.88	32.60	3.30	0.30	0.99
VDD_SNVS_IN	3.30	0.056	0.1 8	3.30	0.052	0.1 7	3.30	0.026	0.0 9	3.30	0.040	0.1 3
• Overdrive: CPU runs at 600 MHz, all peripheral enabled and running at target frequency. • Full Speed Run: CPU runs at 528 MHz, all peripheral enabled and running at target frequency. • Low Speed Run: CPU runs at 132 MHz, 20 % peripheral active. • Low Speed Run: CPU runs at 24 MHz, only low speed peripherals active, such as UART/I^2C. • All power consumption values are typical silicon at 25 C.												

5.2 Low-power mode

The power consumption in Table 9. Power consumption results on page 10 is measured with the power mode switch project (The demo project in the attachment).

NOTE

The discontinuous conduction mode (DCM) increased the efficiency of DCDC if low current is loading, It is always recommended.

Table 9. Power consumption results

Power Rail	System Idle			Low-Power Idle[1]			Suspend[2]			SNVS[3]		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	3.30	3.46	11.42	3.30	1.3 0	4.29	3.30	0.17	0.56	0.00	0.00	0.00
VDD_HIGH_IN	3.30	6.65	21.95	3.30	0.31	1.02	3.30	0.0247	0.08	0.00	0.00	0.00
VDD_SNVS_IN	3.30	0.0238	0.08	3.30	0.041	0.14	3.30	0.016	0.05	3.30	0.0 18	0.06
• All power consumption values are typical silicon at 25 C.												

NOTE

1. **System/Low-Power idle:** FreeRTOS with System/Low-power idle mode.
2. **Suspend:** Suspend mode with RAM data in OCRAM/D-TCM (bank0).
3. **SNVS:** SNVS mode with RTC working.

NOTE

In order to reduce power consumption, VDD_SNVS_IN is powered by VDD_HIGH_IN except for Low-Power Idle, Suspend, and SNVS mode.

6 Conclusion

This document mainly describes how to measure power consumption on i.MX RT based on MIMXRT1060 EVK (Rev. A 1). For more design details in designing a low-power application, see the application note How to use iMXRT Low Power Feature.

7 Revision history

Table 10. Revision history

Revision number	Date	Substantive changes
0	09/2018	Initial release

8 References

1. i.MX RT 1060 Reference Manual
2. ARM Cortex M7 Reference Manual
3. How to use iMXRT Low Power Feature

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