1 Introduction

This document discusses about the power consumption of i.MX RT1060. Mainly includes the following contents:

- i.MX RT1060 overview
- Run mode definition and configuration
- Low-power mode definition and configuration
- How to measure power consumption based on MIMXRT1060 EVK board
- Power consumption under different power modes

The development environment in this application note is IAR Embedded Workbench. Software is based on SDK 2.6.1. The hardware environment is MIMXRT1060 EVK board (Rev A1).

2 i.MX RT chip overview

The i.MX RT chip is a Cortex-M7 based chip that operates at speed up to 600 MHz to provide high CPU performance and best real-time response.

- Cortex-M7 based processor, which can operate at speed up to 600 MHz.
- 1 MB On-Chip SRAM - up to 512 KB configurable as Tightly Coupled Memory (TCM).
- Advanced power management module with DCDC and LDO to reduce complexity of external power supply and simplifies power sequencing.
- Various memory interfaces, including SDRAM, Raw NAND FLASH, NOR flash, SD/eMMC, Quad SPI.
- A wide range of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors.
- Rich audio & video features, including LCD display, basic 2D graphics, camera interface, S/PDIF, and I2S audio interface.
- Provide rich peripheral modules, such as SPI, I²C, Can, Ethernet, Flex-Timers, and ADC.
- Target at Industrial HMI, Motor Control, and Home Appliance areas.

3 Low power overview

3.1 Power supply

Table 1 below shows the power supply rails of i.MX RT1060.
Table 1. External power supply rails

<table>
<thead>
<tr>
<th>Power Rail</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCDC_IN</td>
<td>Power for DCDC.</td>
</tr>
<tr>
<td>SOC_IN</td>
<td>Power for SOC.</td>
</tr>
<tr>
<td>VDD_HIGH_IN</td>
<td>Power for Analog.</td>
</tr>
<tr>
<td>VDD_SNVS_IN</td>
<td>Power for SNVS and RTC.</td>
</tr>
<tr>
<td>USB_OTG1_VBUS</td>
<td>Power for USB VBUS.</td>
</tr>
<tr>
<td>USB_OTG2_VBUS</td>
<td></td>
</tr>
<tr>
<td>VDDA_ADC_3P3</td>
<td>Power for 12-bit ADC.</td>
</tr>
<tr>
<td>NVCC_SD0</td>
<td>Power for GPIO in SDIO1 bank (3.3 V mode).</td>
</tr>
<tr>
<td></td>
<td>Power for GPIO in SDIO1 bank (1.8 V mode).</td>
</tr>
<tr>
<td>NVCC_SD1</td>
<td>Power for GPIO in SDIO2 bank (3.3 V mode).</td>
</tr>
<tr>
<td></td>
<td>Power for GPIO in SDIO2 bank (1.8 V mode).</td>
</tr>
<tr>
<td>NVCC_GPIO</td>
<td>IO Power for GPIO in GPIO bank.</td>
</tr>
<tr>
<td>NVCC_EMC</td>
<td>IO Power for GPIO in EMC bank.</td>
</tr>
</tbody>
</table>

3.2 Run mode

- Run mode definition
- Run mode configuration

3.2.1 Run mode definition

Table 2. Run mode definition

<table>
<thead>
<tr>
<th>Run Mode</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overdrive Run</td>
<td>• CPU runs at 600 MHz, overdrive voltage to 1.275 V</td>
</tr>
<tr>
<td></td>
<td>• Bus frequency at 150 MHz</td>
</tr>
<tr>
<td></td>
<td>• All the peripheral is enabled and runs at target frequency</td>
</tr>
<tr>
<td></td>
<td>• All PLLs are enabled</td>
</tr>
<tr>
<td>Full-Speed Run</td>
<td>• CPU runs at 528 MHz, full loading, lower voltage to 1.15 V</td>
</tr>
<tr>
<td></td>
<td>• Bus frequency at 132 MHz</td>
</tr>
<tr>
<td></td>
<td>• All the peripheral is enabled and runs at target frequency</td>
</tr>
<tr>
<td></td>
<td>• All PLLs are enabled</td>
</tr>
</tbody>
</table>

*Table continues on the next page...*
<table>
<thead>
<tr>
<th>Table 2. Run mode definition (continued)</th>
</tr>
</thead>
</table>
| **Low-Speed Run** | • CPU runs at 132 MHz, lower voltage to 1.15 V  
• Internal bus frequency at 33 MHz  
• All PLL and PFDs are disabled except SYSPLL and SYSPLL/PFD2  
• 20% peripheral are active, others are in low-power mode |
| **Low-Power Run** | • CPU runs at 24 MHz, lower voltage to 0.95 V  
• Internal bus frequency at 12 MHz  
• All PLLs are powered down, OSC24M powered down, RCOSC24 enabled  
• High-speed peripherals are power down |

### 3.2.2 Run mode configuration

<table>
<thead>
<tr>
<th>Table 3. Run mode configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>CCM LPM Mode</strong></td>
</tr>
<tr>
<td>CPU Core</td>
</tr>
<tr>
<td>L1 Cache</td>
</tr>
<tr>
<td>IPG CLK</td>
</tr>
<tr>
<td>PER CLK</td>
</tr>
<tr>
<td>FlexRAM</td>
</tr>
<tr>
<td>SOC Voltage</td>
</tr>
<tr>
<td>Analog LDO</td>
</tr>
<tr>
<td>24 MHz XTAL OSC</td>
</tr>
<tr>
<td>24 MHz RC OSC</td>
</tr>
<tr>
<td>ARM PLL</td>
</tr>
<tr>
<td>SYS PLL</td>
</tr>
<tr>
<td>SYS PFD0</td>
</tr>
<tr>
<td>SYS PFD1</td>
</tr>
<tr>
<td>SYS PFD2</td>
</tr>
<tr>
<td>SYS PFD3</td>
</tr>
<tr>
<td>USB1 PLL</td>
</tr>
<tr>
<td>USB1 PFD0</td>
</tr>
<tr>
<td>USB1 PFD1</td>
</tr>
<tr>
<td>USB1 PFD2</td>
</tr>
<tr>
<td>USB1 PFD3</td>
</tr>
</tbody>
</table>

*Table continues on the next page...*
Table 3. Run mode configuration (continued)

<table>
<thead>
<tr>
<th>CCM LPM Mode</th>
<th>RUN</th>
<th>RUN</th>
<th>RUN</th>
<th>RUN</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB2 PLL</td>
<td>ON</td>
<td>ON</td>
<td>Power Down</td>
<td>Power Down</td>
</tr>
<tr>
<td>Audio PLL</td>
<td>ON</td>
<td>ON</td>
<td>Power Down</td>
<td>Power Down</td>
</tr>
<tr>
<td>Video PLL</td>
<td>ON</td>
<td>ON</td>
<td>Power Down</td>
<td>Power Down</td>
</tr>
<tr>
<td>ENET PLL</td>
<td>ON</td>
<td>ON</td>
<td>Power Down</td>
<td>Power Down</td>
</tr>
<tr>
<td>Module Clock</td>
<td>ON</td>
<td>ON</td>
<td>On as needed</td>
<td>Peripheral clock off</td>
</tr>
<tr>
<td>RTC32K</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
</tbody>
</table>

3.3 Low-power mode

- Low-power mode definition
- Low-power mode configuration
- Wake-up source

3.3.1 Low-power mode definition

Table 4. Low-power mode definition

<table>
<thead>
<tr>
<th>Low-Power Mode</th>
<th>Definition</th>
</tr>
</thead>
</table>
| System Idle    | • CPU can automatically enter this mode when no thread running  
                • All the peripherals can remain active  
                • CPU only enters WFI mode, it has its state retained so the interrupt response can be very short |
| Low-Power Idle | • Much lower power than System Idle mode, with longer exit time  
                • All PLLs are shut off, analog modules running in low-power mode  
                • All high-speed peripherals are power gated, low speed peripherals can remain running at low frequency |
| Suspend        | • The most power-saving mode with longest exit time  
                • All PLLs are shut off, XTAL are off, all clocks are shut off except 32 K clock  
                • All high-speed peripherals are power gated, low speed peripherals are clock gated |
| SNVS           | • All SOC digital logic, analog modules are shut off only except SNVS domain  
                • 32 KHz RTC is alive  
                • VDD_HIGH_IN and VDD_DCDC_IN can be powered off |
### 3.3.2 Low-power mode configuration

Table 5. Low-power mode configuration

<table>
<thead>
<tr>
<th></th>
<th>System Idle</th>
<th>Low-Power Idle</th>
<th>Suspend</th>
<th>SNVS</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCM LPM Mode</td>
<td>WAIT</td>
<td>WAIT</td>
<td>STOP</td>
<td>-</td>
</tr>
<tr>
<td>Arm Core (PDM7)</td>
<td>WFI</td>
<td>WFI</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>L1 Cache</td>
<td>ON</td>
<td>ON</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>FlexRAM (PDRET)</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>FlexRAM (PDRAM0)</td>
<td>ON</td>
<td>ON</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>FlexRAM (PDRAM1)</td>
<td>ON/OFF</td>
<td>ON/OFF</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>VDD_SOC_IN Voltage</td>
<td>1.15 V</td>
<td>0.95 V</td>
<td>0.925 V</td>
<td>OFF</td>
</tr>
<tr>
<td>ARM PLL</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>SYS PLL</td>
<td>ON</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>SYS PFD0</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>SYS PFD1</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>SYS PFD2</td>
<td>ON</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>SYS PFD3</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>USB1 PLL</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>USB1 PFD0</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>USB1 PFD1</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>USB1 PFD2</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>USB1 PFD3</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>USB2 PLL</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>Audio PLL</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>Video PLL</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>ENET PLL</td>
<td>Power Down</td>
<td>Power Down</td>
<td>Power Down</td>
<td>OFF</td>
</tr>
<tr>
<td>24 MHz XTAL OSC</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>24 MHz RC OSC</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>LDO2P5</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>LDO1P1</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>WEAK2P5</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>WEAK1P1</td>
<td>OFF</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>Bandgap</td>
<td>ON</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
<tr>
<td>Low-Power Bandgap</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>OFF</td>
</tr>
<tr>
<td>AHB clock</td>
<td>33 MHz</td>
<td>12 MHz</td>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

*Table continues on the next page...*
Table 5. Low-power mode configuration (continued)

<table>
<thead>
<tr>
<th></th>
<th>IPG clock 33 MHz</th>
<th>IPG clock 12 MHz</th>
<th>PER clock 33 MHz</th>
<th>PER clock 12 MHz</th>
<th>Module Clocks ON as needed</th>
<th>Module Clocks ON as needed</th>
<th>RTC32K ON</th>
<th>RTC32K ON</th>
</tr>
</thead>
</table>

3.3.3 Wake-up source

Table 6. Wake-up source

<table>
<thead>
<tr>
<th></th>
<th>System Idle</th>
<th>Low Power Idle</th>
<th>Suspend</th>
<th>SNVS</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO wake-up</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>- YES (1 PIN only)</td>
</tr>
<tr>
<td>RTC wake-up</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
</tr>
<tr>
<td>USB remote wake-up</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
</tr>
<tr>
<td>Other peripheral wake-up sources</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
</tr>
</tbody>
</table>

**NOTE**

Irrespective of whether the system is in System Idle, Low-Power Idle or Suspend modes, the wake-up interrupt should be enabled in GPC module. The only pin that can wake up the system in SNVS is IOOMUXC_SNVS_WAKEUP_GPIO5_IO00.

**NOTE**

Peripheral wake-up requires that the clock for the peripheral is available in the mode.

4 How to measure power consumption on MIMXRT1060 EVK
4.1 MIMXRT1060-EVK (REV A1) board overview

Figure 1. Overview of the MIMXRT1060 EVK board (Front side)

4.1.1 Current measurements on EVK

For this application note, measure the current value of DCDC_IN (J37), VDD_HIGH_IN (J4), and VDD_SNVS_IN (J5).
4.1.2 Hardware rework for the EVK

Because the POR_B pin has an internal pullup, R401 and R20 should be removed. Leaving these resistors populated causes higher SNVS current than what is shown in this application note.

SNVS_PMIC_STBY_REQ_GPIO5_IO02 outputs a high-level signal under Suspend Mode (Stop Mode). On the EVK board, this pin is used to control LCD Power switch and a resistor R31 is connected to this pin. When the chip is under the Suspend Mode, this resistor consumes more current. To fix this issue, SNVS_PMIC_STBY_REQ is configured as a low-level output GPIO pin.
4.1.3 Run IAR-based project demo example – Power mode switch

1. The project file is at: `boards\evkbimxrt1060\demo_apps\power_mode_switch_bm\iar\power_mode_switch_bm.eww`
2. Download the project.
3. Select the target power mode on the terminal.

5 Power consumption results

**NOTE**

To reduce power consumption, VDD\_SNVS\_IN is powered by VDD\_HIGH\_IN in all power modes except the SNVS mode.

All power consumption values are typical silicon at 25 C.

Discontinuous conduction mode (DCM) increases the efficiency of DCDC in case of low current loading and is always recommended.
5.1 Run mode

Table 7. Run mode on RAM

<table>
<thead>
<tr>
<th>Power Rail</th>
<th>Voltage (V)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCDC_IN</td>
<td>3.3</td>
<td>53.1432</td>
<td>175.3726</td>
<td>38.2423</td>
<td>126.1996</td>
<td>12.9733</td>
<td>42.8119</td>
<td>2.7634</td>
<td>9.1192</td>
</tr>
<tr>
<td>HIGH_IN</td>
<td>3.3</td>
<td>20.4431</td>
<td>67.4622</td>
<td>20.4244</td>
<td>67.4005</td>
<td>5.2617</td>
<td>17.3636</td>
<td>0.2682</td>
<td>0.8851</td>
</tr>
<tr>
<td>SNVS_IN</td>
<td>3.3</td>
<td>0.0250</td>
<td>0.0824</td>
<td>0.0234</td>
<td>0.0771</td>
<td>0.0137</td>
<td>0.0452</td>
<td>0.0173</td>
<td>0.0571</td>
</tr>
</tbody>
</table>

Table 8. Run mode XIP on Flash

<table>
<thead>
<tr>
<th>Power Rail</th>
<th>Voltage (V)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCDC_IN</td>
<td>3.3</td>
<td>44.5526</td>
<td>147.0236</td>
<td>32.4731</td>
<td>107.1612</td>
<td>11.8486</td>
<td>39.1004</td>
<td>2.4326</td>
<td>8.0276</td>
</tr>
<tr>
<td>HIGH_IN</td>
<td>3.3</td>
<td>20.4381</td>
<td>67.4457</td>
<td>20.4542</td>
<td>67.4989</td>
<td>5.2729</td>
<td>17.4006</td>
<td>0.2827</td>
<td>0.9329</td>
</tr>
<tr>
<td>SNVS_IN</td>
<td>3.3</td>
<td>0.0257</td>
<td>0.0847</td>
<td>0.0241</td>
<td>0.0796</td>
<td>0.0140</td>
<td>0.0461</td>
<td>0.0178</td>
<td>0.0586</td>
</tr>
</tbody>
</table>

5.2 Low-power mode

The power consumption in Table 9 and Table 10 is measured with the power mode switch project.

Table 9. Power consumption results

<table>
<thead>
<tr>
<th>Power Rail</th>
<th>Voltage (V)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCDC_IN</td>
<td>3.3</td>
<td>5.6543</td>
<td>18.6592</td>
<td>1.3263</td>
<td>4.3768</td>
<td>0.2192</td>
<td>0.7234</td>
</tr>
<tr>
<td>HIGH_IN</td>
<td>3.3</td>
<td>5.2542</td>
<td>17.3389</td>
<td>0.2601</td>
<td>0.8583</td>
<td>0.0223</td>
<td>0.0736</td>
</tr>
<tr>
<td>SNVS_IN</td>
<td>3.3</td>
<td>0.0133</td>
<td>0.0438</td>
<td>0.0171</td>
<td>0.0564</td>
<td>0.0109</td>
<td>0.0361</td>
</tr>
</tbody>
</table>

Table 10. Low power mode XIP on Flash

<table>
<thead>
<tr>
<th>Power Rail</th>
<th>Voltage (V)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCDC_IN</td>
<td>3.3</td>
<td>6.0045</td>
<td>19.8149</td>
<td>1.4586</td>
<td>4.8134</td>
<td>0.2156</td>
<td>0.7115</td>
</tr>
<tr>
<td>HIGH_IN</td>
<td>3.3</td>
<td>5.2568</td>
<td>17.3474</td>
<td>0.2601</td>
<td>0.8583</td>
<td>0.0222</td>
<td>0.0733</td>
</tr>
<tr>
<td>SNVS_IN</td>
<td>3.3</td>
<td>0.0136</td>
<td>0.0450</td>
<td>0.0177</td>
<td>0.0583</td>
<td>0.0114</td>
<td>0.0376</td>
</tr>
</tbody>
</table>

NOTE
All power consumption values are typical silicon at 25 C.
NOTE
Discontinuous conduction mode (DCM) increases the efficiency of DCDC in case of low current loading and is always recommended.

6 Conclusion
This document mainly describes how to measure power consumption on i.MX RT based on MIMXRT1060 EVK (Rev. A1). For more design details in designing a low-power application, see the application note How to use iMXRT Low Power Feature.

7 Revision history
Table 11. Revision history

<table>
<thead>
<tr>
<th>Revision number</th>
<th>Date</th>
<th>Substantive changes</th>
</tr>
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<td>0</td>
<td>09/2018</td>
<td>Initial release</td>
</tr>
<tr>
<td>1</td>
<td>08/2019</td>
<td>Updated the power consumption results</td>
</tr>
</tbody>
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8 References
1. i.MX RT 1060 Reference Manual
3. How to use iMXRT Low Power Feature