AN1253

An Improved PLL Design Method Without ω_n and ζ

Prepared by: Morris Smith

INTRODUCTION

This is a design guide for PLL synthesizers used in wireless products. It focuses on compact, low current and low cost synthesizers. Natural frequency and damping are not used in the calculations. The topics covered are:

a) PLL–related limitations on receiver and transmitter performance.
b) A simple measurement of charge pump spurious current at the reference frequency has been developed. It will be included on future datasheets. Formulas have been developed relating the spurious current at one reference frequency to other frequencies.
c) Optimal loop filter component values and PLL performance where design criteria include reference modulation bandwidth, VCO modulation bandwidth, switching time, overshoot after switching time period, reference sideband level, and noise within loop bandwidth.
d) Circuit and charge pump design compromises. Also design tolerance to changes in loop gain can be determined.

Topics are divided into three sections: system limitations and spurious current measurement; formulas and related tradeoffs; and a worked out and tested example.

SYSTEM LIMITATIONS AND SPURIOUS CURRENT MEASUREMENT

THIRD ORDER INTERMODULATION

This is mixing in a receiver front end which causes two adjacent strong undesired signals to mix onto a weak desired signal. Intermod dynamic range is defined as the difference between noise floor and undesired signal level that causes third order products to be mixed at the noise floor level. Third order products are shown below:

Example: f = desired signal, f_1, f_2 = undesired signal
f_1 = f+Δ
f_2 = f+2Δ
Δ = channel spacing

3rd order product falling on f:
$= 2f_1–f_2$
$= 2(f+\Delta) – (f+2\Delta)$
$= 2f+2\Delta – f – 2\Delta$
$= f$

PHASE NOISE

VCO phase noise can mix with strong adjacent channel signals to cover up a weak desired signal. The level of translated noise would depend on IF filter bandwidth and VCO noise density at a one channel offset from center frequency. Phase noise dynamic range is defined as the difference between noise floor and input signal level that causes phase noise to be mixed at the noise floor level. The formula is:

DR∅ = I∅I – 10 log B
DR∅ – Phase noise dynamic range (in dB)
∅ – Phase noise power density at adjacent channel offset (in dBc/Hz)
B – IF Bandwidth (in Hz)

REFERENCE SIDEBANDS

Sidebands cause the same effects as phase noise. They are however represented as a power level rather than power density. Also the product on the desired channel can be demodulated. Reference sideband dynamic range is the dB ratio between VCO carrier level and first sideband level.

OPTIMAL DESIGN

Optimal receiver design requires that 3rd order intermod dynamic range be equal to both the phase noise dynamic range and reference sideband dynamic range. Two undesired signals can simultaneously cause intermod, mix with VCO phase noise, and mix with reference sidebands.

SIGNAL TO NOISE RATIO

Signal to noise ratio in an FM or AM system can be estimated from the phase noise at the lowest offset frequency that contains information and the IF filter bandwidth.

SNR = I∅I – 10 log B, where I∅I = phase noise at lowest offset frequency

Actual signal to noise is better due to the noise decrease as offset frequency is increased. In an FM system, preemphasis and deemphasis provide additional SNR improvement. A good telephone line has a SNR of 40 dB and a cassette tape is 60 dB. Digital communications need better phase noise closer in.

WHY USE A CURRENT SOURCE CHARGE PUMP?

The current source charge pump has advantages over both the switching (pull up/pull down) and sample and hold types. Switching types have nonlinear gain over their output voltage range, which also depends on the direction the VCO is being pulled. The output FETs have a fixed on resistance. As a supply rail is approached, current the FET supplies when turned on decreases. This effect could mean a 10:1 variation of loop gain. The current source has a constant output current over its operating range. Sample and hold types have a transient output pulse present when state changes from sample to hold. This moves the VCO off frequency.

CHARGE PUMP LINEARITY

Pull up and pull down current must be equal for loop linearity. Current must be constant over the operating voltage range and from unit to unit over temperature. Loop gain changes proportionate to changes in charge pump current.

As an example of what can happen, a 25 ms switching loop was analyzed with a reduction in loop gain of 40%. Switching time increased to 41 ms, an increase of 64%. Transmitters which modulate the VCO or reference rely on constant current to maintain desired modulation roll–off frequencies. To reduce current consumption and noise, the filter of Figure 1 has been widely adopted.

SPURIOUS CURRENT MEASUREMENT

The spurious current measured is the RMS current component at the reference frequency passing through a two–element filter. The PLL must be phase locked. Current source charge pumps produce current components at least up to the 30th harmonic of reference frequency. Levels do not decline rapidly from harmonic to harmonic.

Through a current probe with 50 ohm output, and possibly a low noise amplifier, the spectrum analyzer can make a direct measurement. Many modern analyzers can convert the units of measure and add a correction factor. Try to use the current transformer with one turn through the core and increase the signal with the LNA. This will reduce the inductance in series with the loop filter. Inductance has not been a problem as long as the hole in the core isn't filled with wire. The test setup is shown in Figure 2.

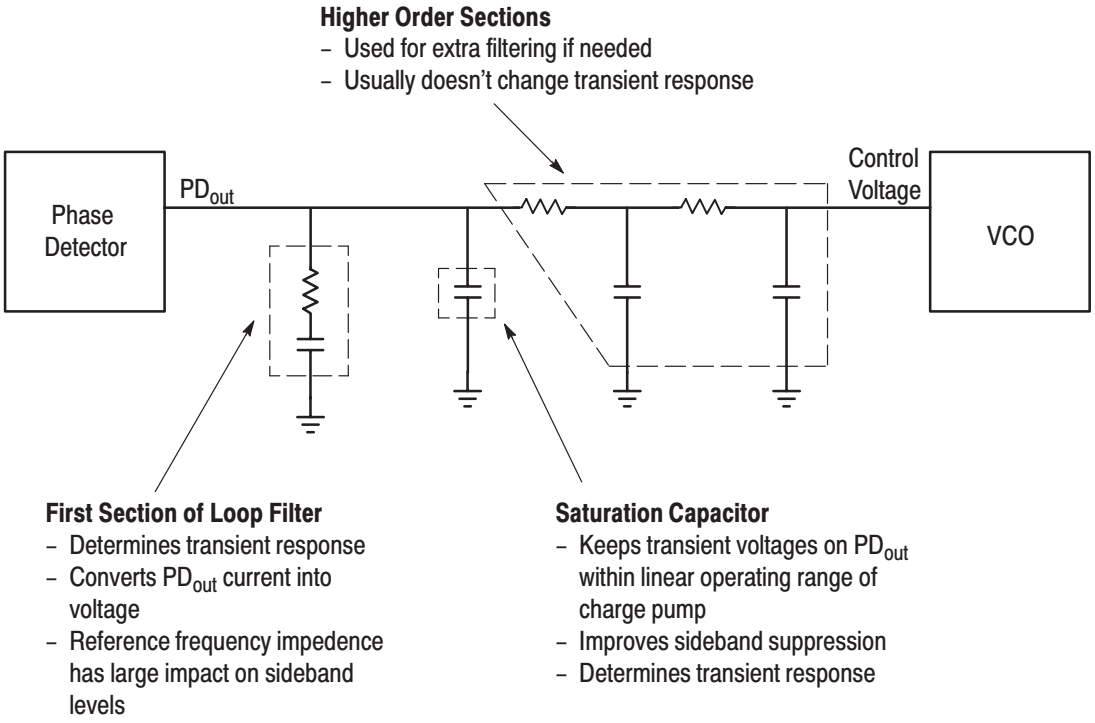
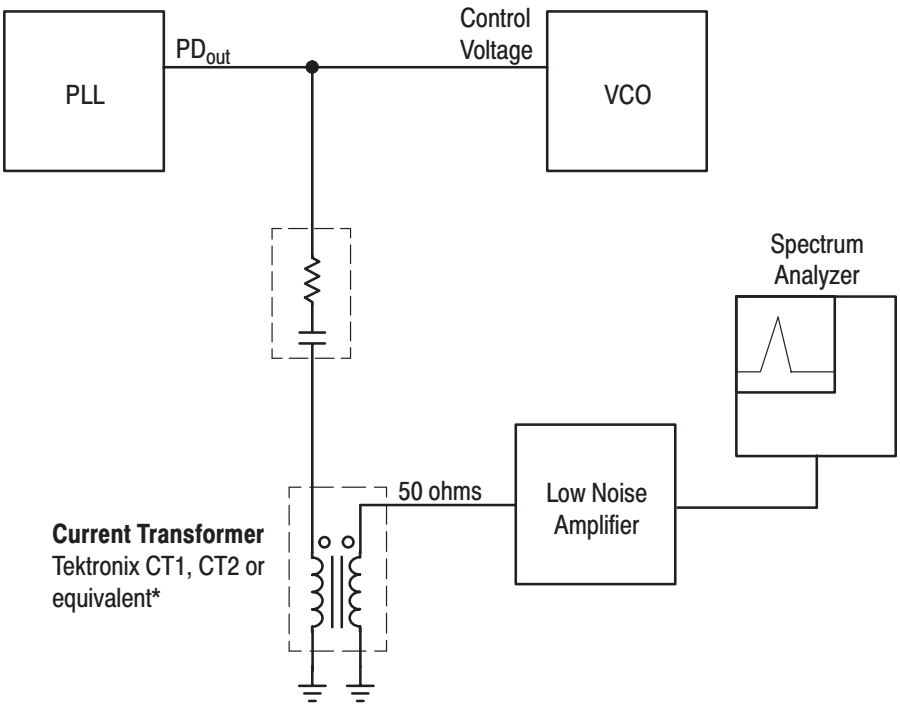


Figure 1. Standard Loop Filter



* Motorola cannot recommend one supplier over another and in no way suggests that this is a complete listing of transformer manufacturers.

Figure 2. Spurious Current Measurement

Table 1. Sample Measurements for the Motorola MC145190 PLL

Reference Frequency (kHz)	Current (nA)
10	1.95
20	4.5
25	11.0
50	28.4
100	141

FORMULA SUMMARY FOR SECOND ORDER PLL

DEFINITION OF VARIABLES

Where r and c are referred to, they are the first section resistor and capacitor of the loop filter. The loop analyzed has a second order response. Also described is a way to add additional higher order sections. All variables use base units. Bandwidth relations assume the use of optimal component values for maximum reference suppression. Log[x] is natural Log of x. Log[10,x] is base 10 Log of x. ’190 and ’191 are the Motorola MC145190 and MC145191 devices.

```
kv  =  VCO Gain (Radians/Second)/Volt
kp  =  Phase Detector gain (Amps/Radian)
a   =  kp*kv
n   =  Feedback divide ratio from VCO
t   =  time variable or switching time
       depending on formula (Seconds)
w   =  frequency variable or 3dB cutoff
       frequency depending on formula
       (Radians/Second)
r   =  resistor value (Ohms)
c   =  capacitor value (Farads)
```

$$b = \mathrm{Log}\left[\frac{\text{deviation}}{\text{tune\_range}}\right]$$

```
deviation  = Allowed frequency deviation
             (absolute value) from final
             frequency after switching time
             has elapsed (Hz)
tune_range = Output Frequency Range of VCO
             (Hz)
```

Closed loop gain in S plane is:

$$CG = \frac{VCO\_Phase}{Reference\_Phase} = \frac{a\,r\,s + \frac{a}{c}}{\frac{a}{n\,c} + \frac{a\,r\,s}{n} + s^2}$$

To satisfy switching time, overshoot requirements, provide best reference suppression and lowest thermal noise, resistance r and capacitance c are:

$$r = -\left(\frac{2\,n\,b}{a\,t}\right)$$

$$c = \frac{2\,a\,t}{n\,(b^2 + Pi^2)}$$

Normalized phase or frequency step response as a function of time (t) is:

$$nsr = 1 - \frac{\mathrm{Cos}\left[\frac{a^{1/2}\,(4\,n - a\,c\,r^2)^{1/2}\,t}{2}\right]}{E^{\frac{(a\,r\,t)/(2\,n)}{2\,c\,n}}} +$$

$$\frac{a^{1/2}\,a^{1/2}\,r\,\mathrm{Sin}\left[\frac{a^{1/2}\,(4\,n - a\,c\,r^2)^{1/2}\,t}{2}\right]}{E^{\frac{(a\,r\,t)/(2\,n)}{2\,c\,n}}\,(4\,n - a\,c\,r^2)^{1/2}}$$

The step response gives a final value of 1 and can be scaled for any frequency step.

Impedance of the optimal loop filter as a function of radian frequency (w) is:

$$z = \frac{n\,\left(b^4 + 2\,b^2\,Pi^2 + Pi^4 + 4\,b^2\,t^2\,w^2\right)^{1/2}}{t^4\,w^2\,a}$$

VCO MODULATION VOLTAGE

```
l    = RMS leakage current component at
       reference frequency
lx   = RMS leakage current component at
       highest frequency
f    = Reference Frequency
fx   = Highest reference frequency
Vrms = RMS modulation voltage
```

Over at least a 10 kHz to 100 kHz reference frequency range, leakage current can be predicted from a measurement at the highest frequency. Accuracy is better than 3 dB in sideband level.

Charge pump leakage current (lx) is measured using a Tektronix* CT–1 or CT–2 probe and spectrum analyzer. The probe is placed in the ground leg of loop filter. The spectrum analyzer measures RMS voltage into 50 ohms at the reference frequency. Using the probe calibration factor, current is computed. It is important that during measurement, the ground lead of loop filter be connected at the point where it ordinarily would be attached. Currents are in the nano–amp range and can be affected by digital circuit ground currents in other parts of the board. Leakage current is:

$$l = \left(\frac{f}{fx}\right)^2 lx$$

VCO modulation voltage is: Vrms = l z

SIDEBAND SUPPRESSION IN dBs

where Vrms = RMS volts modulating voltage on VCO tune line
Psb = Reference sideband suppression in dB (stated as positive number)
kv = VCO tuning sensitivity in (radians/second)/volt
f = Modulation (reference) frequency in Hz

$$Psb = 3.01 + 20\,Log\left[10, f\right] - 20\,Log\left[10, \frac{kv}{2\,Pi}\right] - 20\,Log\left[10, Vrms\right]$$

To increase sideband suppression, without changing other performance traits, an extra resistor–capacitor section can be added. The corner frequency should be at 10x the closed loop gain (– 3 dB) frequency and the resistor value should be 10x the loop filter resistor. A high resistor value helps isolate the two filter sections. On a functioning PLL it may be possible to lower both the corner frequency and resistor value of the added section. An extra section will add 20 dB/decade reference suppression above its corner frequency.

CLOSED LOOP GAIN

Closed loop gain as a function of radian frequency (w) is:

$$\text{Closed loop gain (cgw)} = \frac{\text{VCO frequency deviation}}{\text{Reference frequency deviation}}$$

$$cgw = \left(\frac{n^2\,(b^4 + 2\,b^2\,Pi^2 + Pi^4 + 4\,b^2\,t^2\,w^2)^{1/2}}{b^4 + 2\,b^2\,Pi^2 + Pi^4 + 2\,b^2\,t^2\,w^2 - 2\,Pi^2\,t^2\,w^2 + t^4\,w^4}\right)$$

DC gain is n. At infinite frequency it is 0. For cgw in Hz make the substitution for w (`w = 2 Pi f`). When stated in dBs, closed loop gain is the phase detector noise multiplication factor. In dBs:

```
cgwdB = 20*Log[10,cgw]
```

The following three formulas relate switching time, overshoot and the – 3 dB frequency of closed loop gain using an optimal filter.

The – 3 dB (relative to dc) frequency is:

$$w = \frac{\left(3\,b^2 + Pi^2 + 2\left(5\,b^4 + 4\,b^2\,Pi^2 + Pi^4\right)^{1/2}\right)^{1/2}}{t}$$

Overshoot is:

$$b = -\left(-Pi^2 - 3\,t^2\,w^2 + 2\left(t^2\,w^2\left(2\,Pi^2 + 5\,t^2\,w^2\right)\right)^{1/2}\right)$$

Switching time is:

$$t = \frac{\left(3\,b^2 + Pi^2 + 2\left(5\,b^4 + 4\,b^2\,Pi^2 + Pi^4\right)^{1/2}\right)^{1/2}}{w}$$

MODULATION RESPONSE

Modulation response as function of radian frequency (w) is:

(If modulation response is needed in Hz, use `Kv/(2 Pi)` to replace Kv and (`w = 2 Pi f`) to replace w.)

$$\text{Modulation Response (mr)} = \frac{\text{VCO frequency Change}}{\text{Control voltage change}}$$

$$mr = \frac{kv\ t^2\ w^2}{(b^4 + 2\,b^2\,Pi^2 + Pi^4 + 2\,b^2\,t^2\,w^2 - 2\,Pi^2\,t^2\,w^2 + t^4\,w^4)^{1/2}}$$

In dBs: mrdB = 20*Log[10,mr]
At infinite frequency mr = kv and at dc mr = 0.

The following three formulas relate switching time, overshoot, and the – 3 dB frequency of VCO modulation response using an optimal filter.

The – 3 dB frequency is:

$$w = \frac{(b^2 - Pi^2 + 2(b^4 + Pi^4)^{1/2})^{1/2}}{t}$$

Overshoot is:

$$b = -(-Pi^2 - t^2 w^2 + 2(t^2 w^2 (2 Pi^2 + t^2 w^2) + Pi^4)^{1/2})^{1/2}$$

Switching time is:

$$t = \frac{(b^2 - Pi^2 + 2(b^4 + Pi^4)^{1/2})^{1/2}}{w}$$

CHARGE PUMP DYNAMIC RANGE

The charge pump output voltage range must cover VCO tune range, twice the overshoot, and twice the voltage spikes caused by correction pulses. When switching from low to high channel or high to low channel, there will be a point where correction pulses ride on top of peak overshoot. The voltage spike magnitude is given by ohms law where (i) is charge pump current and (r) is loop filter resistor. For a maximum value of r in a given circuit there is a minimum switching time.

CHARGE PUMP CURRENT

Increasing charge pump current will reduce thermal noise from the loop filter resistor, but it won't change the minimum switching time. It will also increase the capacitor value proportionately.

REDUCE SWITCHING TIME BY INCREASING VCO SENSITIVITY

The 25 ms loop given as an example was the minimum switching time for the tuning range and VCO used with the '190 and a 8.5 volt charge pump supply. Increasing VCO sensitivity reduces switching time somewhat more than proportionately. Sideband levels would remain the same for the same switching time. This is because increasing Kv decreases loop filter resistor to exactly compensate. Noise within loop bandwidth will stay the same but thermal noise from the loop filter resistor gets worse. Thermal noise modulation voltage is proportional to square root of r. For a 10x increase in Kv, r drops by a factor of 10 and thermal noise level increases by 10 dB. It is possible to have spurious pickup problems outside loop bandwidth with high Kv. Also maintaining Q in the VCO while increasing coupling between varicap diodes and tuned circuit, and obtaining high value high tolerance loop filter capacitors can be difficult. Thermal noise will probably not be a problem in common high volume applications of PLLs.

SOURCE/SINK CURRENT MATCH CHANGES SWITCHING TIME

Lack of source/sink match makes it difficult to achieve design values of switching time. For some value of mismatch and switching in one direction, the design value should be in between the source and sink, and closer to the one which is on for the most time. The position of the design value relative to source and sink should be inversely proportionate to the relative on times during the switching period. In the example circuit, for a low to high channel jump, the design value was 2 mA, optimal source current was 1.97 mA, and sink was 2.14 mA. Measured switching time was 27.4 ms. Switching in the opposite direction took 34.3 ms. The 8.5% source sink mismatch caused worst case switching time to be 37% slower than the design value.

EFFECTS OF USING STEP SIZE WHICH IS SUB–MULTIPLE OF CHANNEL SPACING

The same sideband suppression can be obtained with the same switching time at any sub–multiple step size of the channel spacing. This assumes the loop is linear. Since r is proportionate to the feedback divider ratio, the loop will only be linear for longer switching times. Thermal noise gets worse proportionate to square root of r. Noise in loop bandwidth gets a little worse over a wide range of step sizes. The ’190 phase detector at 10 Hz offset with 10 kHz step size had noise of –156 dB/Hz and at 100 kHz step size, it was –141 dBc/Hz. Because of noise multiplication, there would be a 5 dB benefit to using the 100 kHz step size.

VCO SENSITIVITY CHANGE AS MODULATION FREQUENCY VARIES

Above the – 3 dB frequency of modulation response, the output frequency will deviate the same amount for the same modulation voltage regardless of modulation frequency. However, the sidebands created will be greatest in magnitude at the lowest frequency. Sidebands will decline in value at a 20 dB/decade rate as modulation frequency increases. Due to the sideband slope, thermal noise, if it is a problem, will appear as a bump at the – 3 dB frequency of modulation response.

HIGHER CHARGE PUMP SUPPLY VOLTAGES REDUCE SWITCHING TIME AND NOISE

Using a higher supply voltage on the charge pump allows correction pulses to be larger with the loop remaining linear. The loop filter resistor can increase in value. Minimum switching time can decrease. Also VCO gain (kv) could be reduced. Lower VCO gain results in less thermal noise, less tendency to pick up noise outside loop bandwidth, higher oscillator Q and smaller value tighter tolerance capacitors in loop filter.

PRODUCTION SENSITIVITY

$$r = \frac{2\,n\,b}{a\,t}$$

$$c = \frac{a\,t^2}{n\,(b^2 + Pi^2)}$$

There are two extrema of performance variation with component change. Only one need be calculated. One is:
n = n_max; a = a_min; r = r_min; c = c_max;

n in most applications varies by up to ± 10%. It isn’t a problem if charge pump current can be ramped up and down (in software) to compensate (although the ’190 and ’191 devices presently do it in 10% steps). (a/n) ratio must be kept constant for all output frequencies. (a=kp*kv) is the major production problem. kv for a Motorola ’V17 VCO varies ± 5%. kp of the 14519X PLLs varies ± 40%. Total variation of (a) could be ± 47% using the above. A second order loop designed with a 40% tolerance of (a) had a 64% tolerance of switching time.

r can have up to 1% tolerance, with 5% being standard. c can be 1% tolerance, up to 5,000 pF (COG dielectric) with 5% standard. Above 5,000 pF, dielectric changes to X7R which has 5% or 10% tolerance. X7R dielectric is available up to about 0.5 µF in 5% tolerance. Above 0.5 µF tantalum, polystyrene or polypropylene can be used. Polypropylene and polystyrene are too large for compact wireless circuits. The only choice left, tantalum, is available only in 10% tolerance. Charge pump current should be set to keep capacitor in high tolerance range.

Conclusion: To build an optimal loop, high tolerance of kv and kp is needed.

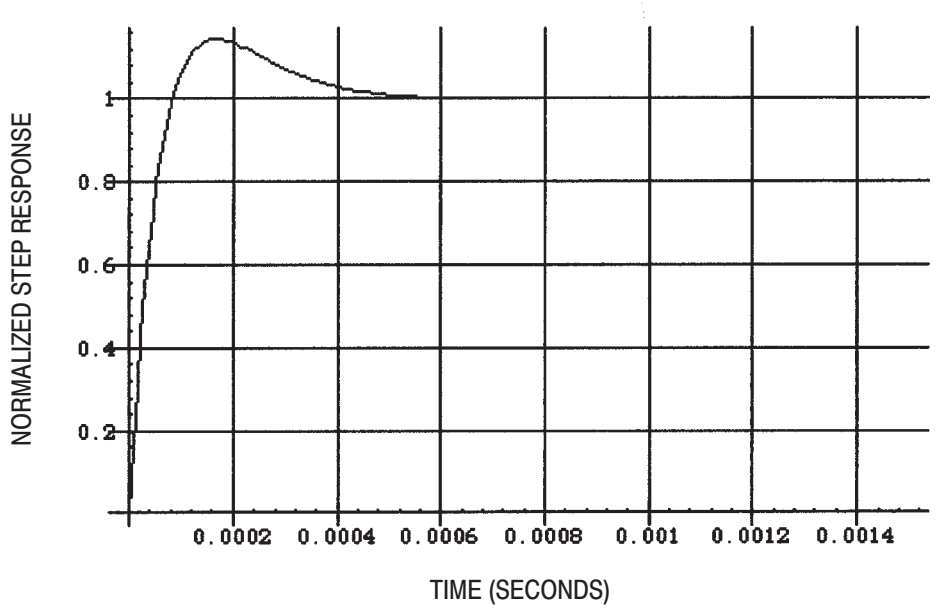


Figure 3. Step Response for a GSM Loop Designed for a = 6300

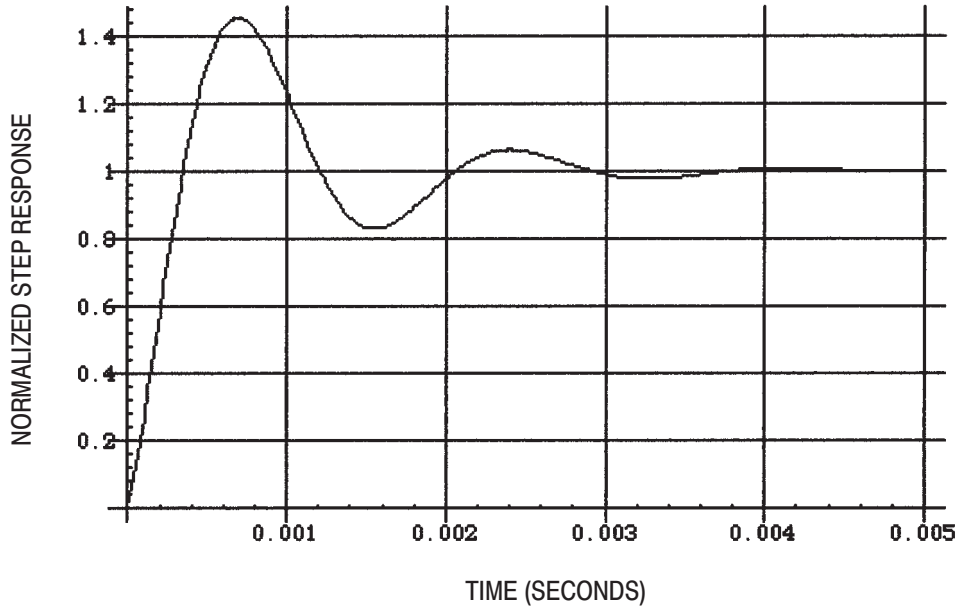


Figure 4. Step Response With All Parameters the Same Except a = 630

Note that time scales for the two graphs are different!

In most instances reducing (a) upsets loop dynamics too much. Even when locked, the VCO experiences disturbances; i.e., vibration. Overshoot can pull the PLL off frequency. Natural frequency is also much lower, so response is slow.

SATURATION CAPACITOR AND EXTRA FILTER SECTIONS

The calculated values for r and c have appeared experimentally to be optimum, with or without the saturation capacitor. To design the loop filter, r and c should first be selected. It is all right for the resistor to cause loop nonlinearity if the saturation capacitor has not been added. The saturation capacitor is added and adjusted for minimum switching time. A good initial value is 5 – 25% of c. Loop linearity is checked by making both small and large frequency jumps. If the loop isn't linear then the filter must be designed for a longer switching time. Extra filter sections are added to roll–off sidebands and PLL device noise, but should not modify transient response.

EXAMPLE: PLL THAT SWITCHES IN 25 ms

The PLL uses a MC145190 with 2 mA of charge pump current. Thus:

$$kp = \frac{0.002}{2\ Pi};$$

The Motorola custom VCO used (a V17) has a sensitivity of 3.0 – 3.3 MHz/volt. So converting to (radians / second) / volt:

$$kv = 2\ Pi\ 3.15\ 10^{6};$$

The design constant a is: a = kp kv = 6300

The VCO operates 739.3 – 749.3 MHz. Channel spacing is 100 kHz. The median feedback divide ratio (n) is:

$$n = \frac{744.3}{0.1} = 7443.$$

Switching time t given by system specification is 25 ms. Thus:

$$t = \frac{25}{10^{3}};$$

Frequency deviation tolerance is set at 1 kHz. Tune range is 10 MHz. b is:

$$b = \mathrm{Log}\left[\frac{0.001}{10}\right] = -9.21034$$

Resistor and capacitor values are:

$$r = -\left(\frac{2\ n\ b}{a\ t}\right) = 870.509$$

$$c = \frac{a\ t^{2}}{n\ (b^{2} + Pi^{2})} = 5.58628\ 10^{-6}$$

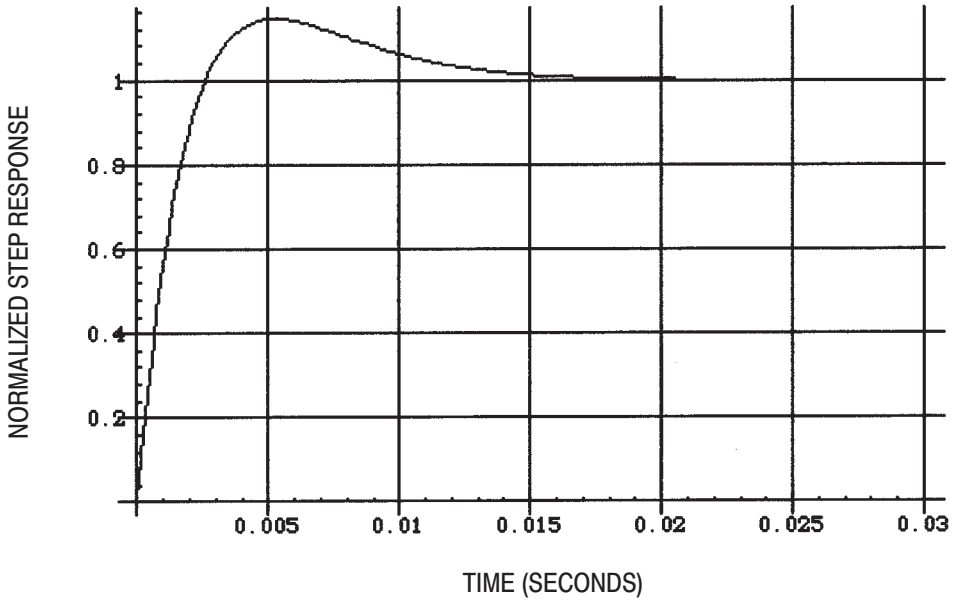


Figure 5. Normalized Step Response

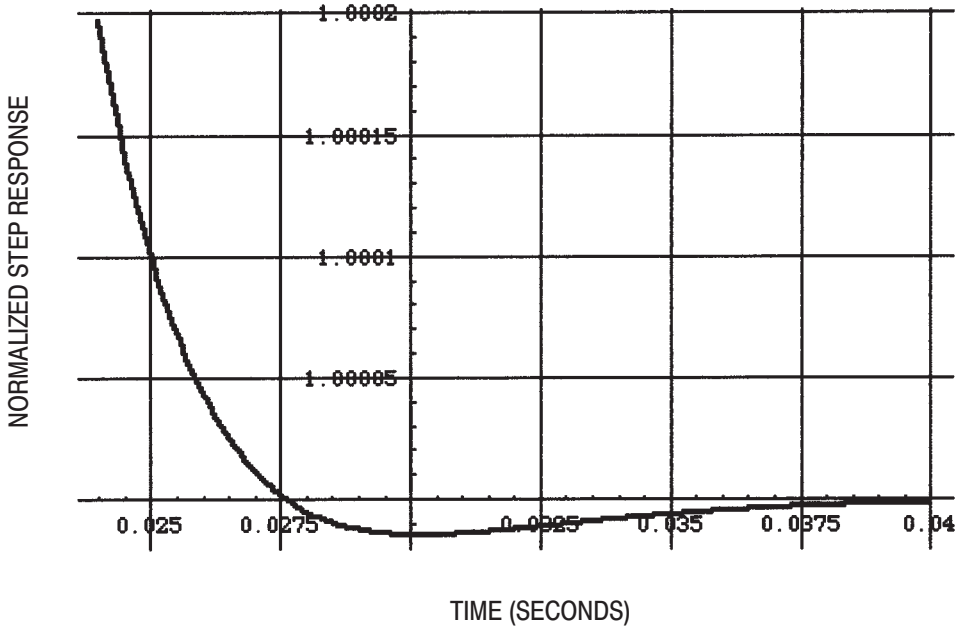


Figure 5a. Normalized Step Response — Expanded View

Loop filter impedance at 100 kHz is:

$$w = 2\,Pi\,1\,10^{5}\,;\; t = \frac{25}{10^{3}};$$

$$z = \frac{n\left(\frac{b^{4} + 2\,b^{2}\,Pi^{2} + Pi^{4} + 4\,b^{2}\,t^{2}\,w^{2}}{t^{4}\,w^{2}}\right)^{1/2}}{a} = 870.509$$

VCO MODULATION VOLTAGE

```
l    = RMS leakage current component at reference frequency
lx   = RMS leakage current component at highest frequency
f    = Reference Frequency
fx   = Highest reference frequency
Vrms = RMS modulation voltage
```

Over at least a 10 kHz to 100 kHz reference frequency range, leakage current can be predicted from a measurement at the highest frequency. Accuracy is better than 3 dB in sideband level.

$$f = 100\,10^{3}\,;\; fx = 200\,10^{3}\,;\; lx = \frac{564}{10^{9}};$$

$$l = \left(\frac{f}{fx}\right)^{2} lx$$

$$= 1.41\,10^{-7}$$

VCO modulation voltage is: Vrms = l z = 0.000122742

SIDEBAND SUPPRESSION IN dBs

```
where  Vrms = RMS volts modulating voltage on VCO tune line
       Psb  = Reference sideband suppression in dB (stated as positive number)
       Kv   = VCO tuning sensitivity in (Radians/Second)/volt
       f    = Modulating frequency in Hz
```

$$Psb = 3.01 + 20\,Log\left[10, f\right] - 20\,Log\left[10, \frac{kv}{2\,Pi}\right] - 20\,Log\left[10, Vrms\right];$$

$$= 51.2639\ dB$$

CLOSED LOOP GAIN AS A FUNCTION OF FREQUENCY

This also gives phase detector noise multiplication when stated in dBs. For cgw in Hz, make the substitution for w (w = 2 Pi f).

$$\text{Closed loop gain} = \frac{\text{VCO frequency deviation}}{\text{Reference frequency deviation}}$$

$$cgw = \left(\frac{n^2\,(b^4 + 2\,b^2\,Pi^2 + Pi^4 + 4\,b^2\,t^2\,w^2)}{b^4 + 2\,b^2\,Pi^2 + Pi^4 + 2\,b^2\,t^2\,w^2 - 2\,Pi^2\,t^2\,w^2 + t^4\,w^4}\right)^{1/2}$$

$$cgwdB = 20*Log[10,cgw];$$

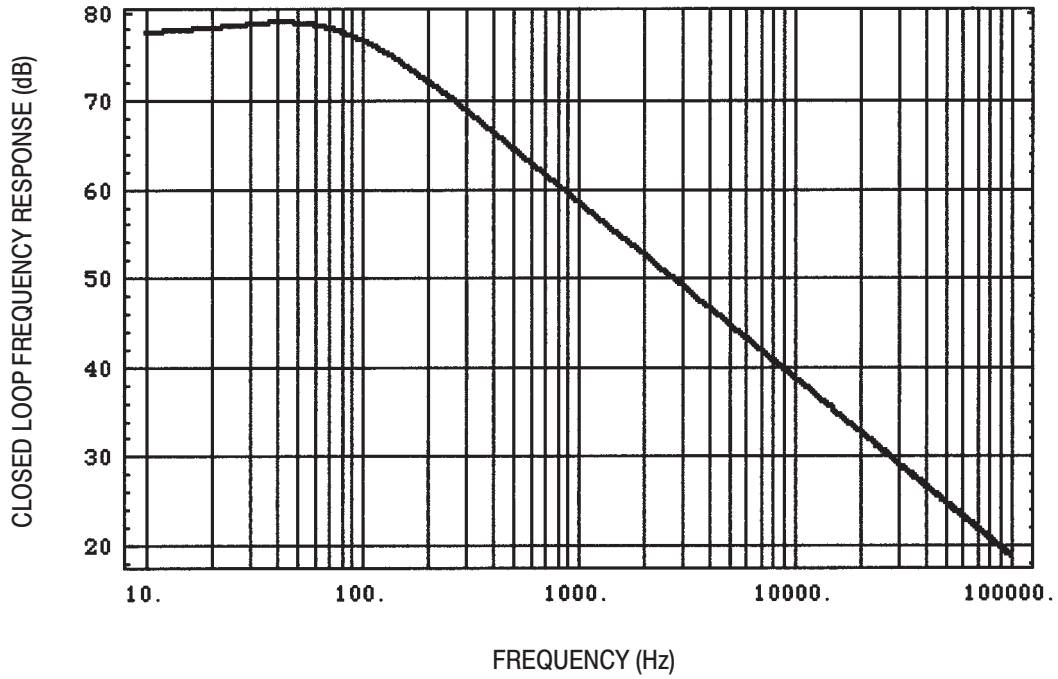


Figure 6. Closed Loop Gain

The – 3 dB frequency of closed loop gain is:

$$w = \frac{(3\,b^2 + Pi^2 + 2\,(5\,b^4 + 4\,b^2\,Pi^2 + Pi^4)^{1/2})^{1/2}}{t} = 933.956$$

$$f = \frac{w}{2\,Pi} = 148.644 \text{ Hz}$$

VCO MODULATION RESPONSE

If modulation response is needed in Hz use Kv/(2 Pi) to replace Kv and (w = 2 Pi f) to replace w.

$$kv = kv/(2*Pi) = 3.15\ 10^{6}$$

$$mr = \frac{2\ 2}{kv\ t\ \ w}$$

$$\frac{}{4 \quad 2 \quad 2 \quad 4 \quad 2\ 2\ 2 \quad 2\ 2\ 2 \quad 4\ 4\ 1/2}$$
$$(b\ \ + 2\ b\ \ Pi\ \ + Pi\ \ + 2\ b\ \ t\ \ w\ \ - 2\ Pi\ \ t\ \ w\ \ + t\ \ w\ )$$

$$mrdB = 20*Log[10,mr];$$

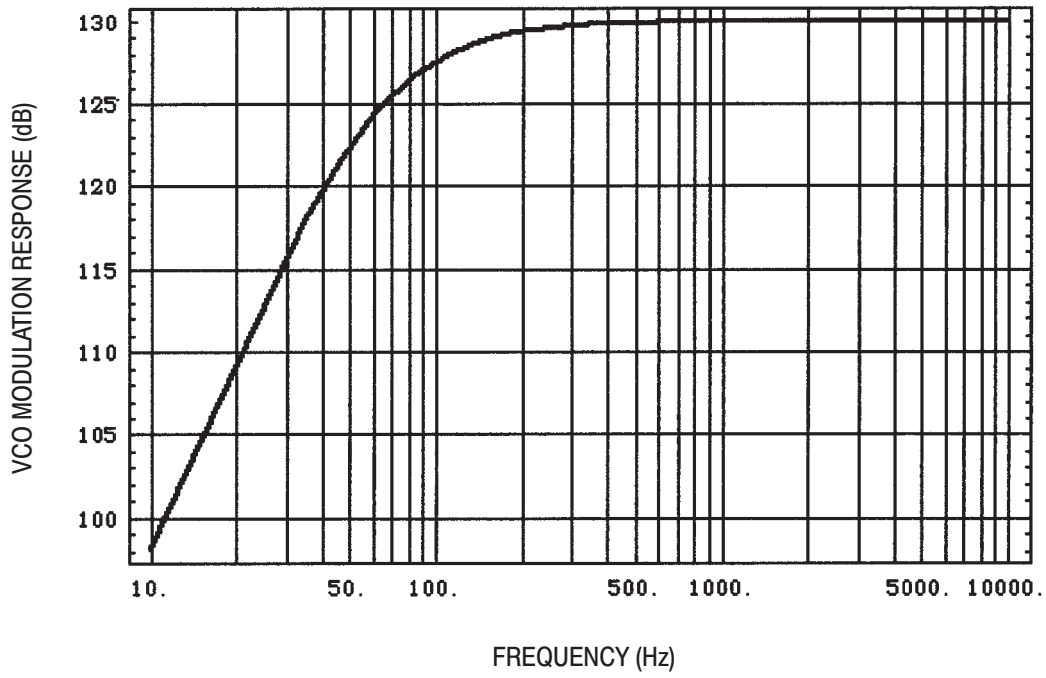


Figure 7. Modulation Response

The – 3 dB frequency of modulation response is:

$$w = \frac{\sqrt{(b\ \ - Pi\ \ + 2 \quad (b\ \ + Pi\ )\ \ )}}{t}; \text{ where } f = \frac{w}{2\ Pi};$$

$$f = 89.0672\ Hz$$

PRODUCTION SENSITIVITY — A TOLERANCE ONLY

a=kp*kv is decreased by 40% to account for charge pump current tolerance in the '190 or '191 PLL. Thus a = 0.6*a = 3780.

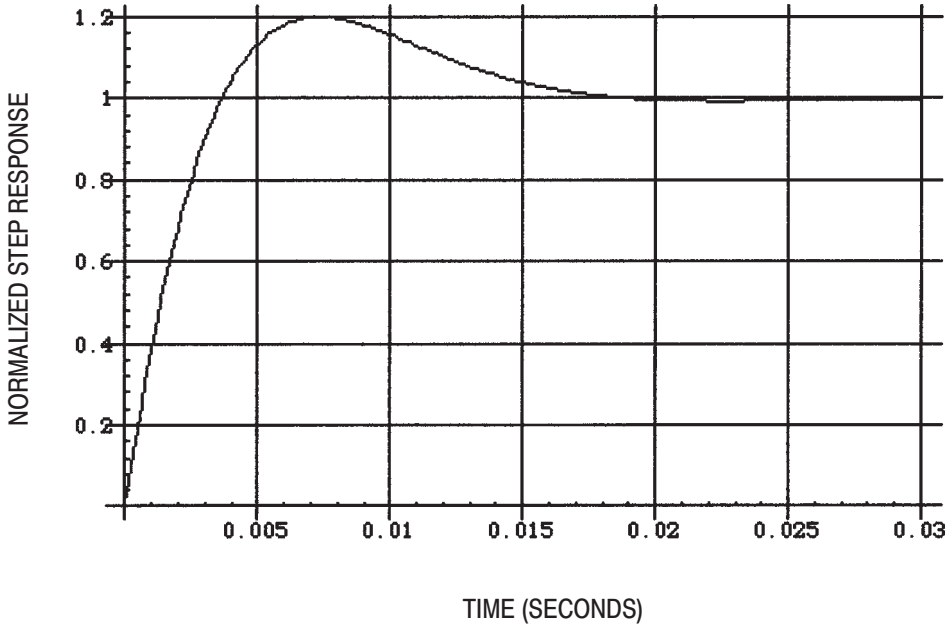


Figure 8. Normalized Step Response (a = 3780)

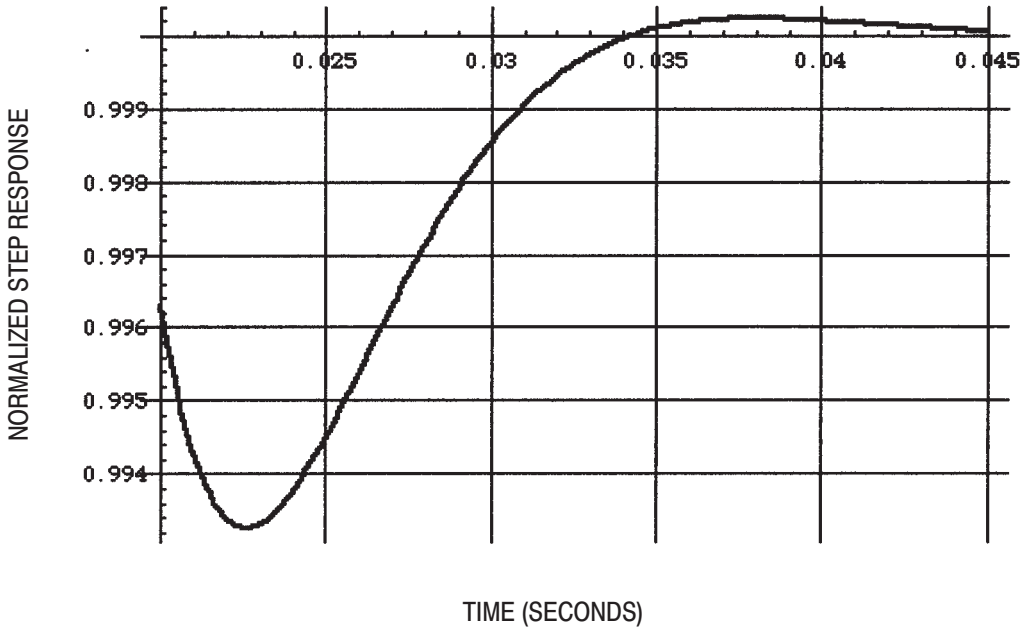


Figure 8a. Normalized Step Response — Expanded View (a = 3780)

The reduction in (a) of 40% has caused switching time to change from 25 ms to 41 ms. This is an increase of 64%.

PRODUCTION SENSITIVITY — CUMULATIVE TOLERANCE

a was decreased previously by 40% to account for tolerance. r and c 5% tolerances are assumed. Therefore:

$$c = 1.05*c = 5.86559\ 10^{-6}, \quad r = 0.95*r = 826.983$$

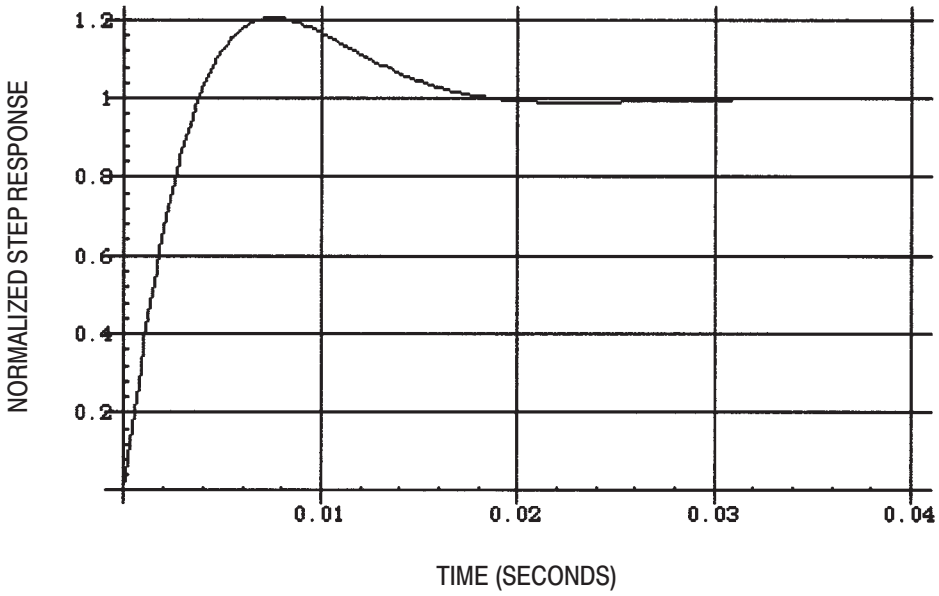


Figure 9. Normalized Step Response

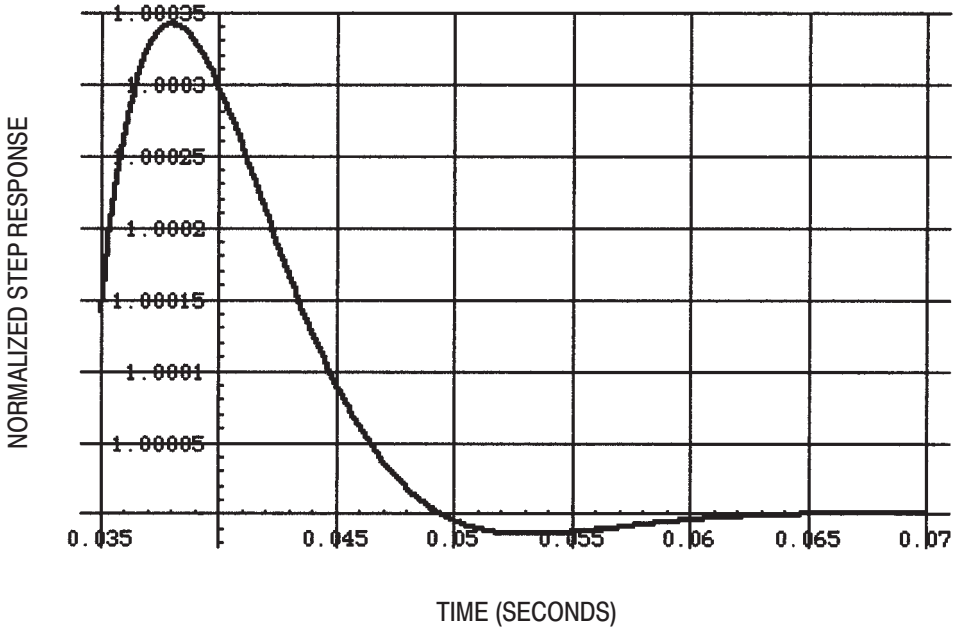


Figure 9a. Normalized Step Response — Expanded View

Switching time is 45 ms with resistor capacitor and charge pump variation. Original design value was 25 ms. Switching time is 80% worse.

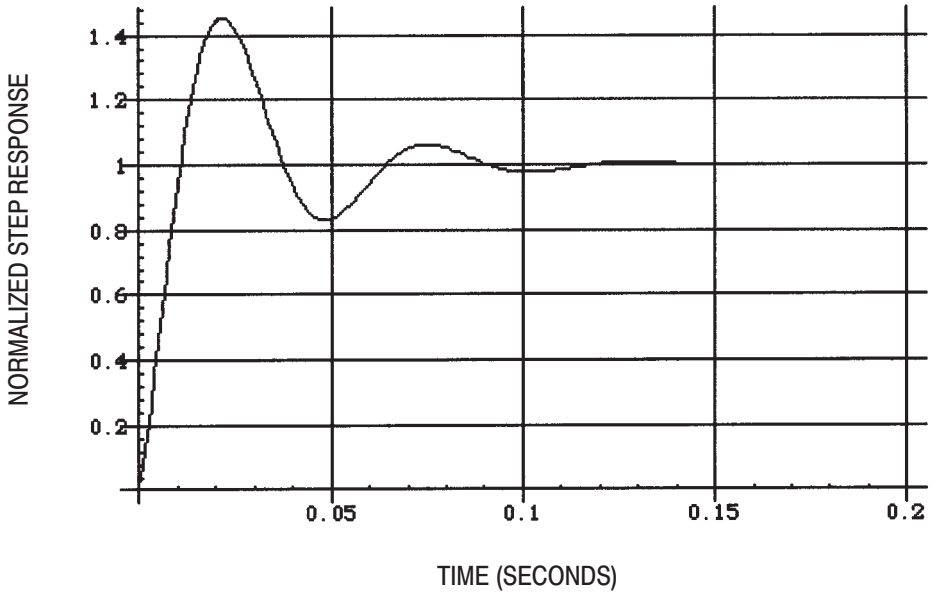


Figure 10. Normalized Step Response When a is Reduced by Factor of 10

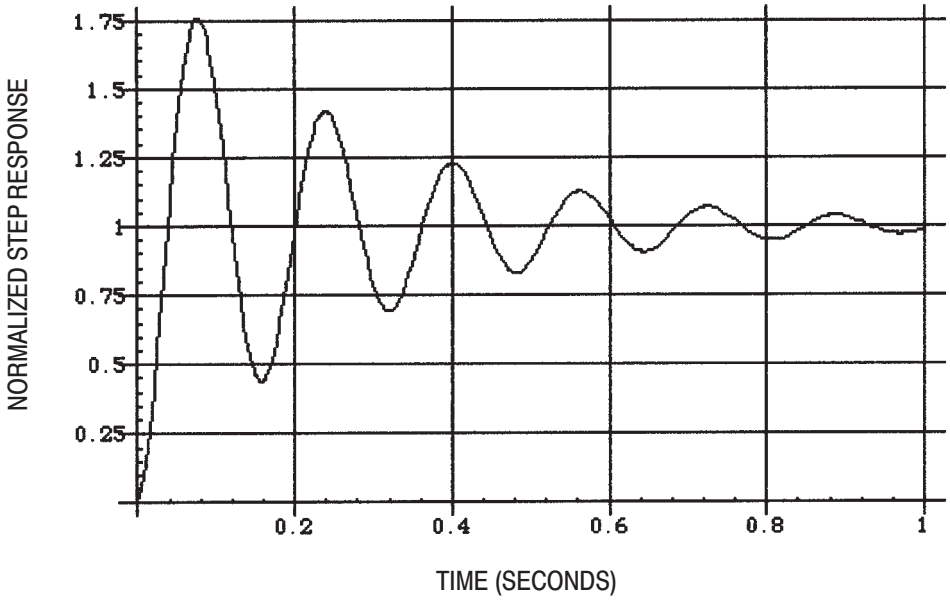


Figure 11. Normalized Step Response When a is Reduced by Factor of 100

REFERENCES

1. Mathematica Enhanced version 2.2, Wolfram Research, Champaign IL, 1993.

2. Discussions with Jim Irwin of Motorola, Semiconductor Products Sector.

NOTES

NOTES

NOTES

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com – TOUCHTONE 1–602–244–6609
Motorola Fax Back System – US & Canada ONLY 1–800–774–1848
– http://sps.motorola.com/mfax/

HOME PAGE: http://motorola.com/sps/

JAPAN: Nippon Motorola Ltd.: SPD, Strategic Planning Office, 141,
4–32–1 Nishi–Gotanda, Shagawa–ku, Tokyo, Japan. 03–5487–8488

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

CUSTOMER FOCUS CENTER: 1–800–521–6274