AN12573

i.MX 7ULP Power Consumption Measurement

Rev. 0 — September 2019 Application Note

1 Introduction

This application note helps the user design power management systems. This report provides power consumption measurements for several use cases and provides information on minimizing power consumption on the i.MX 7ULP.

Because the data presented in this application note is based on empirical measurements taken on a small sample size, the presented results are not guaranteed.

Contents

2 Acronyms and abbreviations

Table 1 defines the acronyms and abbreviations used in this document.

Table 1. Acronyms and definitions

Term	Definition
A7	Arm® Cortex®-A7 processor
AD	Application Domain
ADC	Analog-to-Digital Converter
AHB	Arm AMBA High-performance Bus
APLL	Auxiliary Phase-Locked Loop clock generator
Arm	Advanced RISC machines processor architecture
AWIC	i.MX 7ULP Asynchronous Wakeup Interrupt Controller
AXI	Arm Advanced eXtensible Interface
BSP	Board Support Package
CMP	i.MX 7ULP Analog Comparator module
DAC	Digital-to-Analog Converter
DDR	Dual data rate DRAM
DGO	Designator for the Always On power domain
DMA	i.MX 7ULP Direct Memory Access Controller
DRAM	Dynamic Random-Access Memory
DVFS	Dynamic Voltage and Frequency Scaling
EVK	Evaluation Kit
FBB	Forward Body Bias
FIRC	FAST Internal Reference Clock
GND	Ground
GPIO	General-purpose input/output
GPU	Graphics Processing Unit
GPU2D	2-Dimensional Graphics Processing Unit
GPU3D	3-Dimensional Graphics Processing Unit
High-Z	High impedance
HSRUN	i.MX 7ULP High Speed Run mode
I/Os	Inputs / Outputs
IOMUX	Chip-level I/O multiplexing
IOMUXC	i.MX 7ULP Input/Output Multiplexing Controller

Table continues on the next page...

Table 1. Acronyms and definitions (continued)

Term	Definition
IPG	i.MX 7ULP Internal Peripheral clocks and controls
LDO	Low drop-out regulator
LLS	i.MX 7ULP Low Leakage Stop mode
LPDDR2	Low-power DDR2 SDRAM
LPDDR3	Low-power DDR3 SDRAM
LPTMR	i.MX 7ULP Low Power Timer
LVD	Low-Voltage Detector
M4	Arm Cortex-M4 processor
MIPI DSI	MIPI display serial interface controller
MMDC	Multi-mode DDR controller
MU	i.MX 7ULP Messaging Unit
OTP	One-time programmable
PCB	Printed Circuit Board
PLL	Phase-Locked Loop clock generator
PMC	Power Management Controller
PMIC	Power management integrated circuit
PSTOP	i.MX 7ULP Low Power Partial Stop mode
PTA	Signals associated with Port A
PTB	Signals associated with Port B
PTC	Signals associated with Port C
PTD	Signals associated with Port D
PTE	Signals associated with Port E
PTF	Signals associated with Port F
QSPI	i.MX 7ULP Quad Serial Peripheral Interface module
RAM	Random access memory
RBB	Reverse Body Bias
ROM	Read-only memory
RTC	Real-Time Clock
RTD	Real-Time Domain
RUN	i.MX 7ULP Normal Speed Run mode
SDK	Software Development Kit
SIM	i.MX 7ULP System Integration Module

Table continues on the next page...

Table 1. Acronyms and definitions (continued)

Term	Definition
SIRC	Slow Internal Reference Clock
SNVS	Secure Non-Volatile Storage
SoC	System on Chip
SPLL	System Phase-Locked Loop clock generator
SRAM	On-Chip Static Random Access Memory
SRTC	i.MX 7ULP Secure Real-Time Clock
STOP	i.MX 7ULP Low Power Stop mode
TCM	Cortex-M4 Tightly-Coupled Memory
UART	Universal asynchronous receiver/transmitter
USB	Universal serial bus
USB 2.0	USB version 2.0 peripheral
USB HSIC	Universal serial bus high-speed inter-chip physical layer
USB OTG	USB on-the-go
uSDHC	Ultra-secured digital host controller
VLLS	i.MX 7ULP Very Low Leakage Stop mode
VLPR	i.MX 7ULP Very Low Power Run mode
VLPS	i.MX 7ULP Very Low Power Stop mode
WFI	Wait-for-interrupt

3 Overview of i.MX 7ULP power domains

The i.MX 7ULP has several power domains each containing multiple power supplies.

The i.MX 7ULP power architecture is organized in four main power domains:

- The **Real-Time Domain (RTD)** contains the Arm Cortex-M4 platform, multiple peripherals, system-level components and two GPIO ports (Ports A and B).
- The **Application Domain (AD)** contains the Arm Cortex-A7 platform, a 3D Graphics Processing Unit (3DGPU), a 2D Graphics Processing Unit (2DGPU), the LPDDR2/LPDDR3 interface (MMDC), the MIPI DSI display interface, multiple peripherals, and four GPIO ports (Ports C, D, E and F).
- The **DGO "Always-On" Domain** contains reset and system mode control logic, the Low-Leakage Wakeup Unit (LLWU), analog comparators and low-power timers.
- The **VBAT Domain** contains the Real-Time Clock (RTC) and Secure Non-Volatile Storage (SNVS) components.

In general, these domains are independent of each other. Multiple power modes are available in the Real-Time Domain and the Application Domain to optimize power consumption to the demands of the application at a given time. These modes optimize power consumption by reducing clock frequencies, reducing voltages, gating clocks and gating power supplies.

Figure 1 shows the connections of the power supplies and the distribution of the internal power domains.

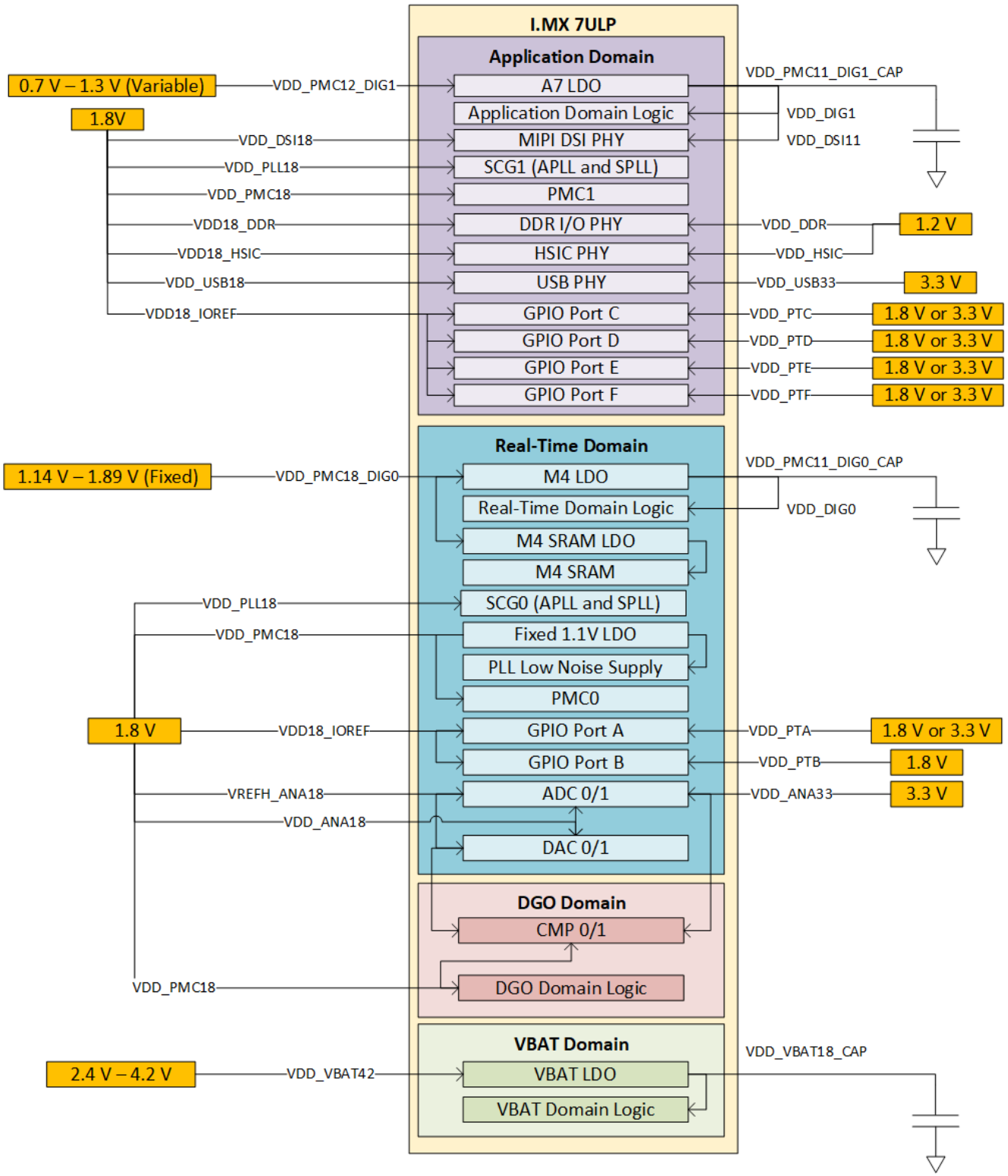

Figure 1. i.MX 7ULP power supplies and power domains (LDO Enabled Mode shown)

The external supplies shown in Figure 1 do not imply that separate power supplies are required for each orange block shown.

- All the i.MX 7ULP 1.2 V supplies can provided from a single source.

- All the i.MX 7ULP 1.8 V supplies can provided from a single source.
- All the i.MX 7ULP 3.3 V supplies can provided from a single source.

NOTE

For the recommended operating conditions of each supply rail and for a detailed description of the groups of pins powered by each I/O voltage supply, see i.MX 7ULP Applications Processor - Consumer Products data sheet (document IMX7ULPCEC).

For more details regarding the i.MX 7ULP power architecture, see i.MX 7ULP Applications Processor Reference Manual (document IMX7ULPRM).

4 Internal power measurement of the i.MX 7ULP processor

Several use cases (described in Use cases and measurement results) have been run on the i.MX 7ULP EVK (MCIMX7ULP-EVK). Some measurements have been obtained from other hardware as indicated.

The low-power mode measurements in this document apply to multiple power supplies.

The RUN mode and High-Speed RUN (HSRUN) mode measurements in this document primarily contains measurements from the dominant power supply in each active domain:

- For the Real-Time Domain, the dominant supply is VDD_PMC18_DIG0. This supply provides power to the internal LDO and the downstream low-voltage logic (including the M4, on-chip memory and peripherals). The internal LDO in this domain controls the voltage to the logic under software control.
- For the Application Domain, the dominant supply depends on the internal LDO configurations:
  - In LDO Enabled mode, a constant voltage is applied to VDD_PMC12_DIG1 and the internal LDO provides a lower voltage to the logic under software control. For more details on A7 LDO Enabled Mode, see A7 LDO enabled mode.
  - In LDO Bypass mode, the internal LDO is disabled and VDD_PMC12_DIG1, VDD_PMC11_DIG1_CAP, VDD_DIG1, and VDD_DSI11 are all connected externally. An external variable voltage is provided usually by an external Power Management IC (PMIC). This combined group of supplies is the dominant power consumer. The MCIMX7ULP-EVK is designed to operate in A7 LDO Bypass mode. All power measurements in this document were taken in A7 LDO Bypass mode. For more details on A7 LDO Bypass mode, see Overview of i.MX 7ULP power domains.

4.1 DGO "Always ON" domain power supplies

The following power supplies are used by the DGO domain:

- VDD_PMC18 supplies the following circuits:
  - CMP0/1
  - PMC0/1
  - Slow Internal Reference Clock (SIRC) generation [16 MHz]
  - FAST Internal Reference Clock (SIRC) generation [48 MHz]
  - Multiple other chip-level functions

4.2 Real-Time Domain (RTD) power supplies

The following power supplies are used by the Real-Time Domain:

- VDD_PMC18_DIG0 supplies the following circuits:
  - M4 LDO, which provides power to the RTD low-voltage logic. The LDO output VDD_PMC11_DIG0_CAP is connected to an external filter capacitor and it routed back into VDD_DIG0 to supply the internal logic. For decoupling and bulk capacitor requirements, see i.MX 7ULP Hardware Development Guide (document IMX7ULPHDG).

  - M4 SRAM LDO, which provides a fixed voltage to the on-chip RAM

- VDD_PMC18 supplies the following circuits:
  - A portion of the M4 LDO
  - An internal fixed-voltage LDO which outputs a low-noise 1.1 V power source for the PLLs. VDD_PMC18 also supplies the DGO **Always-ON** domain logic and the Power Management Controller 0 (PMC).
- VDD_PTA supplies the I/Os on Port A (signals named PTA*nn*).
- VDD_PTB supplies the I/Os on Port B (signals named PTB*nn*).
- Power consumption of VDD_PTA and VDD_PTB are completely application dependent and as such, measurements for these supplies are not included in this document. For an equation that can be used to estimate GPIO segment power based on the activity of the individual I/O signals, see the **Maximum Supply Currents** table in i.MX 7ULP Applications Processor - Consumer Products data sheet (document IMX7ULPCEC).

4.3 Application Domain (AD) power supplies

The following power supplies are used by the Application Domain:

- VDD_PMC12_DIG1/VDD_PMC11_DIG1_CAP/VDD_DIG1 supplies the A7 LDO and the application domain logic. The LDO output, VDD_PMC11_DIG1_CAP, is connected to an external filter capacitor and is routed back into VDD_DIG1 to supply the internal logic. For decoupling and bulk capacitor requirements, see i.MX 7ULP Hardware Development Guide (document IMX7ULPHDG). The board-level configuration of these supplies is dependent on the choice of A7 LDO Enabled mode or A7 LDO Bypass mode. For details, see On-chip LDO regulator modes.
- VDD_PMC18 supplies the following circuits:
  - A portion of the A7 LDO
  - PMC1
- VDD_DSI18 and VDD_DSI11 supply the MIPI DSI display interface. VDD_DSI11 must always be connected to VDD_DIG1 at the board level.
- VDD18_DDR and VDD_DDR supply the LPDDR2/LPDDR3 PHY. VDD_DDR is the 1.2 V supply for the LPDDR2/LPDDR3 interface I/Os.
- VDD18_HSIC and VDD_HSIC supply the HSIC PHY. VDD_HSIC is the 1.2 V supply for the USB HSIC interface I/Os.
- VDD_USB33 and VDD_USB18 supply the USB PHY
- VDD_PTC supplies the I/Os on Port C (signals named PTC*nn*)
- VDD_PTD supplies the I/Os on Port D (signals named PTD*nn*)
- VDD_PTE supplies the I/Os on Port E (signals named PTE*nn*)
- VDD_PTF supplies the I/Os on Port F (signals named PTF*nn*).
- Power consumption of VDD_PTC, VDD_PTD, VDD_PTE, and VDD_PTF are completely application dependent and as such, measurements for these supplies are not included in this document. For an equation that can be used to estimate GPIO segment power based on the activity of the individual I/O signals, see the **Maximum Supply Currents** table in i.MX 7ULP Applications Processor - Consumer Products data sheet (document IMX7ULPCEC).

4.4 VBAT domain power supplies

VDD_VBAT42 supplies the VBAT Domain. In most applications, this supply will be provided by a battery. An internal LDO regulates the output to the 1.8 V used by the internal logic on the VBAT Domain. VDD_VBAT18_CAP is connected to an external capacitor. For decoupling and bulk capacitor requirements, see i.MX 7ULP Hardware Development Guide (document IMX7ULPHDG).

4.5 Analog and other supplies

The following supplies are used for analog and chip-level functions:

- VDD_ANA33 is a 3.3 V supply for analog functions.
- VDD_ANA18 is a 1.8 V supply for analog functions.
- VDD_PLL18 is a 1.8 V supply for the analog portions of the PLLs.
- VREFH_ANA18 is the voltage reference for the high end of the ADC range.
- VDD18_IOREF is a 1.8 V reference supply used by the I/Os.

4.6 Voltage levels and DVFS usage in measurement process

The voltage levels of all the supplies are set to the typical voltage levels as defined in i.MX 7ULP Hardware Development Guide (document IMX7ULPHDG) unless otherwise specified.

VDD_DIG0 and VDD_DIG1 may be changed to implement Dynamic Voltage and Frequency Scaling (DVFS) during the run time of the use cases to minimize power consumption in each power mode. For the voltage specifications for each of the power modes, see the **Recommended operating conditions** table in i.MX 7ULP Hardware Development Guide (document IMX7ULPHDG).

4.7 Temperature

The power measurements in this document were measured at room temperature (approximately 25 °C) unless otherwise specified.

4.8 Hardware and software used

The EVK includes 0 Ω resistors in various current paths that can be replaced with low impedance resistors to make current measurements. In addition, a specially designed EVK instrumented with power measurement capability was used for some measurements.

The software used for the active power measurements for the M4 and A7 cores and the GPUs is indicated in the tables containing the measurements.

5 Use cases and measurement results

For the purpose of this document, active power modes are those in which the chip components are active (powered and have clock running). Low power modes are those in which some circuitry may be clock-gated, power-gated or both. These modes provide much lower power consumption in exchange for more limited capability.

Low-power modes between the Real-Time Domain (M4 side) and the Application Domain (A7 side) are generally independent and can be entered/exited separately. There are some chip-level limitations for combinations of power modes between the Real-Time Domain and the Application Domain. For details on the low-power mode definitions and the allowed combinations, see the **Power Modes** section and the **Allowed power modes between multicore** section in i.MX 7ULP Applications Processor Reference Manual (document IMX7ULPRM).

5.1 Real-time domain low-power modes

Table 2 summarizes the low-power modes for the Real-Time Domain.

Table 2. M4 low-power modes

M4 Power mode	Description
STOP/VLPS (Very Low Power Stop)	• i.MX 7ULP is static state with all registers retained with maintaining LVD protection. • Peripherals optionally operational in STOP mode4. • RBB only allowed in VLPS mode. • FIRC enabled in VLPS mode via `SCG0_FIRCCSR` register. • LVDs could be turned off in VLPS mode.
LLS (Low Leakage Stop)	• Static mode with no active transition. • CM4 in WFI mode with core clock gated. • RBB allowed.
VLLS (Very Low Leakage Stop)	• M4 core supply OFF with majority of the logic power gated. • AWIC detects wake-up sources for M4 (via LLWU). • Selectable Memory retention (32/64/256 KB). • ADC, Comparators, LP Timers optionally functional. • RBB allowed (Optional). • DGO (aka Always ON) Logic Active. Only Peripherals in DGO domain (CMPx, LPTMRx) are functional. **NOTE** The M4 can only enter VLLS when the A7 is in VLLS or OFF. For details on the low-power mode definitions and the allowed combinations, see the **Power Modes** section and the **Allowed power modes between multicore** section in i.MX 7ULP Applications Processor Reference Manual (document IMX7ULPRM).

5.2 Application domain low-power modes

Table 3 summarizes the low-power modes for the Application Domain.

Table 3. A7 low-power modes

A7 Power mode	Description
OFF	• Application Domain supplies are unpowered. • LPDDR2/LPDDR3 supplies are unpowered.
STOP/VLPS (Very Low Power Stop)	• i.MX 7ULP is in static state with all registers retained with maintaining LVD protection. • RBB only allowed in VLPS mode. • FIRCCSR[FIRCLPEN] in the SCG module keeps FIRC enabled in VLPS mode. • LVDs could be turned off in VLPS mode.

Table continues on the next page...

Table 3. A7 low-power modes (continued)

A7 Power mode	Description
LLS (Low Leakage Stop)	• A7 supply ON. • RBB is allowed. • LVD protection. • I/O supplies ON. • A7 processor is in a wait-for-interrupt (WFI) state. The core clock is gated. • Bus and DMA clocks are gated. • All peripheral clocks are gated. • SRAM contents are retained. • External LPDDR2/LPDDR3 can be in self-refresh.
VLLS (Very Low Leakage Stop)	• A7 domain fully power gated. • Wake-up only via MU_A (CM4 domain) or reset. • External LPDDR2/LPDDR3 can be in self-refresh.

5.3 VBAT domain low-power mode

VBAT mode is a low-power mode on the i.MX 7ULP in which only the VBAT Domain is powered. VBAT mode is a chip-level state with the following conditions:

- All power supplies except `VDD_VBAT42` are off externally.
- `VDD_VBAT42` is on and within the voltage range specified in the i.MX 7ULP datasheet.
- The Secure Real-Time Clock (SRTC) is maintained and running.
- Tamper logic is retained.

VBAT mode represents the state where the application would be off and a battery would retain the SRTC and tamper logic.

5.3.1 Low-power mode power measurements

Table 4 shows power measurements for low-power modes under the following conditions:

- Typical silicon
- Room temperature
- Nominal supply voltages (as defined for each mode in i.MX 7ULP Applications Processor - Consumer Products data sheet (document IMX7ULPCEC)
- Software used
  - M4: The power_mode_switch demo in the MCU-SDK 2.5.1 software package
  - A7: The Linux kernel
- Hardware Platform: MCIMX7ULP-EVK

Table 4. Low-power mode power measurements

Test description	Total 7ULP SoC power (mW)
VBAT Mode A7 is powered OFF externally. M4 is powered OFF externally. VBAT domain maintained and operational. VDD_VBAT42 = 3.0 V Measured on Production Tester	0.007
A7-OFF / M4-VLLS A7 is powered OFF externally (VDD_DIG1 = 0 V). LPDDR3 powered OFF externally. M4 in VLLS mode (VDD_DIG0 = 0 V). TCM banks in retention mode (256 KB). VBAT domain maintained and operational. SoC can wake from GPIO or timer (based on 32 kHz clock). All GPIOs (except the wakeup GPIO) disabled: • IOMUXC0_SW_MUX_CTL_PAD_n = 0x00000000 • IOMUXC1_SW_MUX_CTL_PAD_n = 0x00000000 VDD_PTD = 0 V **NOTE** This test case cannot be measured on the EVK as designed. For details on the EVK modifications required for this test, see EVK modifications for A7-OFF/M4-VLLS test.	0.054
A7-VLLS / M4-VLLS A7 in VLLS mode (VDD_DIG1 = 0 V). LPDDR3 in self-refresh mode. M4 in VLLS mode (VDD_DIG0 = 0 V). TCM banks in retention mode (256 KB). Only VBAT domain maintained and operational. SoC can wake from GPIO or timer (based on 32 kHz clock). All GPIOs (except the wakeup GPIO) disabled: • IOMUXC0_SW_MUX_CTL_PAD_n = 0x00000000 • IOMUXC1_SW_MUX_CTL_PAD_n = 0x00000000 VDD_PTD = 0 V Measured on MCIMX7ULP-EVK	0.123

5.3.1.1 EVK modifications for A7-OFF/M4-VLLS test

According to i.MX 7ULP Applications Processor - Consumer Products data sheet (document IMX7ULPCEC), VDD_DIG1 must remain powered if the following supplies are powered: VDD_USB18, VDD_USB33, VDD_DSI18 and VDD_DSI11. If the USB and DSI supplies are not used/powered, VDD_DIG1 can be turned off at the board level.

On the EVK, the i.MX 7ULP VDD_USB33 supply is connected to the EVK VDD_3V3 rail, so to achieve lowest power consumption VDD_DIG1 and VDD_3V3 would need to be turned off.

VDD_3V3 is derived from EVK supply PMC_3V3 via a low enabled load switch. PTA25 is configured to output HIGH to disable the load switch. Driving PTA25 low turns off VDD_3V3. Power measurements on the i.MX 7ULP after the design of the EVK indicated that lower leakage power is achieved by leaving VDD_PTA/B/C/E/F powered instead of turning them off. VDD_PTD may be powered off.

To achieve lower power consumption, STANDBY_REQ was used instead of PTA25 to control the load switch. The EVK was modified to connect STANDYBY_REQ to PTA25, and PTA25 was configured as an input. STANDBY_REQ was chosen because it doesn't belong to a GPIO group; it is controlled by the SIM.

All other GPIOs were disabled by configuring IOMUXC0_SW_MUX_CTL_PAD_n to 0x00000000 and IOMUXC1_SW_MUX_CTL_PAD_n to 0x00000000.

5.3.2 Real-time domain (M4) active power measurements

Table 5 shows power measurements active power measurements for the Real-Time Domain under the following conditions:

- Typical silicon
- Room temperature
- Nominal supply voltages
- Real-Time Domain Software: SDK 2.5.1
- Application Domain Software: Linux 4.14.98-imx_4.14.98_2.0.0_g0bbe6f4e9b42
- Hardware Platform: MCIMX7ULP-EVK

Table 5. Real-Time Domain (M4) active power measurements

Test description	Total 7ULP SoC power (mW)
M4 Active – Low Performance – Execution from internal RAM A7 in VLLS mode M4 in VLPR mode (48 MHz) running Coremark from TCM	7.926
M4 Active – Normal Performance – Execution from internal RAM A7 in VLLS mode M4 in RUN mode (96 MHz) running Coremark from TCM	24.117
M4 Active – Low Performance – Execution from external QSPI NOR memory A7 in VLLS mode M4 in VLPR mode (48 MHz) running Coremark from QSPI	9.937
M4 Active – Normal Performance – Execution from external QSPI NOR memory A7 in VLLS mode M4 in RUN mode (96 MHz) running Coremark from QSPI	27.867

5.4 Application domain (A7) active power measurements

Table 6 shows power measurements active power measurements for the Application Domain under the following conditions:

- Typical silicon
- Room temperature
- Nominal supply voltages
- Real-Time Domain Software: SDK 2.5.1
- Application Domain Software: Linux 4.14.98-imx_4.14.98_2.0.0_g0bbe6f4e9b42
- Hardware Platform: MCIMX7ULP-EVK configured for MIPI display

Table 6. Application Domain (A7) active power measurements

Test description	Total 7ULP SoC power (mW)
A7 Active – Low Performance – Execution from external LPDDR3 – No graphics/ display A7 in RUN mode (500 MHz; VDD_DIG1 = 1.0 V) running STREAM core benchmark M4 in VLPS mode No GPU or display activity DVFS disabled LPDDR3 at 320 MHz	148.44
A7 Active – High Performance – Execution from external LPDDR3 – With 2D graphics/display A7 in RUN mode (500 MHz; VDD_DIG1 = 1.0 V) M4 in VLPS mode Running 2D effect with GLMARK2 benchmark DVFS disabled LPDDR3 at 320 MHz	190.84
A7 Active – High Performance – Execution from external LPDDR3 – With 3D graphics/display A7 in RUN mode (500 MHz; VDD_DIG1 = 1.0 V) M4 in VLPS mode Running 3D effect with GLMARK2 benchmark DVFS disabled LPDDR3 at 320 MHz	187.65

6 Minimizing power consumption

The overall system power consumption depends on both software optimization and how the system hardware is implemented. Below is a list of suggestions that may help reduce system power. Some of these are already implemented in Linux BSP and/or SDK. Further optimizations can be done on the individual user's system.

NOTE

Further power optimizations are planned for future software releases. See https://www.nxp.com/imxsw to obtain the latest software releases.

- Apply clock gating whenever clocks or modules are not used by configuring registers in the System Clock Generation (SCG) Module.
- For run modes, use the slowest frequency that will still support the application requirements.
- Reduce the number of operating PLLs whenever possible. Enabled PLLs can consume a few milliamps of current.
- Core DVFS and system bus scaling—Applying DVFS for the ARM cores and scaling the frequencies of the AXI, AHB, and IPG bus clocks can significantly reduce the power consumption. However, due to the reduced operation frequency, the accesses to the DDR take longer, which increases the power consumption of the DDR I/O and memories. This trade-off needs to be considered for each mode, to quantify the overall effect on system power.
- Put i.MX 7ULP into low power modes whenever possible and into the lowest power mode that will support the application requirements.
- For each operating mode, use the lowest voltage (with the power supply tolerance) that still meets the requirements of voltage specifications in i.MX 7ULP Applications Processor - Consumer Products data sheet (document IMX7ULPCEC).
- Reverse Body Bias (RBB) can be used to reduce power consumption in static low-power modes. For more details regarding RBB, see i.MX 7ULP Applications Processor Reference Manual (document IMX7ULPRM).
- DDR interface optimization:
  - Use careful board routing of the DDR memories, maintaining PCB trace lengths as short as possible.
  - Use the proper output driver impedance for DDR interface pins that provides good impedance matching. Select the lowest possible drive strength that provides the required performance, in order to save current through DDR I/O pins.
  - Set the i.MX 7ULP DDR interface pins High-Z when DDR memory is in Self-Refresh mode and keep `DDR_SDCKE0` and `DDR_SDCKE1` held low. If `DDR_SDCKE0` and `DDR_SDCKE1` are kept at low value by using external pull-down resistors, make sure there is no onboard termination on these pins during this mode.
  - If possible (depending on system stability), configure DDR input pins to CMOS mode, instead of Differential mode. This can be done by clearing the `DDR_INPUT` bit in the corresponding registers in IOMUXC. This setting is mostly recommended when operating at low frequencies.
  - Use of LPDDR2/LPDDR3 memory offerings in the latest process technology can significantly reduce the power consumption of the DDR devices and the DDR I/O.

7 Low-power design considerations for i.MX 7ULP

7.1 Designing power supply rails for power consumption

The i.MX 7ULP has multiple power supplies that operate at the same voltages as other components in the system. Power supply connections should be separated to accommodate the desired power to be measured current paths to be measured. The following list contains some considerations for power supply distribution:

- Power measurement can be performed by measuring the voltage across low impedance resistors placed in the desired current path, or by providing a connector for an ammeter. If resistors are used, the resistors should be placed in the correct locations to measure the desired current without including other system level currents. For example, the same 1.2 V power supply may be used to power I/Os on the LPDDR3 interface on the i.MX 7ULP and the I/Os of the external LPDDR3

DRAM itself. If it is desired to measure the current to the i.MX 7ULP only, the resistor should be placed such that the i.MX 7ULP current is the only current in that path. The LPDDR3 supply can be routed separately.

- If resistors are used for current measurement, the impedance value should be chosen carefully so the voltage drop during the peak expected current does not cause the supply voltage at the i.MX 7ULP to fall below the required specification in i.MX 7ULP Applications Processor - Consumer Products data sheet (document IMX7ULPCEC).
- If using an external ammeter, caution must be taken with respect to cable length/resistance mainly on power rails that require high speed switching. Measurements must be taken prior to bulk/bypass capacitor to avoid any inductance in series that may cause voltage to drop.
- The i.MX 7ULP has some power supply connections that must be connected (as specified in i.MX 7ULP Applications Processor - Consumer Products data sheet (document IMX7ULPCEC). There is no benefit to providing the ability to measure the power on these supplies separately because they will always be combined. The affected power supplies are listed below:
  - VDD_PMC18, VDD18_IOREF and VDD_PTB are connected internally to the i.MX 7ULP and, as such, must be driven from the same 1.8 V source.
  - If VDD_PMC18_DIG0 is operated at 1.8 V, it should be tied to VDD_PMC18 at the board level.
  - VDD_ANA33 must be shorted to VDD_PTA at the board level.
  - If the MIPI DSI is used, VDD_DSI11 must be connected to VDD_DIG1 at board level.
- Load switches can be included at the system level to turn on/off some power supplies as required for M4-VLLS mode, A7-VLLS mode and A7-OFF mode. For details on which supplies can be turned off, see Table 7.

7.2 Controlling i.MX 7ULP power supplies in the lowest power modes

Many applications will use the M4-VLLS/A7-VLLS or M4-VLLS/A7-OFF power mode combinations to minimize power when the application is a standby state. These are the lowest power combinations on the i.MX 7ULP. To minimize power consumption, the I/O voltage supplies VDD_PTA, VDD_PTB, VDD_PTC, VDD_PTE and VDD_PTF must remain powered.

Table 7 shows the power supply configuration to minimize power consumption in these modes.

Table 7. Power supply configuration to minimize power in VLLS modes

Power Domain	M4-VLLS/A7-VLLS	M4-VLLS/A7-OFF
VDD_ANA18	ON	ON
VDD_ANA33	ON	ON
VDD_DDR	ON	OFF
VDD_DIG1	OFF	OFF
VDD_DSI11	OFF	OFF
VDD_DSI18	OFF	OFF
VDD_HSIC	OFF	OFF
VDD_PLL18	ON	ON
VDD_PMC12_DIG1	OFF	OFF
VDD_PMC18	ON	ON
VDD_PMC18_DIG0	ON	ON
VDD_PTA	ON	ON

Table continues on the next page...

Table 7. Power supply configuration to minimize power in VLLS modes (continued)

Power Domain	M4-VLLS/A7-VLLS	M4-VLLS/A7-OFF
VDD_PTB	ON	ON
VDD_PTC	ON	ON
VDD_PTD	OFF	OFF
VDD_PTE	ON	ON
VDD_PTF	ON	ON
VDD_USB18	OFF	OFF
VDD_USB33	OFF	OFF
VDD_VBAT42	ON	ON
VDD18_DDR	ON	OFF
VDD18_IOREF	ON	ON
VREFH_ANA18	ON	ON

7.2.1 M4-VLLS/A7-VLLS power distribution using PF1550 PMIC

The PF1550 is a PMIC specifically design for use with the i.MX 7ULP. For details on the PF1550, see the PF1550 product page on https://www.nxp.com.

Figure 2 shows an example power distribution using the PF1550 PMIC for the M4-VLLS/A7-VLLS power configuration.

The following conditions must be used for minimum power consumption in this configuration:

- Power PF1550 via the VBATT pin and use LDO2 to enable the load switch.
- Only `VLDO1_STBY_EN`, `VLDO3_STBY_EN`, `SW2_STBY_EN` and `SW3_STBY_EN` bits are set to **1**. Other `xxx_STBY_EN` bits are 0.
- `VLDO1_LPWR`, `VLDO3_LPWR`, `SW2_LPWR` and `SW3_LPWR` bits are set to **1**. Doing so forces LDO1/3 and SW2/3 into low-power mode in Sleep and Standby modes.
- Turn off SW1 and LDO2 after the A7 enters VLLS mode.
- Toggle `PMIC_STANDBY_REQ` from **0** to **1** to allow the PMIC to enter standby mode before M4 enters VLLS mode.

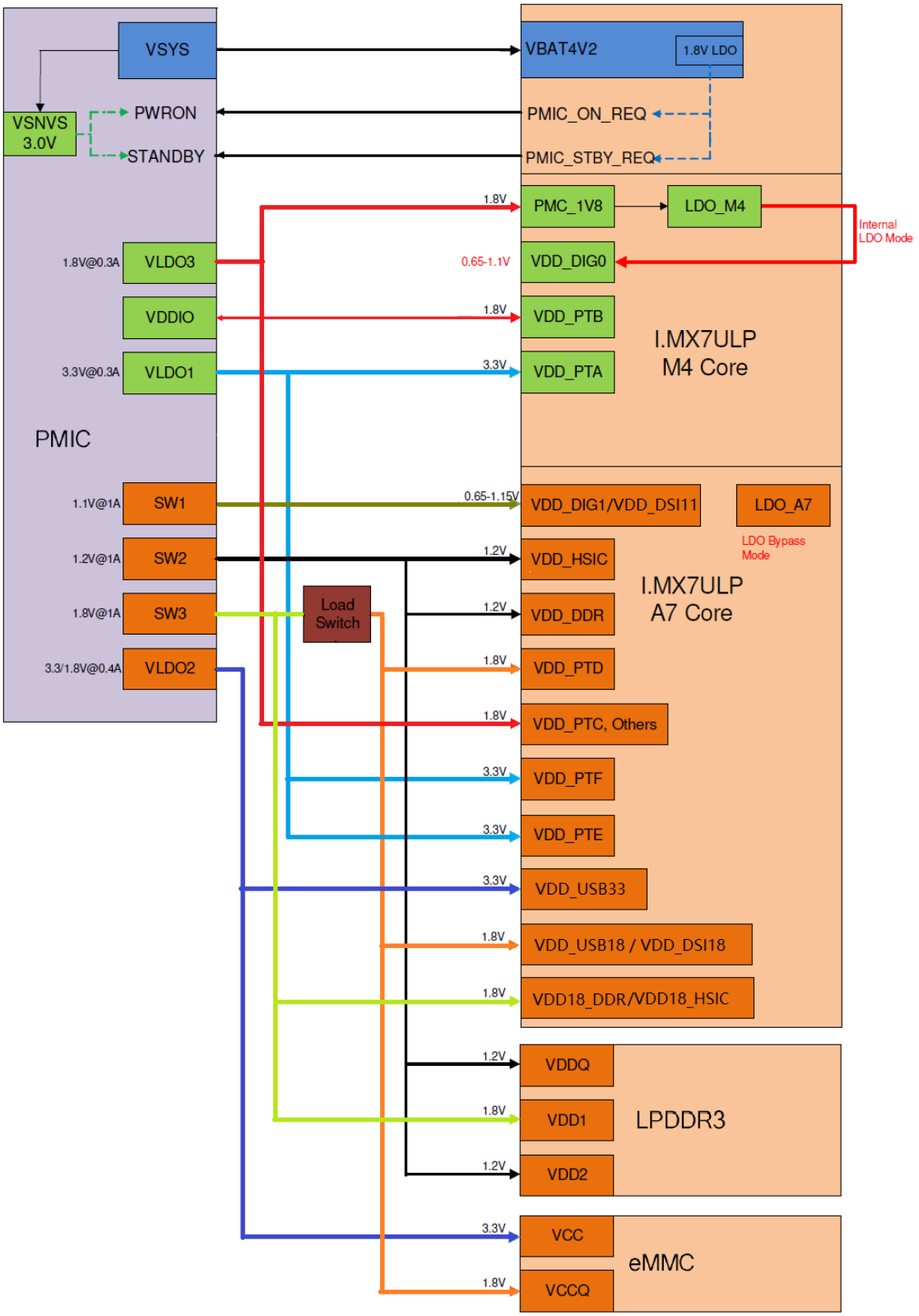

Figure 2. i.MX 7ULP power distribution with PF1550 PMIC for M4-VLLS/A7-VLLS

7.2.2 M4-VLLS/A7-OFF power distribution using PF1550 PMIC

Figure 3 shows an example power distribution using the PF1550 PMIC for the M4-VLLS/A7-OFF power configuration.

The following conditions must be used for minimum power consumption in this configuration:

- Power PF1550 via the VBATT pin
- Only `VLDO1_STBY_EN` and `VLDO3_STBY_EN` bits are set to 1. Other `xxx_STBY_EN` bits are **0**.
- `VLDO1_LPWR` and `VLDO3_LPWR` bits are set to 1. Doing so, forces LDO1/3 to low-power mode in Sleep and Standby modes.
- Turn SW1, SW2, SW3 and LDO2 off after the A7 enters OFF mode.
- Toggle `PMIC_STANDBY_REQ` from **0** to **1** to allow the PMIC to enter standby mode before M4 enters VLLS mode.

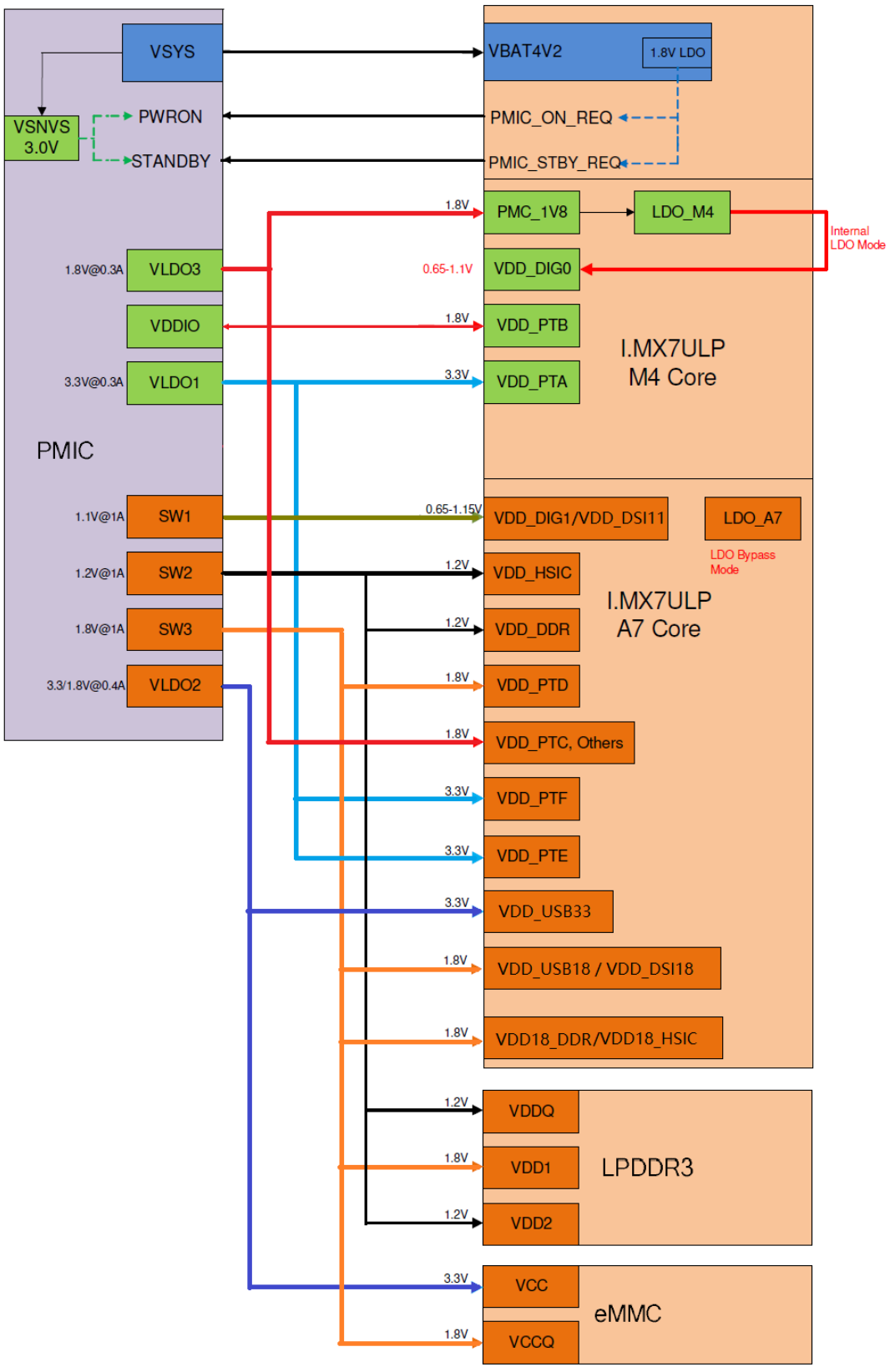

Figure 3. i.MX 7ULP power distribution with PF1550 PMIC for M4-VLLS/A7-OFF

7.3 On-chip LDO regulator modes

The i.MX 7ULP provides on-chip LDO regulators to support DVFS on the M4 core and the A7 core. The M4 core always uses the internal LDO to provide power to the core logic in the Real-Time Domain. The A7 core can use the internal LDO (LDO Enabled mode) or use an external variable power supply (A7 LDO Bypass mode) to provide power to the core logic in the Application Domain. There are board design implications to choosing A7 LDO Enabled mode versus LDO Bypass mode as described in the following sections.

On the i.MX 7ULP, power supplies with the naming convention **DIG0** are associated with the core logic in the Real-Time Domain and power supplies with the naming convention **DIG1** are associated with the core logic in the Application Domain.

7.3.1 M4 LDO enabled mode

The M4 LDO only supports LDO Enabled mode. The input of the M4 LDO is powered via VDD_PMC18_DIG0. VDD_PMC18_DIG0 can be powered at 1.8 V nominal or 1.2 V nominal. M4 HSRUN mode is not supported when the VDD_PMC18_DIG0 is operated at 1.2 V nominal. See the supply voltage requirements in the **Recommended operating conditions-system** section in i.MX 7ULP Applications Processor - Consumer Products data sheet (document IMX7ULPCEC).

The LDO output is VDD_PMC11_DIG0_CAP. An external capacitor is required at the board-level on VDD_PMC11_DIG0_CAP. For decoupling and bulk capacitor requirements, see i.MX 7ULP Hardware Development Guide (document IMX7ULPHDG).

VDD_PMC11_DIG0_CAP is then connected back to VDD_DIG0. This connection has maximum impedance requirements (see the product datasheet parameter RDIG0).

Figure 4 shows the required board connections for the M4 LDO.

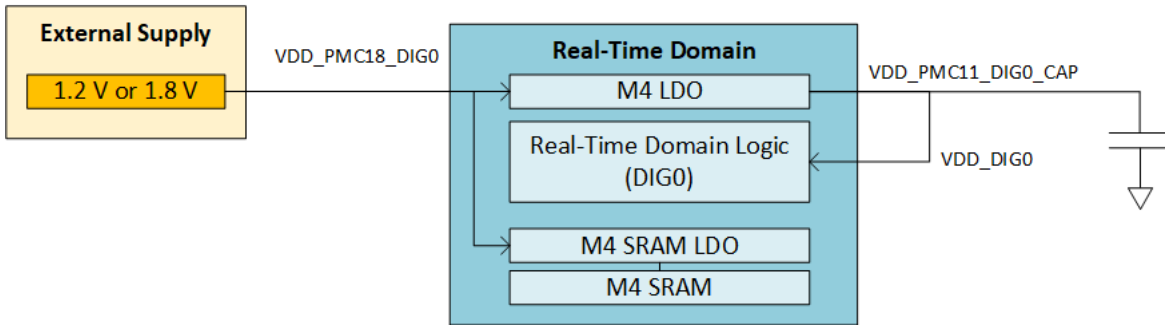

Figure 4. M4 LDO enabled mode board-level power supply connections

7.3.2 A7 LDO enabled mode

The A7 LDO can be operated in LDO Enabled Mode or LDO Bypass Mode. The board-level connections for each mode are different. A7 LDO Enabled Mode allows control of DVFS internally by software programming of the A7 LDO output voltage. This configuration is useful when an external PMIC is not desired (such as a power supply implementation with discrete components) or the external power supply cannot provide a variable voltage.

NOTE

A7 HSRUN mode is not supported in A7 LDO Enabled Mode. See the supply voltage requirements in the **Recommended operating conditions-system** section in i.MX 7ULP Applications Processor - Consumer Products data sheet (document IMX7ULPCEC).

In A7 LDO Enabled Mode, the input of the A7 LDO is powered via VDD_PMC12_DIG1. The LDO output is VDD_PMC11_DIG1_CAP. An external capacitor is required at the board-level on VDD_PMC11_DIG1_CAP. For decoupling and bulk capacitor requirements, see i.MX 7ULP Hardware Development Guide (document IMX7ULPHDG).

VDD_PMC11_DIG1_CAP is connected to VDD_DIG1. This connection has maximum impedance requirements (see the product datasheet parameter RDIG1).

Figure 5 shows the required board connections for the A7 LDO enabled mode configuration.

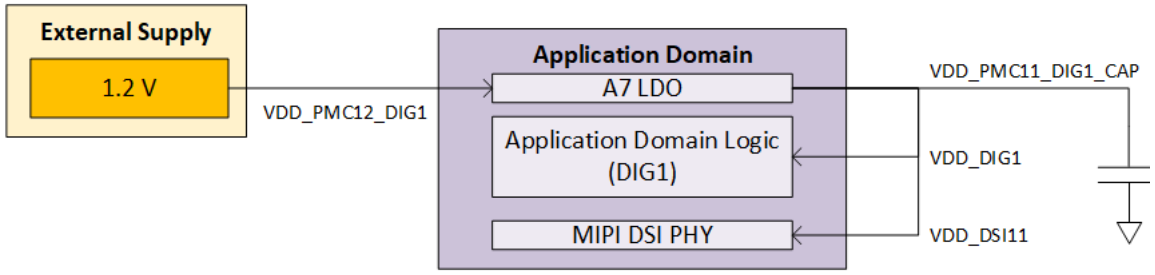

Figure 5. A7 LDO enabled mode board-level power supply connections

7.3.3 A7 LDO bypass mode

In A7 LDO Bypass Mode, the Application Domain core logic voltage is controlled externally (usually by a PMIC) and the internal A7 LDO is disabled. This configuration is preferable when a PMIC is present to provide a variable voltage for the Application Domain logic.

Since the load on A7 is high under maximum performance conditions, using an external regulated supply provides overall higher power efficiency compared to using A7 LDO Enabled mode, especially for scenarios where the Application Domain is running at lower voltages.

HSRUN mode on the A7 is supported in A7 LDO Enabled Mode. See the supply voltage requirements in the **Recommended operating conditions-system** section in i.MX 7ULP Applications Processor - Consumer Products data sheet (document IMX7ULPCEC).

In A7 LDO Enabled Mode, VDD_PMC12_DIG1, VDD_PMC11_DIG1_CAP and VDD_DIG1 are all connected at the board-level.

Figure 6 shows the required board connections for the A7 LDO Enabled Mode configuration.

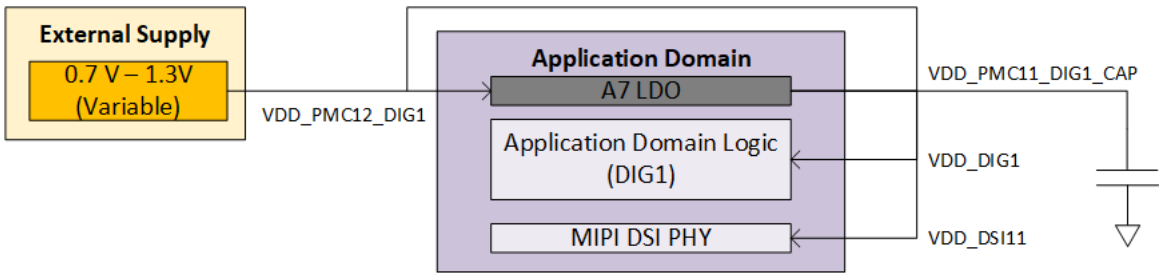

Figure 6. A7 LDO bypass mode board-level power supply connections

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

While NXP has implemented advanced security features, all products may be subject to unidentified vulnerabilities. Customers are responsible for the design and operation of their applications and products to reduce the effect of these vulnerabilities on customer’s applications and products, and NXP accepts no liability for any vulnerability that is discovered. Customers should implement appropriate design and operating safeguards to minimize the risks associated with their applications and products.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: September 2019
Document identifier: AN12573

arm