1 Introduction

1.1 Purpose
This application note introduces the major considerations required to migrate from i.MX 8X B0 to i.MX 8X C0, including i.MX 8QuadXPlus, i.MX 8DualXPlus, and i.MX 8DualX.

To distinguish between i.MX 8X B0 and i.MX 8X C0 parts, users can check the last letter of the part number, which indicates the silicon reversion. For example, MiMX8QX6AVLFZAB indicates that it is i.MX 8X B0 part, while MiMX8QX6AVLFZAC indicating that it is i.MX 8X C0 part.

1.2 Scope
The i.MX 8X C0 fixes most of the errata that are reported on i.MX 8X B0. The major changes include:

- **Imaging/ISI**: The same functionality as B0 with optimization on the image stream flow control and performance improvement. Bug fixes to enhance the IP and system use case operating quality.

- **DRC**: Bug fixes for derating logic and shorten the ECC boot time.

- **DPLL**: Bug fixes to resolve the pll lock issue at cold temperature and some other issues. Programming sequence changed.

- **DB**: Bug fix for TDM QoS mechanism is broken when HW clock gating is enabled.

- **SCU**: Several bug fixes. Add the ability to wake up from the SNVS ON/OFF key in KS1(LLS), Improve SNVS startup time on LDO.

- **DC**: Bug fixes for PRG on the fly bypass switch issue.

- **GPU**: Fix OpenCV and Vulkan conformance issues.

- **VPU**: Enhancement for encoder and decoder using different reset signal

- **MIPI_CSI**: Several enhancements, including align RAW8 format in MIPI_CSI reformatter with ISI.

- **MIPI_DSI**: Bug fixes to resolve MIPI DSI CRC issue for LP DCS long write.

- **USB**: Several bug fixes, including fix for ISO out queue issue.

- **TOP**: Several bug fixes, including fix for display write-back feature.

- **ROM**: Several bug fixes, including reset SECO timer if SD/MMC initialization takes too long.

For a detailed description of the complete change list, see Chapter 2.2 “Change list” below.

1.3 Audience
This document is intended for system integrators and software developers migrating from the platforms based on i.MX 8X B0 to i.MX 8X C0.

2 Feature Change Summary
## 2.1 BSP support
The i.MX 8X C0 is now supported by the L4.14.98_2.3.0 BSP release.

## 2.2 Change list
This section summarizes the changes of the i.MX 8X C0 with respect to the i.MX 8X B0.

### Table 1. Changes List of i.MX 8X C0

<table>
<thead>
<tr>
<th>Subsystem</th>
<th>Changes/Issue fixed in C0</th>
<th>Related Errata/Enhancement</th>
<th>SW migration impact</th>
<th>HW migration impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>Imaging/ISI</td>
<td>ISI stream flow control problem. ISI does not have any built-in mechanism for controlling the AXI transaction frequency</td>
<td>e50066</td>
<td>Driver update</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td>ISI Virtual channel issue with 4 camera, 4 cameras cannot be supported well</td>
<td>e50058</td>
<td>Driver update</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td>When ISI is programmed to do scaler on 2 adjacent channels, image on the second channel is corrupted. There are some empty lines inserted every 16 lines.</td>
<td>e50067</td>
<td>Driver update</td>
<td>None</td>
</tr>
<tr>
<td>DRC</td>
<td>DDR3 ECC boot time over 50 ms. This issue does not meet auto customer application requirement for DDR3 ECC boot.</td>
<td>e50054</td>
<td>SCFW (dcd) update</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td>Derating logic does not Consider the System Temperature when Derating is Enabled</td>
<td>e50125</td>
<td>SCFW (dcd) update</td>
<td>None</td>
</tr>
<tr>
<td>DPLL</td>
<td>At cold temperatures, the DPLL does not lock for some parts. Switch DPLL phase detector to a phase frequency hybrid structure. Saturation logic broken in DPLL integrator preventing reset and lock if saturated.</td>
<td>e50061</td>
<td>SCFW update</td>
<td>None</td>
</tr>
<tr>
<td>SCU</td>
<td>SNVS startup on LDO is too slow 1)SNVS_ANA LDO regulator fix 2) The VBAT_POR_B signal, which is the SNVS DGO domain reset, is included in the logic which provides the POR signal to the DSC.</td>
<td>e50056</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>DC</td>
<td>PRG on the fly bypass switch issue. De-rate the PRG AXI channel clock from 400 MHz to 375 MHz to meet the STA of the ECO.</td>
<td>e50060</td>
<td>SCFW update</td>
<td>None</td>
</tr>
<tr>
<td>GPU</td>
<td>OpenCV and Vulkan conformance issue. Modified the GPU revision number for SW identification</td>
<td>e50057</td>
<td>Driver update</td>
<td>None</td>
</tr>
<tr>
<td>VPU</td>
<td>VPU encoder and decoder use different reset signal from DSC in different power domain.</td>
<td>enhancement</td>
<td>SCFW update</td>
<td>None</td>
</tr>
<tr>
<td>MIPI_CSI</td>
<td>CSI generates the ODD/EVEN signal according to the incoming start of frame package.</td>
<td>enhancement</td>
<td>Driver update</td>
<td>None</td>
</tr>
</tbody>
</table>

*Table continues on the next page...*
### Table 1. Changes List of i.MX 8X C0 (continued)

<table>
<thead>
<tr>
<th>Category</th>
<th>Description</th>
<th>Related Issue No.</th>
<th>Driver Update</th>
<th>HW Migration Impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIPI_DSI</td>
<td>MIPI DSI CRC issue for LP DCS long write</td>
<td>e11439</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>Connectivity</td>
<td>NXP USB2 ISO OUT issue in device mode.</td>
<td>e50141</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td>USB3: Multiple DMA write transfer complete interrupts are generated before final write access handshake to the AXI bus</td>
<td>e50147</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td>USB3: TRB OUT endpoints transfer blockage and performance delays</td>
<td>e50149</td>
<td>Driver Update</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td>USB3: Port Configuration Response is not compliant with the USB compliance TD 7.17 test case</td>
<td>e50115</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>Top</td>
<td>The impact of the temperature sensor turning on and off in its normal operation couples and corrupts other analog blocks through top-level metal coupling.</td>
<td>e50055</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td>Display write back feature is broken due to the pixel link receiver address tied-off. With this fix, application can allocate the write-back to different LVDS.</td>
<td>e50059</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td></td>
<td>Chip ID need to be a new value for C0 rev. by updating the JTAG ID for C0 as 0x2890201D</td>
<td>N/A</td>
<td>Driver &amp; SCFW update</td>
<td>None</td>
</tr>
</tbody>
</table>

### Table 2. Changes List of i.MX 8X C0 ROM

<table>
<thead>
<tr>
<th>Related Errata/Enhancement</th>
<th>Changes/Issue fixed in C0</th>
<th>SW migration impact</th>
<th>HW migration impact</th>
</tr>
</thead>
<tbody>
<tr>
<td>e50108</td>
<td>Reset SECO timer if SD/MMC initialization taking too much time to fix boot failure issue</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>e50052</td>
<td>NAND boot fails when image header points to an unprogrammed block</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>e50053</td>
<td>USB HID device cannot be re-enumerated successfully after an unplug/plug USB cable operation</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>Enhancement</td>
<td>Support boot image provisioned by boot partitions for eMMC regular boot, no 32k gpt offset</td>
<td>Driver update</td>
<td>None</td>
</tr>
<tr>
<td>Enhancement</td>
<td>Using CM4 self-reset to issue warm reset instead of WDOG reset</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>Enhancement</td>
<td>Update DPLL lock sequence</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>N/A</td>
<td>Update SCU ROM version to 1.3</td>
<td>SCFW update</td>
<td>None</td>
</tr>
</tbody>
</table>
2.3 Software changes

For software changes to bring up i.MX 8X C0, the main aspects are listed below. However, the driver update for all modules in the change list is not included here. It will be included in the BSP release L4.14.98_2.3.0.

For other unchanged parts, see i.MX 8X Linux User Guide for more details.

- SCFW
  
  Use SCFW Porting Kit 1.3.0 and later version.
  
  Compile the SCFW with “R=b0” option, it will dynamically supports i.MX 8X B0/C0.

- SECO FW
  
  Use the SECO FW v2.5.4 for C0 and later version.

  **NOTE**
  
  The SECO FW has two separated version for i.MX 8X B0 and C0, naming as “mx8qxb0-ahab-container.img” and “mx8qxc0-ahab-container.img”, use the one for C0.

- U-boot
  
  Two patches are needed based on L4.14.98_2.0.0_ga version

  1. [PATCH] MLK-22711-1 show RevC instead of Rev? at boot log
     
     Add REVC information.

     Signed-off-by: Frank Li <Frank.Li@nxp.com>

     ---
     
     arch/arm/include/asm/arch-imx/cpu.h | 1 +
     arch/arm/mach-imx/imx8/cpu.c | 2 ++
     2 files changed, 3 insertions(+)
     
     diff --git a/arch/arm/include/asm/arch-imx/cpu.h b/arch/arm/include/asm/arch-imx/cpu.h
     index 05d48f6..ae5d02f 100644
     --- a/arch/arm/include/asm/arch-imx/cpu.h
     +++ b/arch/arm/include/asm/arch-imx/cpu.h
     @@ -67,6 +67,7 @@
     #define CHIP_REV_A 0x0
     #define CHIP_REV_B 0x1
     +#define CHIP_REV_C 0x2
     #define BOARD_REV_1_0 0x0
     #define BOARD_REV_2_0 0x1
     
     diff --git a/arch/arm/mach-imx/imx8/cpu.c b/arch/arm/mach-imx/imx8/cpu.c
     index 2f4af58..2cda814 100644
     --- a/arch/arm/mach-imx/imx8/cpu.c
     +++ b/arch/arm/mach-imx/imx8/cpu.c
     @@ -81,6 +81,8 @@
     return "A";
     case CHIP_REV_B:
return "B";
+ case CHIP_REV_C:
+ return "C";
default:
return "?";
}
--

2. [PATCH] MLK-22711-2: fastboot: emmc: update bootloader to offset 0
   for RevC QXP chip
   ROM update emmc offset to 0.
   previous B0 is 32K.
   Signed-off-by: Frank Li <Frank.Li@nxp.com>
---
drivers/usb/gadget/f_fastboot.c | 2 +-
1 file changed, 1 insertion(+), 1 deletion(-)
diff --git a/drivers/usb/gadget/f_fastboot.c b/drivers/usb/gadget/f_fastboot.c
index df8b537..eb1a06d 100644
--- a/drivers/usb/gadget/f_fastboot.c
+++ b/drivers/usb/gadget/f_fastboot.c
@@ -797,7 +797,7 @@ static ulong bootloader_mmc_offset(void)
{ 
  if (is_imx8mq() || is_imx8mm() || (is_imx8() && is_soc_rev(CHIP_REV_A)))
    return 0x8400;
- else if (is_imx8qm()) {
+ else if (is_imx8qm() || (is_imx8qxp() && !is_soc_rev(CHIP_REV_B))) {
    if (MEK_8QM_EMMC == fastboot_devinfo.dev_id)
      /* target device is eMMC boot0 partition, bootloader offset is 0x0 */
      return 0x0;
--

• Linux Kernel
  No changes base on L4.14.98_2.0.0_ga version
• Release
  Currently i.MX 8QuadXPlus C0 BSP release L4.14.98_2.3.0 is available under following link:
  https://www.nxp.com/webapp/Download?colCode=L4.14.98_2.3.0_MX8QXP&appType=license
  Find the release note under following link:
2.4 Hardware changes
No hardware changes for i.MX 8X C0 migration.

3 Revision history

<table>
<thead>
<tr>
<th>Revision number</th>
<th>Date</th>
<th>Substantive changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>03/2020</td>
<td>Initial release</td>
</tr>
</tbody>
</table>
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