AN12853

i.MX ROMs Log Events

Rev. 0 — May 2020

Application Note

Contents

1 Introduction

1.1 Scope

ROM events are defined for ROM debug purpose. When the ROM code executes to a significant node, a specific ROM event is recorded in the ROM event log buffer. Events are captured in the ROM log buffer for every boot attempt, success or fail. This provides the developer with a snapshot of the ROM boot process for analysis.

This document describes the details of ROM log events for i.MX6/7/8 series ROM. The previous ROM project, earlier than i.MX6, is not included in this document.

1.2 Glossary

This section describes the terms and acronyms required to interpret this document.

Table 1. Glossary

Term	Definition
ROM event	Identifies a specific point in ROM boot processing, to show the ROM boot related information. For example, which boot mode ROM is retrieved from fuses or GPIOs, which boot device is used for this boot try, is boot device initialization complete, is loading data from boot device complete, does boot image authentication pass, and so on.
ROM event log buffer	A section or several sections (for some devices) in RAM where ROM events are logged.

2 ROM events

2.1 ROM event entry

The ROM event entries are saved in ROM event log buffer. One single ROM event entry consist of ROM event ID and its parameters:

Table 2. A ROM event entry

Offset	Bits [31:0]
0x0	ROM event ID
0x4	Parameter0 (Optional, available for some events)

Table continues on the next page...

Table 2. A ROM event entry (continued)

Offset	Bits [31:0]
0x8	Parameter1 (Optional, available for some events)
0xC	Parameter2 (Optional, available for some events)

2.2 ROM event ID format

There are two versions of ROM event ID formats:

Table 3. ROM event format version

ROM event ID format versions	User
ROM event ID format version 0	i.MX6 series
ROM event ID format version 1	i.MX 7D, i.MX 7ULT, i.MX 8QM series, and i.MX mSCALE series.

2.2.1 ROM event ID format version 0

Table 4. ROM event format version 0

Bits 31-24	Bits 23-0
Reserved	Log event ID

2.2.2 ROM event ID format version 1

Table 5. ROM event format version 1

Bits 31-24	Bits 23-0
Log event ID	Reserved

2.3 ROM event ID definitions

Table 6. ROM event ID definition version

ROM event ID definition versions	ROM event ID format	User
ROM event ID definition version 0	ROM event ID format version 0	i.MX6 series.
ROM event ID definition version 1	ROM event ID format version 1	i.MX 7D and i.MX 7ULT
ROM event ID definition version 2	ROM event ID format version 1	mSCALE series
ROM event ID definition version 3	ROM event ID format version 1	i.MX 8QM B0, i.MX8 QXP B0, i.MX 8DXL

2.3.1 ROM event ID definition version 0

The ROM event IDs used in i.MX6 series are as follows.

Table 7. ROM event ID definition version 0

ID	Description	Parameters
0x010000	Boot mode is Boot from Fuse	—
0x010001	Boot mode is Serial Download	—
0x010002	Boot mode is Internal Boot	—
0x010003	Boot mode is Test Mode	—
0x020000	Secure config is FAB	—
0x020033	Secure config is Field Return	—
0x0200F0	Secure config is Open	—
0x0200CC	Secure config is Closed	—
0x030000	Internal use	—
0x030001	Internal use	—
0x040000	FUSE_SEL_VALUE Fuse is not blown	—
0x040001	FUSE_SEL_VALUE Fuse is blown	—
0x050000	Boot from the primary boot image	—
0x050001	Boot from the secondary boot image	—
0x060000	Primary boot from RAW NAND device	—
0x060001	Primary boot from SD or EMMC device	—
0x060003	Primary boot from I2C EEPROM device	—
0x060004	Primary boot from ECSPI NOR device	—
0x060005	Primary boot from WEIM NOR device	—
0x060006	Primary boot from one NAND device	—
0x060007	Primary boot from QSPI NOR device	—
0x061003	Recovery boot from I2C EEPROM device	—
0x061004	Recovery boot from EXSPI NOR device	—
0x061FFF	No recovery boot device	—
0x062001	Manufacture boot from SD or EMMC	—

Table continues on the next page...

Table 7. ROM event ID definition version 0 (continued)

ID	Description	Parameters
0x070000	Start to perform the device initialization	—
0x0700F0	The boot device initialization completes	—
0x070033	The boot device initialization fails	—
0x080000	Start to read data from boot device	Parameter0: image offset
0x0800F0	Reading data from boot device completes	—
0x080033	Reading data from boot device fails	—
0x090000	Image authentication result	Parameter0: Authentication result Bit[7:0] == 0xF0: Authentication pass
0x0A0000	Start to execute the plugin program	Parameter0: the entry point of plugin image
0x0A00F0	The plugin program returns success	—
0x0A0033	The plugin program returns failure	—
0x0B0000	Jump to the boot image soon	Parameter0: the entry point of boot image
0x0C0000	Enters serial download processing	—
0x0D0000	Jump to the SDP boot image soon	Parameter0: the entry point of boot image
0x0E0000	Internal use	—

2.3.2 ROM event ID definition version 1

The ROM event IDs used in i.MX 7D and i.MX 7ULP series are as follows.

Table 8. ROM event ID definition version 1

ID	Description	Parameters
0x10	Boot mode is Boot from Fuse	—
0x11	Boot mode is Serial Download	—
0x12	Boot mode is Internal Boot	—
0x13	Boot mode is Test mode	—
0x18	Low Power mode selected (7ULP only)	—
0x19	Dual Boot mode selected (7ULP only)	—
0x1A	Single Boot mode selected (7ULP only)	—

Table continues on the next page...

Table 8. ROM event ID definition version 1 (continued)

ID	Description	Parameters
0x20	Secure config is FAB	—
0x21	Secure config is Field Return	—
0x22	Secure config is Open	—
0x23	Secure config is Closed	—
0x30	Internal use	—
0x31	Internal use	—
0x40	FUSE_SEL_VALUE Fuse is not blown	—
0x41	FUSE_SEL_VALUE Fuse is blown	—
0x50	Boot from the primary boot image	—
0x51	Boot from the secondary boot image	—
0x60	Primary boot from RAW NAND device	—
0x61	Primary boot from SD or EMMC device	—
0x63	Primary boot from I2C EEPROM device	—
0x64	Primary boot from ECSPI NOR device	—
0x65	Primary boot from WEIM NOR device	—
0x66	Primary boot from One NAND device	—
0x67	Primary boot from QSPI NOR device	—
0x70	Recovery boot from I2C EEPROM device	—
0x71	Recovery boot from EXSPI NOR device	—
0x72	No recovery boot device	—
0x73	Manufacture boot from SD or EMMC	—
0x80	Start to perform the device initialization	Parameter0: Time tick
0x81	The boot device initialization completes	Parameter0: Time tick
0x8F	The boot device initialization fails	Parameter0: Time tick
0x90	Start to read data from boot device	Parameter0: Image offset

Table continues on the next page...

Table 8. ROM event ID definition version 1 (continued)

ID	Description	Parameters
0x91	Reading data from boot device completes	Parameter0: Time tick
0x9F	Reading data from boot device fails	Parameter0: Time tick
0xA0	Image authentication result	Parameter0: Authentication result Bit[7:0] == 0xF0: Authentication pass Parameter1: Time tick
0xB0	Start to execute the plugin program	Parameter0: The entry point of plugin image Parameter1: Time tick
0xB1	The plugin program returns success	—
0xBF	The plugin program returns failure	—
0xC0	Jump to the boot image soon	Parameter0: The entry point of boot image Parameter1: Time tick
0xD0	Enters serial download processing	—
0xD1	Jump to the SDP boot image soon	Parameter0: The entry point of boot image Parameter1: Time tick
0xD8	Get CM4 FW entry from persistent register (7ULP only)	Parameter0: The entry point of CM4 FW Parameter1: Time tick
0xE0	Internal use	—
0xF0	Enters ROM exception handler (7ULP only)	—
0xF1	NMI occurs (7ULP only)	—

2.3.3 ROM event ID definition version 2

The ROM event IDs used in mSCALE series are as follows.

Table 9. ROM event ID definition version 2

ID	Description	Parameters
0x01	ROM event version, bit[7:0] is version	—
0x10	Boot mode is Boot from Fuse	—
0x11	Boot mode is Serial Download	—
0x12	Boot mode is Internal Boot	—

Table continues on the next page...

Table 9. ROM event ID definition version 2 (continued)

ID	Description	Parameters
0x13	Boot mode is Test Mode	—
0x20	Secure config is FAB	—
0x21	Secure config is Field Return	—
0x22	Secure config is Open	—
0x23	Secure config is Closed	—
0x30	Internal use	—
0x31	Internal use	—
0x40	FUSE_SEL_VALUE Fuse is not blown	—
0x41	FUSE_SEL_VALUE Fuse is blown	—
0x50	Boot from the primary boot image	—
0x51	Boot from the secondary boot image	—
0x60	Primary boot from RAW NAND device	—
0x61	Primary boot from SD or EMMC device	—
0x64	Primary boot from ECSPI NOR device	—
0x67	Primary boot from QSPI NOR device	—
0x71	Recovery boot from EXSPI NOR device	—
0x72	No Recovery boot device	—
0x73	Manufacture boot from SD or EMMC	—
0x74	Primary boot from SPI NAND device	—
0x80	Start to perform the device initialization	Parameter0: Time tick
0x81	The boot device initialization completes	Parameter0: Time tick
0x82	Starts to execute boot device driver pre-config	—
0x83	Boot device driver pre-config completes	—
0x8E	Boot device driver pre-config fails	—

Table continues on the next page...

Table 9. ROM event ID definition version 2 (continued)

ID	Description	Parameters
0x8F	The boot device initialization fails	Parameter0: Time tick
0x90	Start to read data from boot device	Parameter0: Image offset
0x91	Reading data from boot device completes	Parameter0: Time tick
0x9F	Reading data from boot device fails	Parameter0: Time tick
0xA0	Image authentication result	Parameter0: Authentication result Bit[7:0] == 0xF0: Authentication pass Parameter1: Time tick
0xA1	IVT header is not valid	—
0xC0	Jump to the boot image soon	Parameter0: The entry point of boot image Parameter1: Time tick
0xD0	Enters serial download processing	—
0xE0	Internal use	—
0xF0	Enters ROM exception handler	—

2.3.4 ROM event ID definition version 3

The ROM event IDs used in i.MX 8QM B0, i.MX 8QXP B0, and i.MX 8DXL series are as follows.

Table 10. ROM event ID definition version 3

ID	Description	Parameters
0x01	ROM event version, bit[7:0] is version	—
0x02	Setup the boot device driver fails	—
0x03	Handling the first 8 KB data of boot image fails	—
0x04	Handling the boot image fails	—
0x0F	Enters ROM error handling	Parameter0: Current boot stage
0x10	Boot mode is Boot from Fuse	—
0x11	Boot mode is Serial Download	—
0x12	Boot mode is Internal Boot	—
0x13	Boot mode is Test mode	—

Table continues on the next page...

Table 10. ROM event ID definition version 3 (continued)

ID	Description	Parameters
0x1F	RAW Boot mode setting in OCOTP fuses Bit [23:0] == RAW Boot Mode Setting	—
0x20	Secure config is FAB	—
0x21	Secure config is Field Return	—
0x22	Secure config is Open	—
0x23	Secure config is Closed	—
0x30	Internal use	—
0x31	Internal use	—
0x40	FUSE_SEL_VALUE Fuse is not blown	—
0x41	FUSE_SEL_VALUE Fuse is blown	—
0x50	Boot from the primary boot image	—
0x51	Boot from the secondary boot image	—
0x52	Boot from the recovery boot image	—
0x53	Boot via USB serial download	—
0x60	Primary boot from RAW NAND device	—
0x61	Primary boot from SD or EMMC device	—
0x66	Primary boot from one NAND device	—
0x67	Primary boot from QSPI NOR device	—
0x72	No recovery boot device	—
0x73	Recovery boot from SD or EMMC	—
0x80	Start to perform the device initialization	Parameter0: Time tick
0x81	The boot device initialization completes	Parameter0: Time tick
0x82	Starts to execute Boot device driver pre-config	—
0x83	Boot device driver pre-config completes	—
0x84	Boot image set 0 in primary boot device is selected	—
0x85	Boot image set 1 in primary boot device is selected	—

Table continues on the next page...

Table 10. ROM event ID definition version 3 (continued)

ID	Description	Parameters
0x86	The offset of boot image set1 is valid	—
0x8D	Both boot image set0 and set1 are all invalid	—
0x8E	Boot device driver pre-config fails	—
0x8F	The boot device initialization fails	Parameter0: Time tick
0x90	Start to read data from boot device	Parameter0: Image offset Parameter1: Time tick (optional)
0x91	Reading data from boot device completes	Parameter0: Time tick
0x94	The one in the core image target is in FlexSPI NOR space runs with XIP mode	—
0x9E	The target space of boot image recorded in container header is not valid	Parameter0: The base of target space Parameter1: The length of the image
0x9F	Reading data from boot device fails	Parameter0: Time tick
0xA0	Image authentication result	Parameter0: Authentication result Bit[7:0] == 0xF0: Authentication pass Parameter1: Time tick
0xA1	SECO container header is not valid	—
0xA2	SECO container header is valid	—
0xA3	SECO FW authentication pass	Parameter0: Not used Parameter1: Time tick
0xA4	SECO FW authentication fails	Parameter0: Not used Parameter1: Time tick
0xA5	SCU container authentication pass	Parameter0: Not used Parameter1: Time tick
0xA6	SCU container authentication fails	Parameter0: Not used Parameter1: Time tick
0xA7	The image verify passes	Parameter0: The mask of verified image Parameter1: Not used Parameter2: Time tick

Table continues on the next page...

Table 10. ROM event ID definition version 3 (continued)

ID	Description	Parameters
0xA8	The image verify fails	Parameter0: The mask of failed image (optional) Parameter1: Not used (if no failed image mask, it is parameter0) Parameter2: Time tick (if no failed image mask, it is parameter1)
0xA9	Release the container done	Parameter0: Not used
0xAA	Release the container fails	Parameter0: Not used
0xAB	DDR script is available	—
0xAC	SCU container header is not valid	—
0xAD	SCU container header is valid	—
0xAE	V2X container authentication pass (DXL only)	Parameter0: Not used Parameter1: Time tick
0xAF	V2X container authentication fails (DXL only)	Parameter0: Not used Parameter1: Time tick
0xB0	Starts to execute DDR script	Parameter0: The entry point of DDR script Parameter1: Time tick
0xB1	Running DDR script completes	Parameter0: Time tick
0xBA	Enhance image verify pass (DXL only)	
0xBF	DDR script returns failure	Parameter0: Time tick
0xC0	Jump to the boot image soon	Parameter0: The stack point Parameter1: The entry point of SCFW Parameter2: Time tick
0xCF	SCFW unexpectedly returns back to ROM code	—
0xD0	Enters serial download processing	—
0xE0	Internal use	—
0xF0	Enters ROM exception handler	Parameter0: The return address
0xF1	Switch boot stage	Parameter0: the boot stage ROM moves to Parameter1: Time tick

3 ROM event log buffer

The ROM event log buffer is located at a fixed address in the on-chip RAM.

3.1 Base address of ROM event log buffer

The 32-bit base address of the ROM event log buffer is recorded in a fixed location that varies by device type. Users must reference the ROM event log buffer base address to locate the log buffer data.

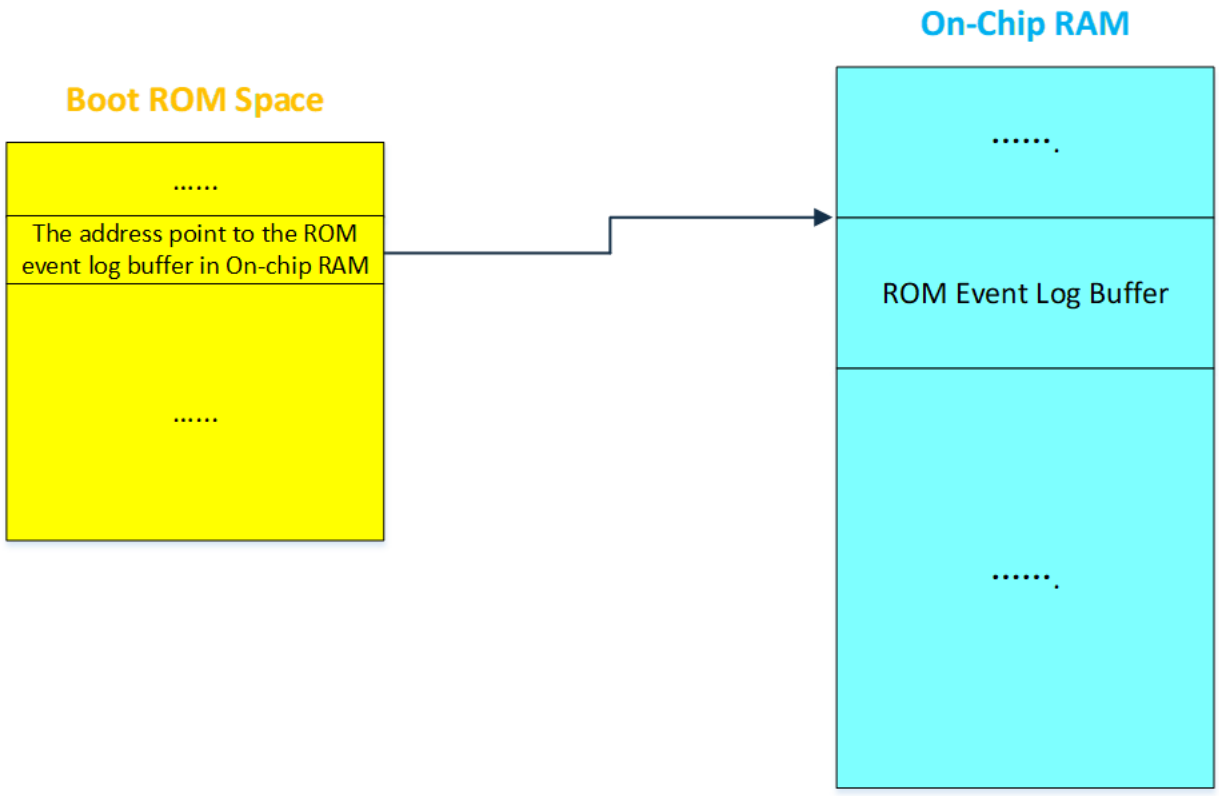

Figure 1. ROM event log buffer address

Table 11. ROM event log buffer address

i.MX device	Log buffer base address location
i.MX 6Q, i.MX 6QP, i.MX 6SL	0xD4
i.MX 6D	0xD8
i.MX 6SLX, i.MX 6SLL, i.MX 6UL, i.MX 6ULL, i.MX7ULP A7 ROM, i.MX7D	0x1E0
i.MX 7ULP M4 ROM	0x1C0005E0
i.MX 8QM series	0x5E0
i.MX mSCALE series	0x9E0

3.2 ROM event log buffer space

Normally, during a ROM boot cycle, the ROM code shares one single ROM event log buffer. The i.MX 8QM ROM log buffer space consists of four individual log buffers, each buffer is for one of four boot stages. These four buffers are continuous.

Table 12. ROM event log buffer space

ROM projects	Buffer number	Total buffer size
i.MX6 series, i.MX 7D, i.MX 7ULP	1	64 words
i.MX8 mSCALE	1	128 words
i.MX8 QM/QXP A0	1	128 words
i.MX8 QM/QXP B0	4	128 * 4 words
i.MX 8DXL	4	160 * 4 words

4 Revision history

Table 13. Revision history

Revision	Date	Description
0	May 2020	Initial release

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