AN12879

How to Enable Spread Spectrum for RT Family

Rev. 0 — June 2020 Application Note

Contents

1 Background

Spread spectrum is a communication technology that turns the frequency spectrum of a transmission signal to a wider bandwidth than its original bandwidth, and is widely used in the field of wireless communication.

This document intends to introduce the basic theory about spread spectrum and how to enable this feature for RT feature in order to enhance EMI performance.

2 Spread spectrum introduction

- Narrow-band Signals

  The Narrow-band signals have the signal strength concentrated, as shown in Figure 1.

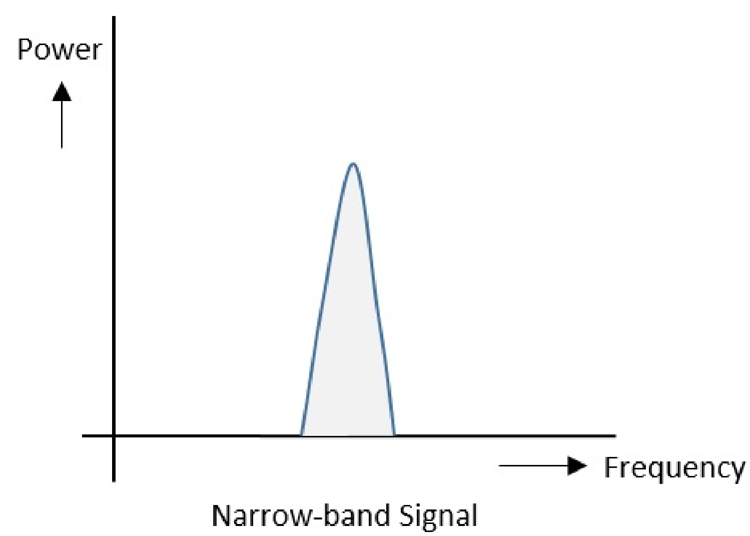

Figure 1. Narrow-band signals

Some features are as follows:

— Band of signals occupy a narrow range of frequencies.

— Power density is high.

— Spread of energy is low and concentrated.

Though the features are good, these signals are prone to interference.

- Spread Spectrum Signals

  The spread spectrum signals have the signal strength distributed,, as shown in Figure 2.

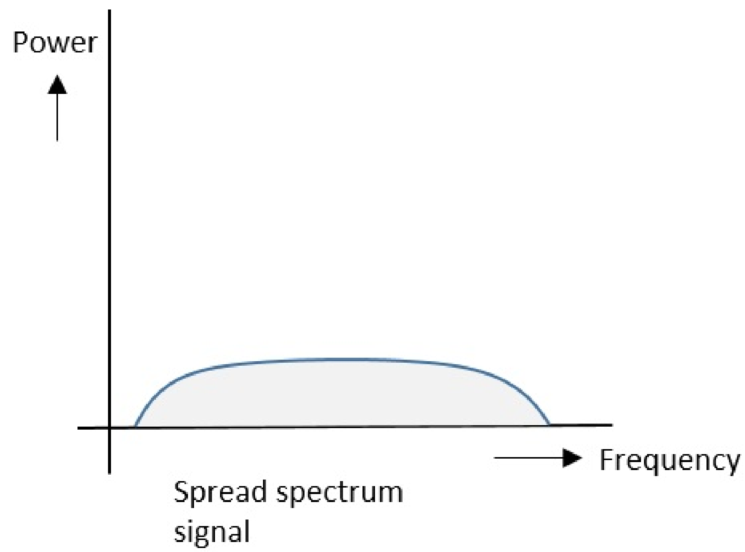

Figure 2. Spectrum spread signals

Some features are as follows:

— Band of signals occupy a wide range of frequencies.

— Power density is very low.

— Energy is wide spread.

From above description that you can see with these features, the spread spectrum signals are highly resistant to interference or jamming.

3 Spread spectrum configuration

For RT family, the `SYS_PLL2`, `AUDIO_PLL`, and `VIDEO_PLL` support spread spectrum (spread down). To enable the spread spectrum function, configure registers in SDK as shown in Figure 3.

```
/*
    0x40c84260 is used to configure the value of
    STOP(bit[31-16]) and STEP(bit[14:0]). Bit 8
    is the enable bit.
    The Frequency change is:
        Frequency change =  STOP/B *24MHz

    The Step value is :
        The max frequency change for each time = STEP/B * 24Mhz

    0x40c842a0 is used to configure the value of B.

    So that, the following configure is :
    STOP = 0x480;
    B    = 0x960;
    STEP = 0x6;
    Frequency change =  12MHz
    The max frequency change for each time = 60KHz

    STOP = 0x240;
    B    = 0x960;
    STEP = 0x6;
    Frequency change =  6MHz

    The max frequency change for each time = 60KHz
*/
    *(uint32_t *)(0x40c84260) = 0x04808006; //12MHz
    //*(uint32_t *)(0x40c84260) = 0x02408006; //6MHz
    *(uint32_t *)(0x40c842a0) = 0x00000960;
```

```
typedef struct _clock_sys_pll_config
{
    uint8_t loopDivider;  /*!< PLL loop divider. Intended to be 1 (528M).
                               0 - Fout=Fref*20;
                               1 - Fout=Fref*22 */
    uint32_t mfn;   /*!< 30 bit mfn of fractional loop divider.*/
    uint32_t mfi; /*!< 30 bit of fractional loop divider */
    uint16_t ss_stop;     /*!< Stop value to get frequency change. */
    uint8_t ss_enable;    /*!< Enable spread spectrum modulation */
    uint16_t ss_step;     /*!< Step value to get frequency change step. */
} clock_sys_pll_config_t;
```

Figure 3. Spread spectrum software configuration

4 Radiation comparison under spread spectrum

MIMXRT1170-EVK platform is used for such test.The radiation value is tested under different configuration for spread spectrum using non-contact probe and spectrum analyzer.

From the settings of the test result, 6 MHz and 12 MHz stop value is recommended in such case to improve EMI performance.

Spread Spectrum(HZ)	0.75M	1.5M	3M	6M	12M	24M
Test Result(dbm)	-46.2	-46.56	-49.85	-52.31	-53.35	-54.3

6M&12MHZ configure is recommended

Figure 4. Test result under different spread spectrum configuration

Figure 5. Spectrum under 3 MHz configuration

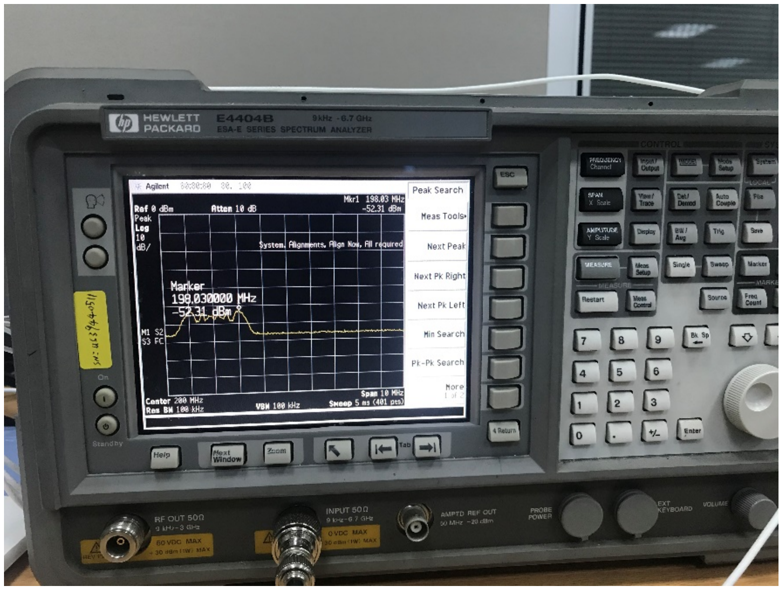

Figure 6. Spectrum under 6 MHz configuration

5 Reliability test under spread spectrum

The SDRAM reliability is verified under spread spectrum enabled on MIMXRT1170-EVK platform.

Table 1 shows the test pattern.

Table 1. Basic configuration of the test

	Module	Freq
Core	Cortex-M7	996 MHz
AXI to SEMC	32 bit	240 MHz
SEMC	32 bit	198 MHz
SDRAM chip	w9825g6kh	256 Mb/up to 200 MHz
L1 Dcache	Total 32 KB/One-line 32 B	—
Code	Text region in ITCM Data region in DTCM CStack region in DTCM	—

From the test result, both 6 M and 12 M can pass the stress test under full temp test, which means it’s quite reliable to enable spectrum spread feature for SDRAM clock.

```
DRAM test setting:
                  Base Address: 0x80000000;
                  Test Size: 67108864 Bytes;
                  Test Loop: 1;
                  DRAM Freq: 198010624;
                  Fail Stop: 0;
                  Enable Cache: 0;
                  Core clock: 996056064;
                  AHB clock: 120006784;
                  SEMC clock: 198010624;


memtester version 4.3.0 (32-bit)
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want 64MB (67108864 bytes)
Loop 1/1:
  Stuck Address: ok
  Random Value: ok
  Compare XOR: ok
  Compare SUB: ok
  Compare MUL: ok
  Compare DIV: ok
  Compare OR: ok
  Compare AND: ok
  Sequential Increment: ok
  Solid Bits: ok
  Block Sequential: ok
  Checkerboard: ok
  Bit Spread: ok
  Bit Flip: ok
  Walking Ones: ok
  Walking Zeroes: ok
  8-bit Writes: ok
  16-bit Writes: ok

Done and Passed!
exit_code 0x0
```

Figure 7. Reliability test result

6 SEMC timing configuration under spectrum spread

Considering about SEMC timing configuration under the spectrum spread, please check the folloeing points:

- For more stability of SDRAM, the SEMC timing configuration can be set with bigger margin based on the working clock speed.
- Referring the below figure of SDRAM chip timing requirements, the Minimum values of *tRC*, *tRAS*, *tRP*, *tRCD*, *tRW*, and *tRRD* can be set more one or two cycles in SEMC register SDRAMCR1 and SDRAMCR2. For example, the *tRC* is 6 cycles (60 ns minimum at 166 MHz) for standard. We can set it to **7** (or **8**) cycles under spectrum spread mode.
- For *tREF* (Refresh Cycle Time), it should be set littler than the Maximum refresh cycle (64 ms). This can be implemented in SEMC register SDRAMCR3. In NXP SDK, the *tREF* is set to be lower than half of Maximum refresh cycle.
- For the detailed SEMC timing configurations, please refer the NXP SDK.

t_{RC}	Command Period (REF to REF / ACT to ACT)	60	—	60	—	ns
t_{RAS}	Command Period (ACT to PRE)	42	100K	37	100K	ns
t_{RP}	Command Period (PRE to ACT)	18	—	15	—	ns
t_{RCD}	Active Command To Read / Write Command Delay Time	18	—	15	—	ns
t_{RRD}	Command Period (ACT [0] to ACT[1])	12	—	14	—	ns
t_{DPL}	Input Data To Precharge Command Delay time	12	—	14	—	ns
t_{DAL}	Input Data To Active / Refresh Command Delay time (During Auto-Precharge)	30	—	30	—	ns
t_{MRD}	Mode Register Program Time	12	—	14	—	ns
t_{DDE}	Power Down Exit Setup Time	6	—	7	—	ns
t_{XSR}	Exit Self-Refresh to Active Time (4)	66	—	70	—	ns
t_T	Transition Time	0.3	1.2	0.3	1.2	ns
t_{REF}	Refresh Cycle Time (8192)					
	$T_A \leq 70°C$ Com., Ind., A1, A2	—	64	—	64	ms
	$T_A \leq 85°$ C Ind., A1, A2	—	64	—	64	ms
	$T_A > 85°C$ A2	—	32	—	32	ms

Figure 8. SDRAM device timing

7 Performance test under spread spectrum

The performance test is done under spectrum spread, please check below test environment and test result. It can draw conclusion that spectrum spread has very small impact to SDRAM R/W performance and has no impact to applications.

- Project configuration: `sdram_debug`
- SDRAM MPU config: non-shareable/cacheable/wb/disable Dcache
- Four test environments: Initial, 6 MHz, 12 MHz, and 24 MHz
- Test results: Test 16 KBytes and 32 KBytes datas write/read performance for a few seconds. The results show that read performances are all 22 MB/s. The write performances are as shown in Figure 9.

Table 2. SDRAM Performance test under spread spectrum

		Initial	6 M	12 M	24 M
Average write	Perf (MB/S)	693	689	685	677
	Reduction percentage	—	-0.6%	-1.2%	-2.3%

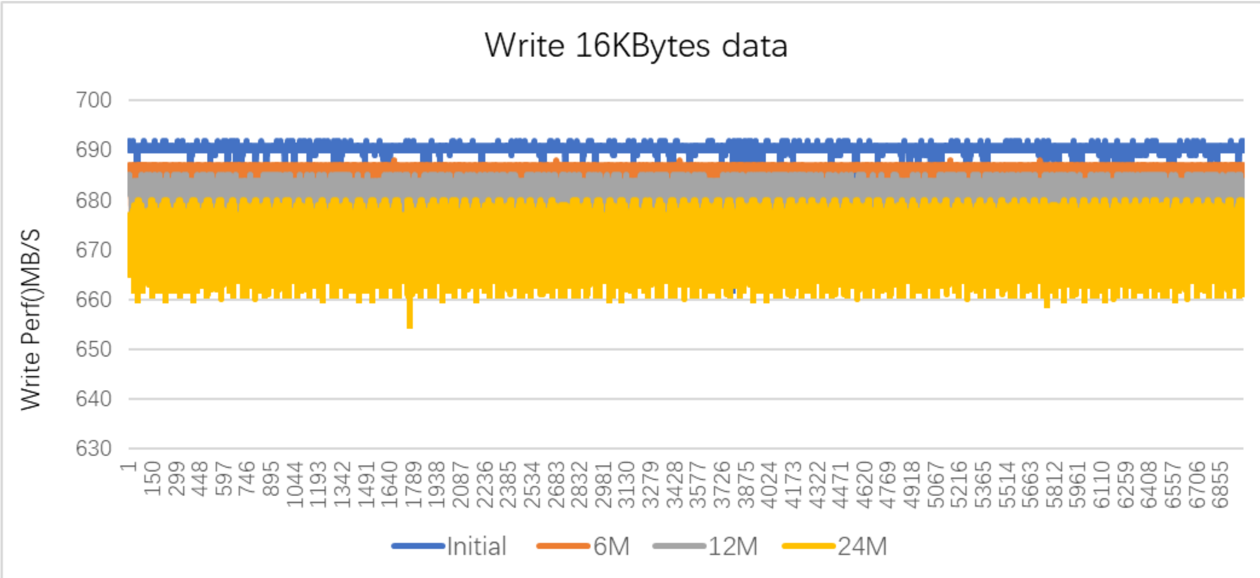

Figure 9. SDRAM Performance test under spread spectrum

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