Document Information

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<td>Keywords</td>
<td>i.MX RT, i.MX RT Crossover MCUs, spread spectrum, communication technology, frequency spectrum, transmission signal, bandwidth, wireless communication, electromagnetic interference, EMI, EMI performance, System-on-Chip, SoC, application processors</td>
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<tr>
<td>Abstract</td>
<td>This document intends to introduce the basic theory about spread spectrum and how to enable this feature for i.MX RT feature in order to enhance EMI performance.</td>
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1 Background

Spread spectrum is a communication technology that turns the frequency spectrum of a transmission signal to a wider bandwidth than its original bandwidth. It is widely used in the field of wireless communication.

This document introduces the basic theory about the spread spectrum and how to enable this feature for RT feature to enhance Electro Magnetic Interference (EMI) performance.

2 Spread spectrum introduction

• Narrowband signals
  The narrowband signals have the signal strength concentrated, as shown in Figure 1. A narrowband signal (or in this case the system clock) has a spectrum signature of a sharp narrow peak centered on a specific frequency.

![Narrowband Signal](image)

Figure 1. Narrowband signals
  Some characteristics are as follows:
  – The band of signals occupies a narrow range of frequencies.
  – The power density is high.
  – The spread of energy is low and concentrated.

• Spread spectrum signals
  The spread spectrum signals have the signal strength distributed, as shown in Figure 2. Instead of keeping the narrowband signal (or system clock in our case) at a fixed frequency, the spread spectrum works by moving the frequency across a defined range. The result is that the energy peak gets reduced and spreads over a range of frequency values.
Some characteristics are as follows:

- The band of signals occupies a wide range of frequencies.
- The power density is low.
- The energy is wide spread.

From the above descriptions, you can see that with these characteristics, the spread spectrum signals are highly resistant to interference or jamming.

### 3 Spread spectrum configuration

For the RT family, the `SYS_PLL2`, `AUDIO_PLL`, and `VIDEO_PLL` support the spread spectrum (spread down).

To enable the spread spectrum function, configure registers in SDK as shown in below.

```c
/*
0x40c84260 is used to configure the value of STOP(bit[31-16]) and STEP(bit[14:0]). Bit 8
is the enable bit.
The Frequency change is:
    Frequency change = STOP/B * 24MHz

The Step value is :
    The max frequency change for each time = STEP/B * 24Mhz

0x40c842a0 is used to configure the value of B.

So that, the following configure is:
STOP = 0x4B0;
B = 0x960;
STEP = 0x6;
Frequency change = 12MHz
The max frequency change for each time = 60KHz

STOP = 0x258;
B = 0x960;
*/
```

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STEP = 0x6;
Frequency change = 6MHZ
*/
*(uint32_t *)(0x40c84260) = 0x04B08006; //12MHZ
//*(uint32_t *)(0x40c84260) = 0x02588006; //6MHZ
*(uint32_t *)(0x40c842a0) = 0x00000960;

/*! @brief Spread specturm configure Pll */
typedef struct _clock_pll_ss_config
{
    uint16_t stop; /*!< Spread spectrum stop value to get frequency change. */
    uint16_t step; /*!< Spread spectrum step value to get frequency change step. */
} clock_pll_ss_config_t;

/*! @brief PLL configure for Sys Pll1 */
typedef struct _clock_sys_pll1_config
{
    bool pllDiv2En;            /*!< Enable Sys Pll1 divide-by-2 clock or not. */
    bool pllDiv5En;            /*!< Enable Sys Pll1 divide-by-5 clock or not. */
    clock_pll_ss_config_t *ss; /*!< Spread spectrum parameter,
                                 it can be NULL, if ssEnable is set to false */
    bool ssEnable;             /*!< Enable spread spectrum flag */
} clock_sys_pll1_config_t;

The following Phase Locked Loop (PLL) in RT1xxx series supports the spread spectrum.

<table>
<thead>
<tr>
<th>PLL</th>
<th>RT1170</th>
<th>RT1010</th>
<th>RT1015</th>
<th>RT1020/1024</th>
<th>RT1050</th>
<th>RT1060/1064</th>
</tr>
</thead>
<tbody>
<tr>
<td>PLL528</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PLL_528_</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>PFDn</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Audio_PLL</td>
<td>✓</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Video_PLL</td>
<td>✓</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>PLL_1G</td>
<td>✓</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
</tr>
</tbody>
</table>

There are two points when enabling the spread spectrum: Spread spectrum range and Step.

- The spread range indicates how much frequency the PLL sweeps down. For example, a spread range of 6 MHz indicates that the PLL sweeps from Target_frequency to Target_Frequency - 6 MHz and then sweeps back.
  The basic formula is used to calculate the range:
  \[ \text{Range} = \frac{\text{STOP}}{B} \times 24\text{MHz} \]  

- The spread step indicates how many frequencies are changed in one step.
  The basic formula is used to calculate the step:
  \[ \text{Step} = \frac{\text{STEP}}{B} \times 24\text{MHz} \]

Taking PLL528 as an example:
- STOP = 0x4B0
- B = 0x960
• STEP = 0x6
Then the Range and Step are:
• Range: 12 MHz
• Step: 60 kHz
The PLL528 sweeps from 528 MHz to 516 MHz (528 - Range) and sweeps back with one step 60 kHz. 

STOP, B, and STEP can be configured in SYS_PLL2_SS and SYS_PLL2_MFD registers on RT10xx series.

STOP, B, and STEP can be configured in CCM_ANALOG_PLL_SYS_SS and CCM_ANALOG_PLL_SYS_DENOM registers on RT1170.

Now when a PLL is initialized, the spread spectrum function can also be configured. Fill the STOP, B, and STEP and then initialize the PLL. Once the PLL is enabled, the spread spectrum function is also enabled.

### 4 Radiation comparison under spread spectrum

MIMXRT1170-EVK platform is used for such test. The radiation value is tested under different configuration for spread spectrum using noncontact probe and spectrum analyzer.

From the settings of the test result, 6 MHz and 12 MHz stop value is recommended in such case to improve EMI performance.

<table>
<thead>
<tr>
<th>Spread spectrum (Hz)</th>
<th>0.75 M</th>
<th>1.5 M</th>
<th>3 M</th>
<th>6 M</th>
<th>12 M</th>
<th>24 M</th>
<th>---&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test result (dBm)</td>
<td>-46.2</td>
<td>-46.56</td>
<td>-49.85</td>
<td>-52.31</td>
<td>-53.35</td>
<td>-54.3</td>
<td>6 M and 12 MHz configuration is recommended.</td>
</tr>
</tbody>
</table>

Figure 3. Spectrum under 3 MHz configuration
5 Reliability test under spread spectrum

The Synchronous DRAM (SDRAM) reliability is verified under the spread spectrum enabled on the MIMXRT1170-EVK platform. 

Table 3 describes the test pattern.

Table 3. Basic configuration of the test

<table>
<thead>
<tr>
<th>Module</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core</td>
<td>Cortex-M7 996 MHz</td>
</tr>
<tr>
<td>AXI to SEMC</td>
<td>32 bit 240 MHz</td>
</tr>
<tr>
<td>SEMC</td>
<td>32 bit 198 MHz</td>
</tr>
<tr>
<td>SDRAM chip</td>
<td>w9825g6kh 256 Mb/up to 200 MHz</td>
</tr>
<tr>
<td>L1 Dcache</td>
<td>Total 32 KB/One-line 32 B</td>
</tr>
<tr>
<td>Code</td>
<td>Text region in ITCM</td>
</tr>
<tr>
<td></td>
<td>Data region in DTCM</td>
</tr>
<tr>
<td></td>
<td>CStack region in DTCM</td>
</tr>
</tbody>
</table>

From the test result, both 6 MHz and 12 MHz spread spectrum configuration can pass the stress test under full temp test. The result indicates that it is reliable to enable the spectrum spread feature for SDRAM clock.
Considering about Smart External Memory Controller (SEMC) timing configuration under the spectrum spread, check the following points:

- For more stability of SDRAM, the SEMC timing configuration can be set with bigger margin based on the working clock speed.
- Referring to Table 4, the minimum values of $t_{RC}$, $t_{RAS}$, $t_{RP}$, $t_{RCD}$, $t_{RW}$, and $t_{RRD}$ can be set more one or two cycles in SEMC register SDRAMCR1 and SDRAMCR2. For example, the $t_{RC}$ is 6 cycles (60 ns minimum at 166 MHz) for standard. We can set it to 7 (or 8) cycles under spectrum spread mode.
- For $t_{REF}$ (Refresh Cycle Time), it is set smaller than the maximum refresh cycle (64 ms). This setting can be implemented in SEMC register SDRAMCR3. In NXP SDK, the $t_{REF}$ is set to be lower than half of the maximum refresh cycle.
- For the detailed SEMC timing configurations, refer to the NXP SDK.
Table 4. SDRAM device timing

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>tRC</td>
<td>Command period (REF to REF/ACT to ACT)</td>
<td>60</td>
<td>—</td>
<td>60</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRAS</td>
<td>Command period (ACT to PRE)</td>
<td>42</td>
<td>100 K</td>
<td>37</td>
<td>100 K</td>
<td>ns</td>
</tr>
<tr>
<td>tRP</td>
<td>Command period (PRE to ACT)</td>
<td>18</td>
<td>—</td>
<td>15</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRCD</td>
<td>Active command To read/write command delay time</td>
<td>18</td>
<td>—</td>
<td>15</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tRDD</td>
<td>Command period (ACT [0] to ACT[1])</td>
<td>12</td>
<td>—</td>
<td>14</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tDPL</td>
<td>Input data to precharge command delay time</td>
<td>12</td>
<td>—</td>
<td>14</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tDAL</td>
<td>Input data to active/refresh command delay time (during auto-precharge)</td>
<td>30</td>
<td>—</td>
<td>30</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tMRD</td>
<td>Mode register program time</td>
<td>12</td>
<td>—</td>
<td>14</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tDDE</td>
<td>Power down exit setup time</td>
<td>6</td>
<td>—</td>
<td>7</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tXSR</td>
<td>Exit self-refresh to active time (4)</td>
<td>66</td>
<td>—</td>
<td>70</td>
<td>—</td>
<td>ns</td>
</tr>
<tr>
<td>tT</td>
<td>Transition time</td>
<td>0.3</td>
<td>1.2</td>
<td>0.3</td>
<td>1.2</td>
<td>ns</td>
</tr>
<tr>
<td>tREF</td>
<td>Refresh cycle time (8192)</td>
<td>—</td>
<td>64</td>
<td>—</td>
<td>64</td>
<td>ms</td>
</tr>
</tbody>
</table>

For Ta ≤ 70 °C Com.,Ind., A1, A2: — 64 — 64 ms
For Ta ≤ 85 °C,Ind., A1, A2: — 64 — 64 ms
For Ta ≤ 85 °C A2: — 32 — 32 ms

7 Performance test under spread spectrum

The performance test is done under spectrum spread, check below test environment and test result. It can conclude that spectrum spread has small impact to SDRAM R/W performance and has no impact to applications.

- **Project configuration**: sdradm_debug
- **SDRAM MPU configuration**: non-shareable/cacheable/wb/disable Dcache
- **Four test environments**: Initial, 6 MHz, 12 MHz, and 24 MHz
- **Test results**: Test 16 kbit and 32 kbit data write/read performance for a few seconds. The results show that the read performances are all 22 MB/s. The write performances are as shown in Figure 6.

Table 5. SDRAM performance test under spread spectrum

<table>
<thead>
<tr>
<th></th>
<th>Initial</th>
<th>6 M</th>
<th>12 M</th>
<th>24 M</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Average write</strong></td>
<td>Perf (MB/s)</td>
<td>693</td>
<td>689</td>
<td>685</td>
</tr>
<tr>
<td><strong>Reduction percentage</strong></td>
<td>—</td>
<td>-0.6%</td>
<td>-1.2%</td>
<td>-2.3%</td>
</tr>
</tbody>
</table>
8  Note about the source code in the document

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9  Revision history

Table 6 summarizes the revisions to this document.
Table 6. Revision history

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<th>Release date</th>
<th>Description</th>
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<tr>
<td>2</td>
<td>25 August 2023</td>
<td>Updated [Section 3]</td>
</tr>
<tr>
<td>1</td>
<td>09 March 2021</td>
<td>Updated [Section 3]</td>
</tr>
<tr>
<td>0</td>
<td>June 2020</td>
<td>Initial public release</td>
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