CONTENT

Introducing 88MW320/322
- Functional Overview
- Key considerations
- Collaterals

Single PCB Design Overview
Introducing 88MW320 and 88MW322
MAIN FEATURES

- Major system blocks
  - Microcontroller sub-system
  - Wi-Fi connectivity sub-system
- Device interface overview
  - Power
  - Clock
  - QSPI and Flash memory interface
  - Antenna interface
- Operating modes
- Always-on circuit and power saving features
88MW32x integrates voltage regulators for 3.3V system power
KEY CONSIDERATIONS

• Power
  - On-chip BUCK regulator for 1.8V for Wi-Fi sub-system analog and digital
  - On-chip LDOs for application sub-system running at 1.8V and 1.1V
  - 3.3V +/- 10% for Wi-Fi TX PA
  - Multiple I/O bias rails

• Clock
  - Two internal and two external sources
    • Main clock reference at 38.4 MHz
    • Sleep clock / RTC reference clock at 32.768 kHz or ~32 kHz

• External Flash memory with Quad-bit SPI up to 50 MHz
  - Execute-In-Place (XIP) support for optimal performance

• Antenna
  - Low pass filter to single antenna for basic configuration
  - External RF switch needed for antenna diversity support
88MW322/320 POWER MANAGEMENT

USB_AVDD33 only in 88MW322

Internal power plane
## POWER PIN TABLE AND DESIGN REFERENCE

<table>
<thead>
<tr>
<th>Power pin</th>
<th>QFN88</th>
<th>QFN68</th>
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<td>18,19,23,24,25,28</td>
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Refer to Schematics and Layout for:

RD-88MW320-QFN-1B-2A_v1 “Stamp Module”,

RD-88MW322-QFN-1B-2A_v1 “Stamp Module”,

Free PADS viewer can be downloaded from:

• Fill the empty spaces of board with ground and connect them to ground plane with multiple vias
• GND pad from 69 should be connected to ground plane with maximum number of vias for better ground connectivity and heat sink capability
  - 25 vias are recommended.
• Traces of power should be as thick as possible
• Layer #2 should be a uniform ground plane to reduce return path for current from other components
• Place decoupling capacitors as close to pin as possible
• Connect each ground pin of the chip to ground plane with separate via(s)
• Try not to share ground via for decoupling capacitors

See the detailed Layout Guidelines in “Single PCB Design Section”
• Each I/O domain can be powered with 1.8V/2.5V/3.3V +/- 10%
  - RESETn bias is on VDDIO_AON
  - VDDIO_3/_3_N 1.8V +10%/-5%
• QSPI bus on VDDIO_2 dedicated for Flash device I/F for majority of applications
  - Majority of QSPI devices operate in 1.8V or 3.0/3.3V range
• JTAG and UART[0] signals useful for development, programming, monitoring, and provisioning
## MULTIFUNCTION MAPPING : VDDIO_0

VDDIO_0 Group : 16 for 88MW322, 11 for 88MW320

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<th>ALT 1</th>
<th>ALT 2</th>
<th>ALT 3</th>
<th>ALT 04</th>
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## Multifunction Mapping: VDDIO_1 and VDDIO_2

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VDDIO_3 Group : 17 for 88MW322, 12 for 88MW320
# MULTIFUNCTION MAPPING: VDDIO_AON

**VDDIO_AON Group**: 5 for 88MW322 and 88MW320

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<td>PU</td>
<td>XTAL32K_IN</td>
<td>GPIO_25</td>
<td>I2C1_SDA</td>
<td>SSP1_FRM</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>50</td>
<td>40</td>
<td>PU</td>
<td>XTAL32K_OUT</td>
<td>GPIO_26</td>
<td>I2C1_SCL</td>
<td>SSP1_TXD</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
EXECUTION SEQUENCE OUT OF RESET

Out of RESET, C-M4F CPU fetches RESET vector from internal ROM that transfers execution to the Primary Boot Code (PBC) in the ROM itself.

- Reset vector and PBC are permanently programmed in the 88MW32x device and cannot be modified ever.

PBC loads the “image header” from external “serial Flash” device to internal SRAM.

Based on the header content, PBC loads second level “boot2” image from external serial Flash to internal SRAM and then executes it from SRAM.

“boot2” code then loads the application image in SRAM along with its data, and executes the application program.

C-M4F CPU also transfers the image for the Communication Processor (CP), which resides in its own SRAM.

“boot2” and application program image created with WMSDK A (Wireless Microcontroller Software Development Kit)
DESIGN NOTE: RESETN AND CONFIGURATION

- 88MW32x SoC executes code from internal ROM (also referred as Boot ROM) after valid reset condition is de-asserted
  - ROM is 128KB (permanently programmed in silicon)
    - PBC 0x000000 : 0x007FFF
    - WMSDKA Library 0x008000 : 0x01FFFF
  - Depending on CON[5:4], loads code from Flash/UART/USB
- Reset sources can be
  - Power-On-Reset (POR)
  - RESETn pin
  - Cortex-M4F exit from low-power mode
  - Warm reset
    - Brown-out detection by power management
    - Soft RESET instruction from CPU
    - CM4F exit LOCKUP state (for example NMI)
    - Watchdog timer timeout

<table>
<thead>
<tr>
<th>Boot configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>CON[5:4]</td>
</tr>
<tr>
<td>----------</td>
</tr>
<tr>
<td>00</td>
</tr>
<tr>
<td>01</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>11</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>GPIO used by boot code</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO</td>
</tr>
<tr>
<td>------</td>
</tr>
<tr>
<td>27</td>
</tr>
<tr>
<td>16</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>28:33</td>
</tr>
</tbody>
</table>

The designer should provide access to GPIO_27 and GPIO_16 on the PCBA to support the alternate boot method.
CLOCK SOURCES AND DISTRIBUTION

- External or internal reference clock generation for FAST and SLOW clocks
  - FAST: 38.4 MHz
  - SLOW: 32.768 kHz

- Three PLLs for application specific operation
  - System PLL (SFLL) : 200 MHz max
  - Audio PLL (AUPLL)
  - USB PLL (USBPLL) for HS/FS/LS

- SYSCLK and its derivatives used by all other system blocks
  - Two programmable fractional divider shared between UART[0:3]
DESIGN NOTE: USING RC32K CLOCK REFERENCE

- Using on-chip RC OSC for 32 kHz reference requires in-system calibration to compensate for:
  - Voltage drift
  - Temperature drift
- Accurate REFCLK_SYS 38.4 MHz required
- Divided clock at 32.768 KHz output on GPIO_24 needs to be fed back to GPIO_25 off-chip

Reduce system cost and board space by not using external 32.768 kHz crystal

GPIO_24 and GPIO_25 are not available for application use

GPT1-CH5 is not available for application use, and GPT1 clock source is fixed, derived from 38.4 MHz
QSPI PHYSICAL INTERFACE TO FLASH MEMORY

- Support for data transfer on 1-bit (DO + DI) or bi-directional 2-bit or 4-bit data bus
- 50 MHz max clock
- VDDIO_2 exclusive to 6 signals for QSPI
  - 3.3V or 1.8V common
- Flash controller useful for READ operations
  - For Write/Erase use QSPI
- “Basic” and “Additional” features use select set of SPI Flash “commands”

QSPI physical interface to external QSPI Flash Memory
Device is multiplexed between two internal functional blocks:
- QSPI controller
- Flash controller
Bus transaction: WRITE

<table>
<thead>
<tr>
<th>INSTRUCTION</th>
<th>ADDRESS</th>
<th>DUMMY</th>
<th>DATA WRITE</th>
</tr>
</thead>
<tbody>
<tr>
<td>instr_cnt</td>
<td>addr_cnt</td>
<td>dummy_cnt</td>
<td>Continue till xfer_stop</td>
</tr>
</tbody>
</table>

Instr count: 0/1/2 bytes  
Addr count: 0/1/2/3/4 bytes  
Dummy count: 0/1/2/3 bytes  
Continue till xfer_stop

Bus transaction: READ

<table>
<thead>
<tr>
<th>INSTRUCTION</th>
<th>ADDRESS</th>
<th>READ MODE</th>
<th>DUMMY</th>
<th>DATA READ</th>
</tr>
</thead>
<tbody>
<tr>
<td>instr_cnt</td>
<td>addr_cnt</td>
<td>rm_cnt</td>
<td>dummy_cnt</td>
<td>DinCnt Register[19:0]</td>
</tr>
</tbody>
</table>

Instr count: 0/1/2 bytes  
Addr count: 0/1/2/3/4 bytes  
Read mode: 0/1/2 bytes  
Dummy count: 0/1/2/3 bytes  
DinCnt Register[19:0]  
0x000000 = continuous

HdrCnt

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

Reserved: bool  
Read mode: bool  
Addr count: bool  
Reserved: bool  
Instr count: bool

dummy_cnt
FLASH MEMORY CONTROLLER

- 16 MB address space
- 8-way set-associative cache
- 32 byte line
- 32 KB cache array
- Pseudo least recently used line replacement algorithm
- Cache can be bypassed
  - Use array as SRAM

Support for Execute-In-Place (XIP) by caching I/D Code bus
FLASH CONTROL REGISTER

FCCR

| 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 |
|----------------------|-------------------|-------------------|-------------------|-------------------|
| flashc_pad_en        | cache_en          | cache_line_flush  | sram_mode_en       |
| 0 = QSPI controls pins | 1 = Flash controller controls pins |

Refer to the table below

<table>
<thead>
<tr>
<th>cmd_type</th>
<th>Code</th>
<th>Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>0x03</td>
<td>Read Data</td>
</tr>
<tr>
<td>0x1</td>
<td>0x0B</td>
<td>Fast Read</td>
</tr>
<tr>
<td>0x2</td>
<td>0x3B</td>
<td>Fast Read Dual Output</td>
</tr>
<tr>
<td>0x3</td>
<td>0x6B</td>
<td>Fast Read Quad Output</td>
</tr>
<tr>
<td>0x4</td>
<td>0xBB</td>
<td>Fast Read Dual I/O</td>
</tr>
<tr>
<td>0x5</td>
<td>0xBB</td>
<td>... w/ Continuous Read Mode</td>
</tr>
<tr>
<td>0x6</td>
<td>0xEB</td>
<td>Fast Read Quad I/O</td>
</tr>
<tr>
<td>0x7</td>
<td>0xEB</td>
<td>... w/ Continuous Read Mode</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>cmd_type</th>
<th>Code</th>
<th>Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x8</td>
<td>0xE7</td>
<td>Word Read Quad I/O</td>
</tr>
<tr>
<td>0x9</td>
<td>0xE7</td>
<td>... w/Continuous Read Mode</td>
</tr>
<tr>
<td>0xA</td>
<td>0xE3</td>
<td>Octal Word Read Quad I/O</td>
</tr>
<tr>
<td>0xB</td>
<td>0xE3</td>
<td>... w/Continuous Read Mode</td>
</tr>
<tr>
<td>0xC</td>
<td>0xFFFF</td>
<td>Exit from cont. Read Dual</td>
</tr>
<tr>
<td>0xD</td>
<td>0xFF</td>
<td>Exit from cont. Read Quad</td>
</tr>
<tr>
<td>0xE</td>
<td>-</td>
<td>Not used</td>
</tr>
<tr>
<td>0xF</td>
<td>-</td>
<td>Not used</td>
</tr>
</tbody>
</table>

Default command

* Bus cycles follow Winbond W25Q Device Family Requirements

0x00 : SPI_CLK/1
0x01 : SPI_CLK/1
0x02 : SPI_CLK/2
0x03 : SPI_CLK/3
...
0x0E : SPI_CLK/14
0x0F : SPI_CLK/15
0x10 : SPI_CLK/2
0x11 : SPI_CLK/2
0x12 : SPI_CLK/4
0x13 : SPI_CLK/6
...
0x1E : SPI_CLK/28
0x1F : SPI_CLK/30
## USING FLASH CONTROL REGISTER 2

### FCCR2

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-31</td>
<td>data_pin</td>
<td>RESERVED</td>
</tr>
<tr>
<td>0-31</td>
<td>ADDR_CNT</td>
<td>RSVD</td>
</tr>
<tr>
<td>0-31</td>
<td>RM_CNT</td>
<td>R</td>
</tr>
<tr>
<td>0-31</td>
<td>ADDR_CNT</td>
<td>RSVD</td>
</tr>
<tr>
<td>0-31</td>
<td>INSTR_CNT</td>
<td></td>
</tr>
</tbody>
</table>

- **Use FCCR based cmd_types fixed in H/W**: 0
- **Use FCCR2 based transactions**: 1

#### addr_pin

- **0**: 1 byte
- **1**: 4 byte

#### use_cfg_ovrd

- **0**: 1 pin
- **1**: same as in data_pin

#### FCSR

- **Send 0x00**: 0x00: instr not sent
- **Instr[15:8]**, **Instr[7:0]** sent: 0x01
- **Instr[15:8]**, **Instr[7:0]** sent: 0x10
- **Instr[15:8]**, **Instr[7:0]** sent: 0x11

#### FINSTR

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-31</td>
<td>RESERVED</td>
<td></td>
</tr>
<tr>
<td>0-31</td>
<td>FINSTR[15:8]</td>
<td></td>
</tr>
<tr>
<td>0-31</td>
<td>FINSTR[7:0]</td>
<td></td>
</tr>
</tbody>
</table>

#### FRMR

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0-31</td>
<td>RESERVED</td>
<td></td>
</tr>
<tr>
<td>0-31</td>
<td>0x00: instr not sent</td>
<td></td>
</tr>
<tr>
<td>0-31</td>
<td>0x01: instr[7:0] sent</td>
<td></td>
</tr>
<tr>
<td>0-31</td>
<td>0x02: instr[15:8], instr[7:0] sent</td>
<td></td>
</tr>
</tbody>
</table>
**DESIGN NOTE: READ TIMING ANALYSIS AT 50 MHZ**

**Parameter** | **Value (ns)**
--- | ---
\( t_w(\text{min}) \) | 20/2 – 0.5 = 9.5
\( t_w(\text{max}) \) | 20 - \( t_w(\text{min}) \) = 10.5
\( t_{\text{CLQV}} \) | 8.5
\( t_{\text{CLQX}} \) | 0
\( t_{\text{su}(\text{RX})} \) | 8
\( t_{\text{TR}(\text{RX})} \) | 0

**MW320 side data setup time analysis:**
\[ t_w(\text{min}) - t_{\text{CLQV}} = 9.5 - 8.5 = 1.0 \text{ ns} \]
\( t_{\text{su}(\text{RX})} = 8 \text{ ns} \)
Design margin available = -7.0 ns

**MW320 side data hold time analysis:**
\[ t_{\text{CLQX}(\text{TX})} = 0 \text{ ns} \]
\( t_{\text{TR}(\text{RX})} = 0 \text{ ns} \)
Design margin available = 9.5 ns

**Flash to MW32x**

**Flash to MW32x**

**USE CLK_CAPT_EDGE = 1**

---

From: Winbond W25Q80BV Datasheet
DESIGN NOTE: WRITE TIMING ANALYSIS AT 50 MHZ

Parameter | Value (ns)
---|---
t_w(min) | 20/2 – 0.5 = 9.5

Flash side data setup time analysis:
\[ t_{w(min)} - t_{out(TX)} = 9.5 - 7 = 2.5 \text{ ns} \]
\[ t_{DVCH} = 2 \text{ ns} \]
Design margin available = 0.5 ns

Flash side data hold time analysis:
\[ t_{w(min)} + t_{h(TX)} = 9.5 + 0 = 9.5 \text{ ns} \]
\[ t_{CHDX} = 5 \text{ ns} \]
Design margin available = 4.5 ns

From: Winbond W25Q80BV Datasheet

**Summary**

Flash device requirement

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value required (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_{DUCH} (min)</td>
<td>2.5 or less</td>
</tr>
<tr>
<td>t_{CHDX} (min)</td>
<td>9.5 or less</td>
</tr>
<tr>
<td>t_{CLQV} (max)</td>
<td>12.0 or less</td>
</tr>
<tr>
<td>t_{CLQX} (min)</td>
<td>0.0 or more</td>
</tr>
</tbody>
</table>

Use CLK_CAPT_EDGE = 1
DESIGN NOTE: FLASHC AND QSPI REGISTER SETTING

• QSPI bus timing needs to be set in two functional blocks
  - QSPI @0x46010000 : 0x4601003B
  - Flash Controller (FLASHC) @0x44003000 : 0x4400302F

• CLK_CAPT_EDGE bit is at different bit-field
  - QSPI → Serial Interface Timing Register (offset 0x24) bit 6
  - FLASHC → Flash Controller Timing Register (offset 0x04) bit 4

• Software component to check
  - Boot ROM
  - Boot2
  - Drivers and Framework
  - Tools

Refer to the Boot ROM section in the Datasheet and MWSDK documents
DESIGN NOTE: FLASH DEVICE SELECTION

- Read and fast read used by Flash controller, once configured
- Boot ROM uses common commands for READ/ERASE/WRITE
  - 0x03 (READ), 0xC7 (ERASE), 0x02 (PROG)
- “Basic” features used by Flash controller and boot ROM UART boot
- “Additional” features include USB boot (for 88MW322 only) and Flash programming

Winbond W25Qxx family validated
Devices from other suppliers support necessary commands for “Basic” features
SINGLE ANTENNA CONNECTOR

- 88MW32x RX_TR (antenna) pin through a low pass filter can be directly connected to a u.FL, w.FL, or other RF connector.
- With external antenna or a separate internal PCB antenna, flexibility for RF testing and calibration can be easily carried out by using the same low cost connector.
• External RF Switch – SPDT (Single Pole, Double Throw) control support is provided through GPIO_44 and GPIO_45 for Antenna Diversity
  • Differential or direct signal configuration can be used
• Plan VDDIO_3 bias voltage to support the RF Switch requirements (typically 3.3V or 1.8V choice) and other GPIO in the group
## Operating Modes: Application Processor

<table>
<thead>
<tr>
<th>Subsystem</th>
<th>PM0 Active</th>
<th>PM1 Idle</th>
<th>PM2 Standby</th>
<th>PM3 Sleep</th>
<th>PM4 Shutoff</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cortex-M4F</td>
<td>C0 (Run)</td>
<td>C1 (Idle)</td>
<td>C2 (Standby)</td>
<td>C3 (Off)</td>
<td>C3 (Off)</td>
</tr>
<tr>
<td>SRAM</td>
<td>M0 (Run)</td>
<td>M0 (Run)</td>
<td>M2 (Standby)</td>
<td>M2 (Standby)</td>
<td>M3 (Off)</td>
</tr>
<tr>
<td>Flash</td>
<td>Active standby (CSn=H)</td>
<td>Active standby</td>
<td>power-down (reduce leakage)</td>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>RTC</td>
<td>on</td>
<td>on</td>
<td>on</td>
<td>on</td>
<td>on</td>
</tr>
<tr>
<td>Peripherals</td>
<td>on: selective clock gating</td>
<td>on: selective clock gating</td>
<td>state retentive</td>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>Main XTAL</td>
<td>on/off</td>
<td>on/off</td>
<td>on/off</td>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>SFLL</td>
<td>on/off</td>
<td>on/off</td>
<td>on/off</td>
<td>off</td>
<td>off</td>
</tr>
<tr>
<td>AUPLL</td>
<td>on/off</td>
<td>on/off</td>
<td>on/off</td>
<td>off</td>
<td>off</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cortex-M4 State</th>
<th>HCLK/FCLK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Run</td>
<td>on/on</td>
</tr>
<tr>
<td>Idle</td>
<td>off/on</td>
</tr>
<tr>
<td>Standby</td>
<td>off/off (State retention)</td>
</tr>
<tr>
<td>Off</td>
<td>Power Removed</td>
</tr>
</tbody>
</table>

**HCLK** = AHB-Lite system clock.  
- Can be gated off during sleep mode

**FCLK** = Free running clock  
(in same phase as HCLK)  
- Must be running to generate edge trigger interrupt
OPERATING MODES: COMMUNICATION PROCESSOR

- **WPM0 active**
  - All internal power domains and external power supplies are fully powered, and operational

- **WPM1 deep sleep**
  - Only the power domains for AON (Always-on) and selected memory modules are ON
  - Other power domains are OFF

- **WPM2 shut down**
  - All power supplies are turned OFF

CP beacon timer can transition out of WPM1 to WPM0. Also, the AP can control the power mode register to change state.

Power mode register is controlled by the AP to transition between WPM0 and WPM2.
Always-on domains for applications processor and communications processor can be independently managed.

- Dedicated internal LDOs power the AON circuits
- Wake-up sources
  - WAKE_UP_0/1 input
  - RTC timeout
  - Ultra low power comparator
**WI-FI PERFORMANCE TESTING SETUP**

- **Platform:** RD-88MW322-QFN-1B-2A_V1
  - Measurements carried out on this platform

- **Test conditions**
  - All RF parameters at 88MW320/322 RF_TR pin
  - Typical RF front-end loss (pin to antenna) is 1.5 dB
  - Minimum/maximum values over temperature, voltage and frequency
    - Temperature → -40° to +85°C
    - Voltage → 1.8V +/- 5% to 3.3V +/- 10%
    - Center frequency → 2.412 to 2.472 GHz
Single PCB Design
SINGLE PCB DESIGN

• Reasons for Chip-on-Board (CoB) design considerations
  - Module-based design not possible
    ▪ Physical shape or size of product
    ▪ Power topology requirement not supported by available modules
  - Cost reduction for high volume with single PCBA
  - Business requirements
    ▪ Barrier to competition
    ▪ CoB design reuse by OEM/ODM for multiple products

• Capabilities (in-house or access to)
  - RF design and testing
  - Regional certification

• Key considerations
  - RF: Low pass filter (LPF), antenna diversity switch
  - Power supply topology
**BAND PASS / LOW PASS FILTER**

- **Reference**
  - Vendor: TDK
  - Part number: DEA162450BT-1298A1

- **LPF or BPF**
  - Low Pass Filter (LPF) sufficient to control 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonic emission where co-existence is not an issue
  - Consider Band Pass Filter (BPF) to attenuate frequency below the Wi-Fi band for co-existence with cellular and other RF communication

- **Key parameters to consider**
  - Insertion loss
  - Characteristic impedance
  - Pass band ripple
  - Stop band ripple: Especially at 2\textsuperscript{nd} and 3\textsuperscript{rd} harmonic frequencies
  - Roll off rate for band pass filter, particularly at lower end of the pass band
RF SWITCH FOR ANTENNA DIVERSITY

• Reference for RF SPDT switch
  - Vendor: Skyworks
  - Part number: SKY13323-378LF

• Key parameters to consider
  - Input power
  - Insertion loss
  - P1dB compression point
  - Characteristic impedance
  - Need for external DC blocking capacitors

• Control signal voltage (3.3V vs. 1.8V)
  - GPIO_[44:45] differential pair used for switch control with bias on VDDIO_3
    • Ensure other GPIO in the group can operate at selected bias
  - Confirm appropriate RF switch characteristics
POWER TOPOLOGY CONSIDERATIONS

• Support for different power sources
  - Wi-Fi PA, logic domain 1.8V and 1.1V, analog domain 1.8V

• Support for different VDDIO groups
  - SPI Flash at 1.8V
  - Digital interfaces at 1.8V or 2.5V or 3.3V
  - Analog at 1.8V or 2.5V or 3.3V
• Decoupling capacitors
  - External CAP for LDO18 (PMIP)
    ▪ C20 value 2.2uF
    ▪ Keep as close as possible to pin 66
  - External CAP for LDO11 (PMIP)
    ▪ C19 value 2.2uF
    ▪ Keep as close as possible to pin 68
LAYOUT GUIDELINE: PSU BUCK18

- Decoupling capacitors for PSU
  - Input CAP
    - C11 value 10uF X5R
    - Input power rail → CAP → pin 34
    - Two vias from input power plane
    - Two vias to GND
  - Output CAP
    - C2 value 10uF X5R
    - Two vias to GND
  - Keep GND via for input and output CAPs as close as possible

- Power inductor
  - Two vias to 1.8V power plane
• Decoupling capacitors for PSU
  - Input CAP
    ▪ C3 value 1.0uF
    ▪ 1.8V power plane → CAP → pin 31
  - Output CAP
    ▪ C4 value 1.0uF
    ▪ Pin 32 → CAP → 1.1V power plane
    ▪ 1.1V power plane → VDD11 pins
• Decoupling capacitors
  – AVDD18 for RF Unit (RFU) and Common Analog Unit (CAU)
    ▪ C21 to C26 value 0.01uF
    ▪ Shortest path from power plane to Capacitor through via, and then to the MW32x AVDD18 pins
  – AVDD33 for PA
    ▪ C1 value 10uF
    ▪ Minimum 2 via from power plane
    ▪ Shortest path to pin from CAP
LAYOUT GUIDELINE: VDDIO AND VDDD11 D-CAPS

- Decoupling capacitors $C[9,10,12,13,14,16,17,18]$ for each VDDIO_x should be connected to the pins $[5,29,41,48,50,53,57,67]$ as close as possible.
- VDD11 power on pins 28 and 49 should have decoupling capacitors $C_{28}$ and $C_{29}$ as close as possible.
- The via from the power plane should first connect to the CAP and then the trace to the pin.
LAYOUT GUIDELINE: RF

- Pay attention to:
  - Impedance control: 50 Ω
  - Noise coupling
  - Emission
  - Ground plane
  - Trace bend

- Solid GND plane under RF
  - GND on top layer around RF trace with sufficient stitching vias

- Place C34 as close as possible to RF_TR pin

- Isolate RF trace from high frequency digital signals and power lines to avoid coupling with them

- Avoid routing RF trace with sharp corners, a smooth arch is suggested
LAYOUT GUIDELINE: USB

- Crystal should be placed as close to chip as possible
- Crystal lines should be as short as possible
- Crystal should be placed as far away as possible from RF section and antenna
- Avoid noise coupling
  - GND plane under crystal and its in/out signal traces
  - No power or signal on any layer underneath crystal or its in/out lines
SECURE CONNECTIONS FOR A SMARTER WORLD