AN12992

Power iMX6 processors with NXP PMIC

Rev. 1 — 4 November 2020 Application note

1 PMICs and i.MX6 processor matrix table

BSP *= BSP available aligned with processor*
PATCH *= Patch available from apps support*
ALT *= Alternative Solution, no BSP available*
Refer to device datasheets for available list of standard parts reference

	PF0100	PF0200	PF3000 PF3001	PF1550 PF1510	PF5020	PF7100	PF8100
i.MX6 ULZ	—	—	PATCH	PATCH	ALT		—
i.MX6 ULL	—	—	PATCH	PATCH	ALT	—	—
i.MX6 UL	—	—	PATCH	PATCH	ALT	—	—
i.MX6 SoloX	—	BSP	PATCH	—	ALT	—	—
i.MX6 SLL	BSP	—	PATCH	—	ALT	—	—
i.MX6 SoloLite	BSP	—	PATCH	—	ALT	—	—
i.MX6 Solo	BSP	—	—	—	ALT	—	—
i.MX6 DualLite	BSP	—	—	—	ALT	—	—
i.MX6 Dual	BSP	—	—	—	—	ALT	—
i.MX6 Quad	BSP	—	—	—	—	ALT	—
i.MX6 DualPlus	BSP	—	—	—	—	ALT	ALT
i.MX6 QuadPlus	BSP	—	—	—	—	ALT	ALT

2 Power i.MX6 UL/ULL/ULZ with the PF5020

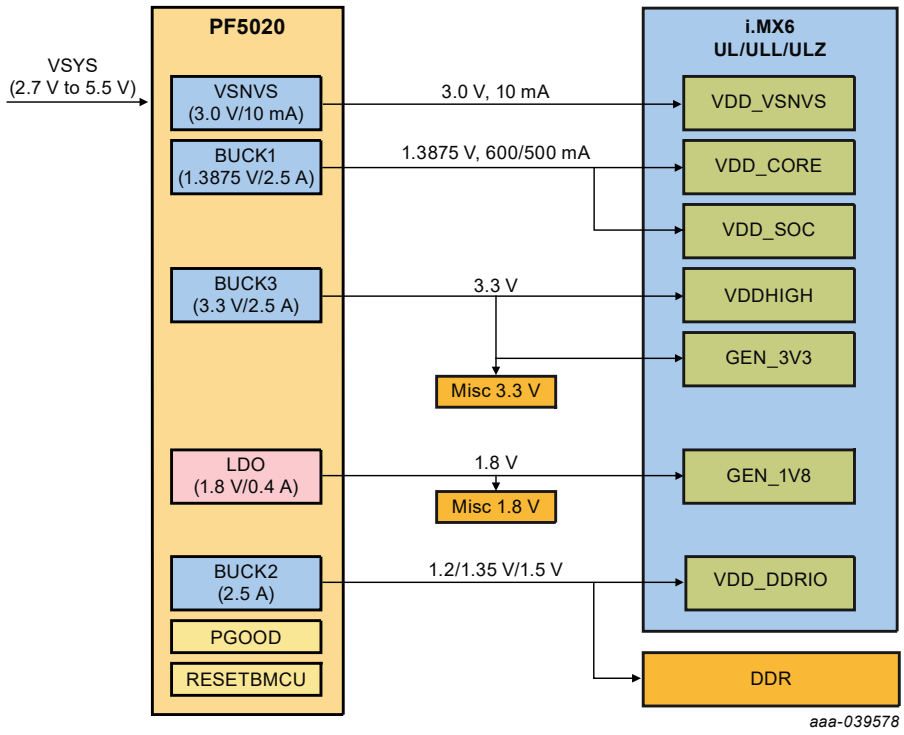

Figure 1. Simplified system power block diagram

The existing PMICs on the i.MX6 UL/ULL/ULZ reference design board are the NXP PF1550/1510, PF3000/3001 and discrete solutions. The following reference design resources can be downloaded from nxp.com.

- i.MX6UL
- i.MX6ULL
- i.MX6ULZ

Reasons why the PF5020 is an alternative solution to the PF1550/1510/3000/3001 and discrete power solution:

- Input voltage range from 2.7 to 5.5 V
- Features an RTC linear regulator
- Has three high-efficiency buck converters (two bucks with Dynamic Voltage Scaling)
- Has a general linear regulator

The PF5020 offers a fully integrated and highly customizable solution to support the i.MX6 UL/ULL/ULZ system. The PF5020 is software compatible with the PF8100 and PF7100 PMIC solutions, reducing the effort of SW integration significantly.

How to design with the PF5020

PF5020 has integrated OTP (One Time Programming) fuses allowing to configurable the PMIC output voltages, sequencing, voltage monitoring, etc. to fit the application need.

Contact your NXP representative for detailed information on OTP fuse programming.

All PF5020 design documents and tools can be downloaded from nxp.com, search for PF5020.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

Table 1. i.MX6 ULZ Power Requirements

PF5020			i.MX6 ULZ		
Regulator	**Rated Current (mA)**	**Default Output Voltage(V)**	**Power Domain**	**Operating Voltage(V)[1]**	**Max Current (mA)[1]**
VSNVS	10	3.0	VDD_SNVS	2.4 to 3.6	0.5
BUCK1	2500	1.3875	VDD_SOC	1.375 to 1.5[2]	500[3]
BUCK2	2500	1.5/1.35/1.2	VDD_DDRIO	—	—
LDO	400	1.8	VDD_1V8	—	—
BUCK3	2500	3.3	VDD_3V3	—	—
			VDDHIGH	2.8 to 3.6	125

[1] The operating voltage range and maximum current are from the i.MX processor datasheet.
[2] The operating voltage range is specified with Run mode: LDO enabled, ARM operation on 900 MHz.
[3] The value is specified with Maximum current, and ARM frequency is 900 MHz based on Dhrystone test.

Table 2. i.MX6 ULL Power Requirements

PF5020			i.MX6 ULL		
Regulator	**Rated Current (mA)**	**Default Output Voltage(V)**	**Power Domain**	**Operating Voltage(V)[1]**	**Max Current (mA)[1]**
VSNVS	10	3.0	VDD_SNVS	2.4 to 3.6	0.5
BUCK1	2500	1.3875	VDD_SOC	1.325 to 1.5[2]	500[3]
BUCK2	2500	1.5/1.35/1.2	VDD_DDRIO	—	—
LDO	400	1.8	VDD_1V8	—	—
BUCK3	2500	3.3	VDD_3V3	—	—
			VDDHIGH	2.8 to 3.6	125

[1] The operating voltage range and maximum current are from the i.MX processor datasheet.
[2] The operating voltage range is specified with Run mode: LDO enabled, ARM operation on 792 MHz.
[3] The value is specified with Maximum current, and ARM frequency is 792 MHz based on Dhrystone test.

Table 3. i.MX6 UL Power Requirements

PF5020			i.MX6 UL		
Regulator	**Rated Current (mA)**	**Default Output Voltage(V)**	**Power Domain**	**Operating Voltage(V)[1]**	**Max Current (mA)[1]**
VSNVS	10	3.0	VDD_SNVS	2.4 to 3.6	0.5
BUCK1	2500	1.3875	VDD_SOC	1.375 to 1.5[2]	600[3]
BUCK2	2500	1.5/1.35/1.2	VDD_DDRIO	—	—
LDO	400	1.8	VDD_1V8	—	—
BUCK3	2500	3.3	VDD_3V3	—	—
			VDDHIGH	2.8 to 3.6	125

[1] The operating voltage range and maximum current are from the i.MX processor datasheet.
[2] The operating voltage range is specified with Run mode: LDO enabled.
[3] The value is specified with Maximum current, and ARM frequency is 696 MHz based on Dhrystone test.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

3 Power i.MX6 DualLite, Solo, SoloLite, SoloX with the PF5020

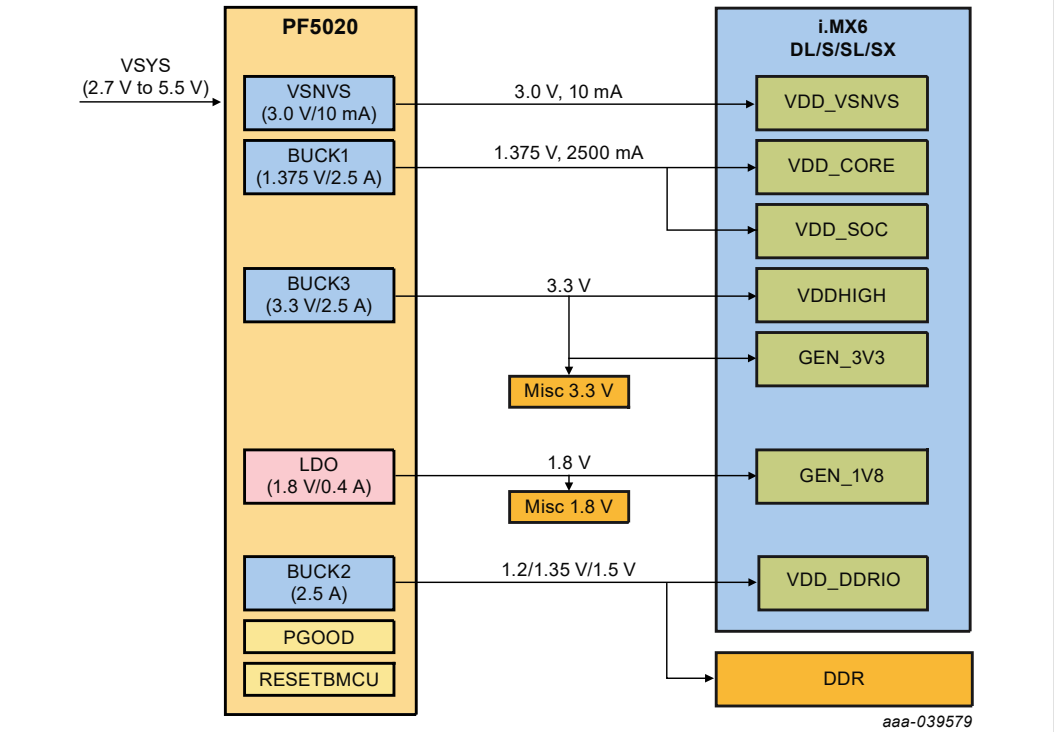

Figure 2. Simplified system power block diagram

The existing PMIC on i.MX6 DualLite, Solo, SoloLite reference design board is the NXP PF0100. The existing PMIC on i.MX6 SoloX reference design board is NXP PF0200.

The following reference design resources can be downloaded from nxp.com.

- i.MX6DL
- i.MX6S
- i.MX6SL
- i.MX6SX

Reasons why the PF5020 is an alternative solution to the PF0100 / 0200:

- Input voltage range from 2.7 to 5.5 V
- Features an RTC linear regulator
- Has three high-efficiency buck converters (two bucks with Dynamic Voltage Scaling)
- Has a general linear regulator
- Supports a watchdog timer / monitor and integrated regulators monitoring
- Offers safety features supporting ASIL B applications
- The ARM and SOC rails power consumption on i.MX6 DL/S/SL/SX processors are lower than i.MX Q/D processors, making it feasible to supply the ARM and SOC with a single 2.5A buck regulator.
- PF5020 offers a fully integrated and highly customizable solution to support the i.MX6 DualLite / Solo / SoloLite / SoloX systems. PF5020 is software compatible with the PF8100 and PF7100 PMIC solutions reducing the effort of SW integration significantly

How to design with the PF5020

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

PF5020 has integrated OTP (One Time Programming) fuses allowing to configurable the PMIC output voltages, sequencing, voltage monitoring, etc. to fit the application need.

Contact your NXP representative for detailed information on OTP fuse programming.

All PF5020 design documents and tools can be downloaded from the nxp.com, search for PF5020.

Table 4. i.MX6 DualLite and Solo power Requirements

PF5020			i.MX6 DL/S		
Regulator	**Rated Current (mA)**	**Default Output Voltage(V)**	**Power Domain**	**Operating Voltage(V)[1]**	**Max Current (mA)[1]**
VSNVS	10	3.0	VDD_SNVS	2.9 to 3.3	0.275
BUCK1	2500	1.375	VDD_ARM	1.275 to 1.5[2]	2200(DualLite) 1320(Solo)[3]
			VDD_SOC	1.275 to 1.5[2]	1260
BUCK2	2500	1.5/1.35/1.2	VDD_DDRIO	—	—
LDO	400	1.8	VDD_1V8	—	—
BUCK3	2500	3.3	VDD_3V3	—	—
			VDDHIGH	2.8 to 3.3	125

[1] The operating voltage range and maximum current are from the i.MX processor datasheet.
[2] The operating voltage range is specified with Run mode: LDO enabled, ARM operation on 792 MHz.
[3] The value is specified with Maximum current, and ARM frequency is 996 MHz based on power virus operation.

Table 5. i.MX6 SoloLite Power Requirements

PF5020			i.MX6 SL		
Regulator	**Rated Current (mA)**	**Default Output Voltage(V)**	**Power Domain**	**Operating Voltage(V)[1]**	**Max Current (mA)[1]**
VSNVS	10	3.0	VDD_SNVS	2.7 to 3.6	0.25
BUCK1	2500	1.375	VDD_ARM	1.275 to 1.5[2]	1100[3]
			VDD_SOC	1.275 to 1.5[2]	650
BUCK2	2500	1.5/1.2	VDD_DDRIO	—	—
LDO	400	1.8	VDD_1V8	—	—
BUCK3	2500	3.3	VDD_3V3	—	—
			VDDHIGH	2.8 to 3.3	30

[1] The operating voltage range and maximum current are from the i.MX processor datasheet.
[2] The operating voltage range is specified with Run mode: LDO enabled, ARM operation on 792 MHz.
[3] The value is specified with Maximum current, and ARM frequency is 1 GHz based on power virus operation.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

Table 6. i.MX6 SoloX Power Requirements

PF5020			i.MX6 SX		
Regulator	**Rated Current (mA)**	**Default Output Voltage(V)**	**Power Domain**	**Operating Voltage(V)[1]**	**Max Current (mA)[1]**
VSNVS	10	3.0	VDD_SNVS	2.4 to 3.6	0.4
BUCK1	2500	1.375	VDD_ARM	1.275 to 1.5[2]	1100[3]
			VDD_SOC	1.275 to 1.5[2]	1260
BUCK2	2500	1.5/1.35/1.2	VDD_DDRIO	—	—
LDO	400	1.8	VDD_1V8	—	—
BUCK3	2500	3.3	VDD_3V3	—	—
			VDDHIGH	2.8 to 3.6	125

[1] The operating voltage range and maximum current are from the i.MX processor datasheet.
[2] The operating voltage range is specified with Run mode: LDO enabled, ARM operation on 792 MHz.
[3] The value is specified with Maximum current, and ARM frequency is 996 MHz based on power virus operation.

4 Power i.MX6 SLL with the PF5020

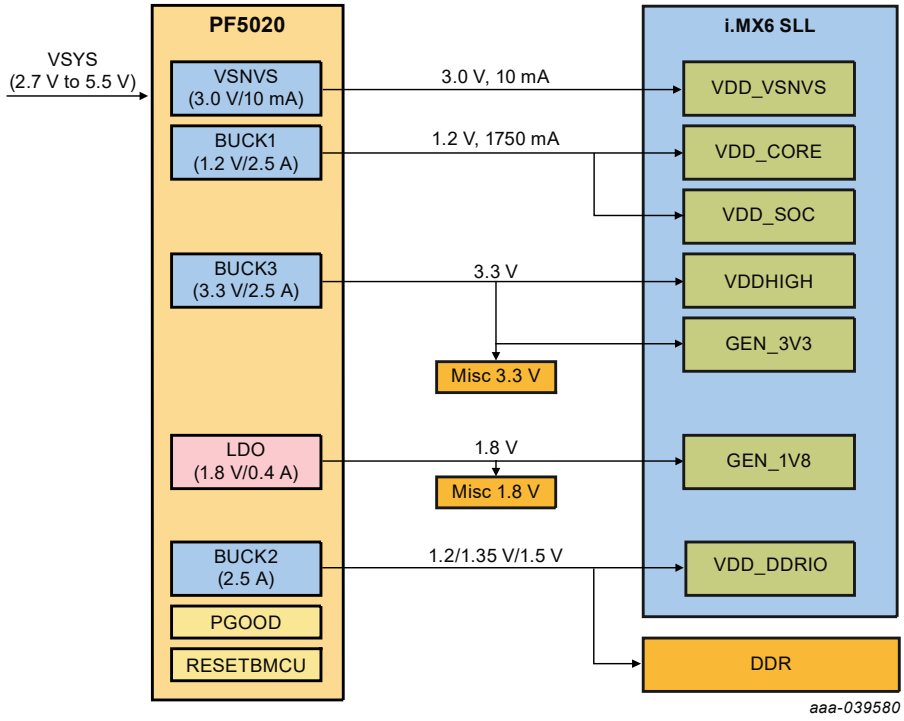

Figure 3. Simplified system power block diagram

The existing PMIC on i.MX6 SLL reference design board is the NXP PF0100. The following reference design resource can be downloaded from nxp.com.

- i.MX6SLL

Reasons why the PF5020 is an alternative solution to the PF0100:

- Input voltage range from 2.7 to 5.5 V
- Features an RTC linear regulator

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

- Has three high-efficiency buck converters (two bucks with Dynamic Voltage Scaling)
- Has a general linear regulator
- Supports a watchdog timer / monitor and integrated regulators voltage monitoring
- Offers safety features supporting ASIL B applications

The ARM and SOC rails power consumption on i.MX6 SLL processors is lower than i.MX high end processors, making it feasible to supply the ARM and SOC with a single 2.5A buck regulator.

PF5020 offers a fully integrated and highly customizable solution to support the i.MX6 SLL system. PF5020 is software compatible with the PF8100 and PF7100 PMIC solutions reducing the effort of SW integration significantly

How to design with the PF5020

PF5020 has integrated OTP (One Time Programming) fuses allowing to configurable the PMIC output voltages, sequencing, voltage monitoring, etc. to fit the application need.

Contact your NXP representative for detailed information on OTP fuse programming.

All PF5020 design documents and tools can be downloaded from the nxp.com, search for PF5020.

Table 7. i.MX6 SLL Power Requirements

PF5020			i.MX6 SLL		
Regulator	**Rated Current (mA)**	**Default Output Voltage(V)**	**Power Domain**	**Operating Voltage(V)[1]**	**Max Current (mA)[1]**
VSNVS	10	3.0	VDD_SNVS	2.4 to 3.6	0.5
BUCK1	2500	1.2	VDD_ARM	1.15 to 1.26[2]	1100[3]
			VDD_SOC	1.15 to 1.26[2]	650
BUCK2	2500	1.5/1.35/1.2	VDD_DDRIO	—	—
LDO	400	1.8	VDD_1V8	—	—
BUCK3	2500	3.3	VDD_3V3	—	—
			VDDHIGH	2.8 to 3.6	100

[1] The operating voltage range and maximum current are from the i.MX processor datasheet.
[2] The operating voltage range is specified with Run mode: ARM operation on 792 MHz.
[3] The value is specified with Maximum current, and ARM frequency is 800 MHz based on power virus operation.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

5 Power i.MX6 Quad, Dual with the PF7100

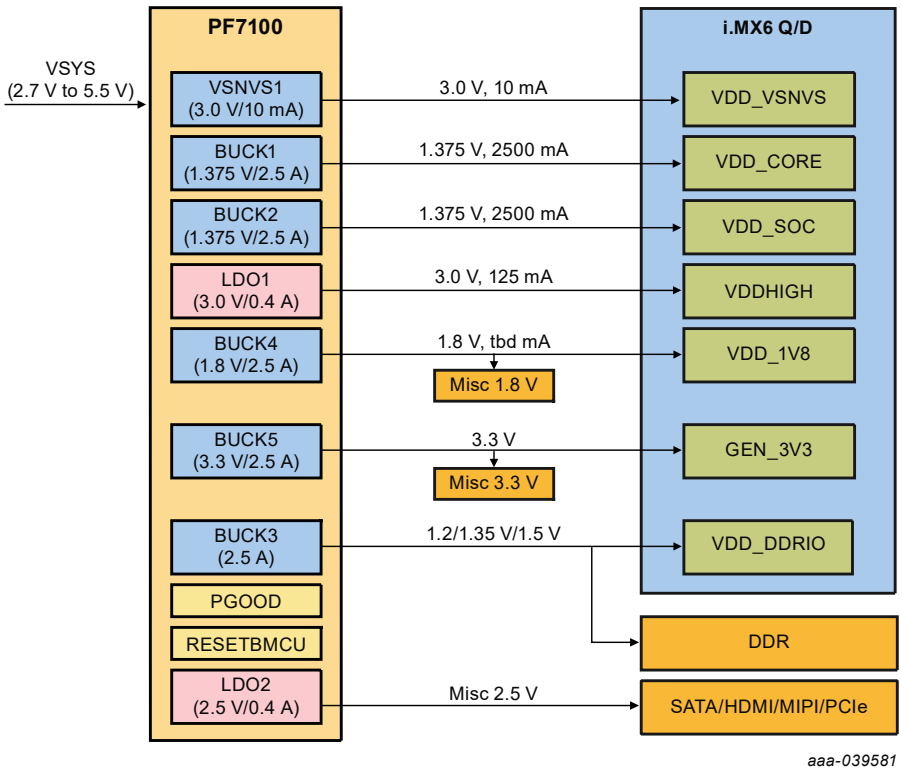

Figure 4. Simplified system power block diagram

Note:

The VDD_ARM is supplied with CoreMark current as specified on the processor datasheet.

The existing PMIC on i.MX6 Quad and Dual reference design boards is the NXP PF0100. The following reference design resources can be downloaded from nxp.com.

- i.MX6Q
- i.MX6D

Reasons why the PF7100 is an alternative solution to the PF0100:

- Input voltage range from 2.7 to 5.5 V
- Features two RTC linear regulators
- Has five high-efficiency buck converters (four bucks with Dynamic Voltage Scaling)
- Has two general linear regulators
- Supports a watchdog timer / monitor and integrated regulators voltage monitoring
- Offers safety features supporting ASIL B applications
- Offers a fully integrated and highly customizable solution to support the i.MX6 Quad / Dual system.
- PF7100 is already used on i.MX 8 reference designs with available drivers in the i.MX family BSP, making the switch to PF7100 effortless.

How to design with the PF7100

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

PF7100 has integrated OTP (One Time Programming) fuses allowing to configurable the PMIC output voltages, sequencing, voltage monitoring, etc. to fit the application need.

Contact your NXP representative for detailed information on OTP fuse programming.

All PF7100 design documents and tools can be downloaded from the nxp.com, search for PF7100.

Table 8. i.MX6 Quad and Dual Power Requirements

PF7100			i.MX6 Q/D		
Regulator	**Rated Current (mA)**	**Default Output Voltage(V)**	**Power Domain**	**Operating Voltage(V)[1]**	**Max Current (mA)[1]**
VSNVS1	10	3.0	VDD_SNVS	2.8 to 3.3	0.275
BUCK1	2500	1.375	VDD_ARM	1.275 to 1.5[2]	2500 (Quad) 1500 (Dual)[3]
BUCK2	2500	1.375	VDD_SOC	1.275 to 1.5[2]	2500
BUCK3	2500	1.5/1.35/1.2	VDD_DDRIO	—	—
BUCK4	2500	1.8	VDD_1V8	—	—
BUCK5	2500	3.3	VDD_3V3	—	—
LDO1	400	3.0	VDDHIGH	2.7 to 3.3	125
LDO2	400	2.5	VDD_2P5	—	—

[1] The operating voltage range and maximum current are from the i.MX processor datasheet.
[2] The operating voltage range is specified with Run mode: LDO enabled, ARM operation on 792 MHz.
[3] The value is specified with Maximum current CoreMark, ARM frequency is 996 MHz.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

6 Power i.MX6 QuadPlus, DualPlus with the PF7100

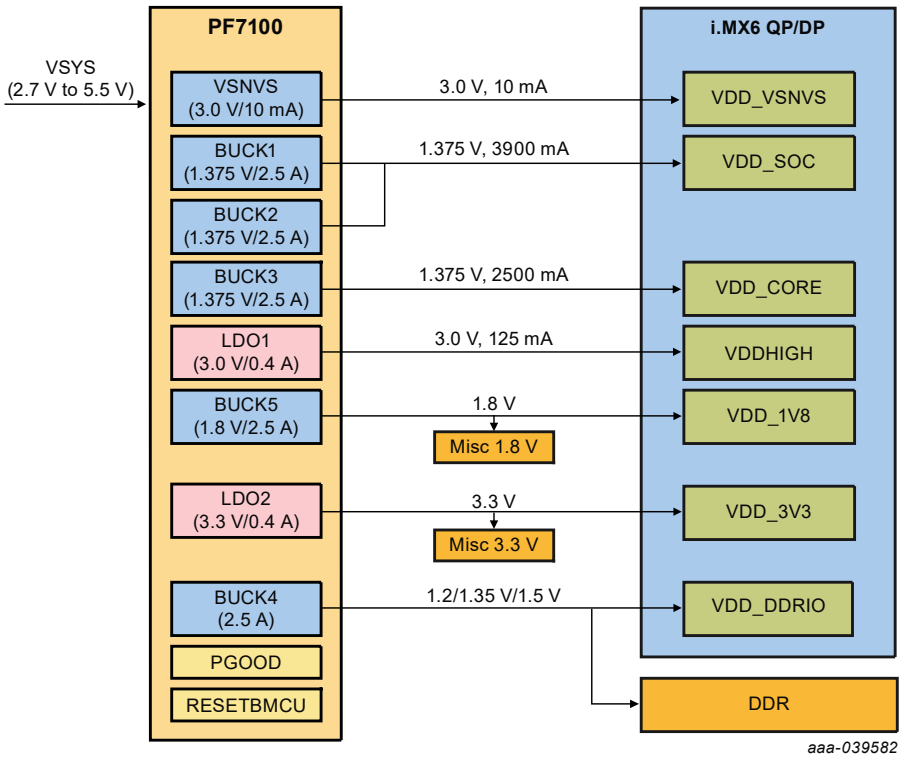

Figure 5. Simplified system power block diagram

Note:

The VDD_ARM is supplied with CoreMark current as specified on the processor datasheet.

The existing PMIC on i.MX6 QuadPlus, DualPlus reference design board is the NXP PF0100. The following reference design resources can be downloaded from nxp.com.

- i.MX6QP
- i.MX6DP

Reasons why the PF7100 is an alternative solution to the PF0100:

- Input voltage range from 2.7 to 5.5 V
- Features two RTC linear regulators
- Has five high-efficiency buck converters (four bucks with Dynamic Voltage Scaling)
- Has two general linear regulators
- Supports a watchdog timer / monitor and integrated regulators voltage monitoring
- Offers safety features supporting ASIL B applications
- The PF7100 is an alternative to the PF8100 as a highly customizable solution to support the i.MX6 QuadPlus / DualPlus system for limited use cases, such as VTT rail is not a must for the system or select PF7100 plus other discrete powers/PMIC for thermal consideration.
- PF7100 is already used on i.MX 8 reference designs with available drivers in the i.MX family BSP, making the switch to PF7100 effortless.

How to design with the PF7100

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

PF7100 has integrated OTP (One Time Programming) fuses allowing to configurable the PMIC output voltages, sequencing, voltage monitoring, etc. to fit the application need.

Contact your NXP representative for detailed information on OTP fuse programming.

All PF7100 design documents and tools can be downloaded from the nxp.com, search for PF7100.

Table 9. i.MX6 QuadPlus and DualPlus Power Requirements with PF7100

PF7100			i.MX6 QP/DP		
Regulator	**Rated Current (mA)**	**Default Output Voltage(V)**	**Power Domain**	**Operating Voltage(V)[1]**	**Max Current (mA)[1]**
VSNVS	10	3.0	VDD_SNVS	2.8 to 3.6	0.275
BUCK1 and Buck2 in dual phase	5000	1.375	VDD_SOC	1.275 to 1.5[2]	3900
BUCK3	2500	1.375	VDD_ARM	1.275 to 1.5[2]	2500 (Quad) 1200 (Dual)[3]
BUCK4	2500	1.5/1.35/1.2	VDD_DDRIO		
BUCK5	2500	1.8	VDD_1V8		
LDO1	400	3.0	VDDHIGH	2.7 to 3.6	125
LDO2	400	3.3	VDD_3V3		

[1] The operating voltage range and maximum current are from the i.MX processor datasheet.
[2] The operating voltage range is specified with Run mode: LDO enabled, ARM operation on 792 MHz, VPU ≤ 264MHz.
[3] The value is specified with Maximum current CoreMark, ARM frequency is 996 MHz.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

7 Power i.MX6 QuadPlus, DualPlus with the PF8100

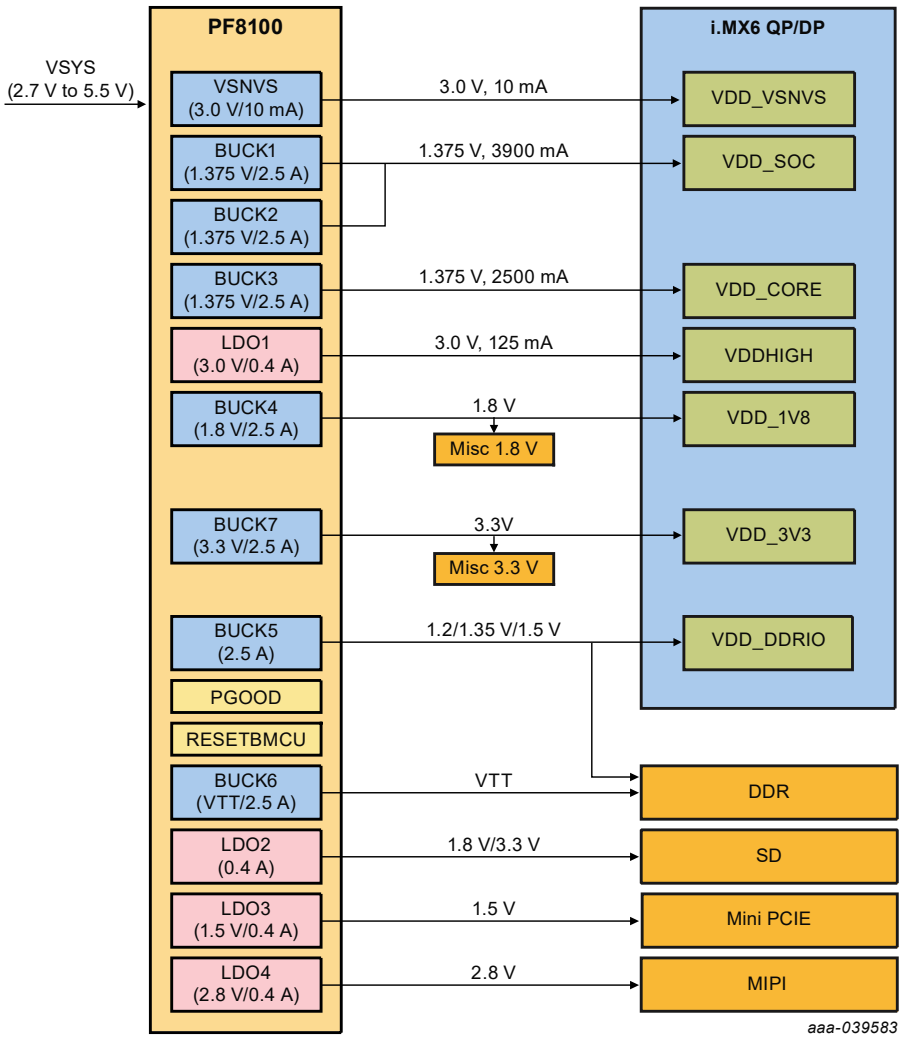

Figure 6. Simplified system power block diagram

Note:

The VDD_ARM is supplied with CoreMark current as specified on the processor datasheet.

The existing PMIC on i.MX6 QuadPlus, DualPlus reference design board is the NXP PF0100. The following reference design resources can be downloaded from nxp.com.

- i.MX6QP
- i.MX6DP

Reasons why the PF8100 is an alternative solution to the PF0100:

- Input voltage range from 2.7 to 5.5 V
- Features an RTC linear regulators
- Up to seven high-efficiency buck converters (six bucks with Dynamic Voltage Scaling)
- Has four general linear regulators
- Supports a watchdog timer / monitor and integrated regulators voltage monitoring

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

- PF8200 is a PF8100 pin-to-pin compatible device offering safety features supporting ASIL B applications.
- PF8100 offers a fully integrated and highly customizable solution to support the i.MX6 QuadPlus / DualPlus system without additional buck and LDO regulators.
- PF8100 is already used on i.MX 8 reference designs with available drivers in the i.MX family BSP, making the switch to PF8100 effortless.

How to design with the PF8100

PF8100 has integrated OTP (One Time Programming) fuses allowing to configurable the PMIC output voltages, sequencing, voltage monitoring, etc. to fit the application need.

Contact your NXP representative for detailed information on OTP fuse programming.

All PF8100 design documents and tools can be downloaded from the nxp.com, search for PF8100.

Table 10. i.MX6 QuadPlus and DualPlus Power Requirements with PF8100

PF8100			i.MX6 QP/DP		
Regulator	**Rated Current (mA)**	**Default Output Voltage(V)**	**Power Domain**	**Operating Voltage(V)[1]**	**Max Current (mA)[1]**
VSNVS	10	3.0	VDD_SNVS	2.8 to 3.6	0.275
BUCK1 and 2 in dual phase	5000	1.375	VDD_SOC	1.275 to 1.5[2]	3900
BUCK3	2500	1.375	VDD_ARM	1.275 to 1.5[2]	2500 (Quad) 1200 (Dual)[3]
BUCK4	2500	1.8	VDD_1V8		
BUCK5	2500	1.5/1.35/1.2	VDD_DDRIO		
BUCK6	2500	BUCK5 output voltage divided by 2	VTT mode[4]		
BUCK7	2500	3.3	VDD_3V3		
LDO1	400	3.0	VDDHIGH	2.7 to 3.6	125
LDO2	400	1.8/3.3	SD		
LDO3	400	1.5	Mini PCIE		
LDO4	400	2.8	MIPI		

[1] The operating voltage range and maximum current are from the i.MX processor datasheet.
[2] The operating voltage range is specified with Run mode: LDO enabled, ARM operation on 792 MHz, VPU ≤ 264MHz.
[3] The value is specified with Maximum current CoreMark, ARM frequency is 996 MHz.
[4] BUCK6 can be used as a general 2.5A DC BUCK, if not used as VTT mode.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

8 Appendix — PF devices comparison

Table 11. PF devices comparison

Function	PF0100 PF0200 QM	PF1550 QM	PF1510 QM	PF3000 QM	PF3001 QM	PF8100 QM	PF8200 ASIL B	PF7100 QM	PF7100 ASIL B	PF5020 QM	PF5020 ASIL B
VIN operation range	2.8 – 4.5 V	4.1 – 6.0 V		2.8 – 4.5 V 3.7 – 5.5 V		2.7 – 5.5 V		2.7 – 5.5 V		2.7 – 5.5 V	
Buck regulator w/DVS	6ch / PF0100 4ch / PF0200	3ch		4ch / PF3000 3ch / PF3001		6ch		4ch		2ch	
Dual phase operation	Yes	—		PF3000 only		Yes		Yes		Yes	
Triple phase operation	—	—		—		Yes		Yes		—	
Quad phase operation	—	—		—		Yes		Yes		—	
Buck regulator w/o DVS	—	—		—		1ch		1ch		1ch	
Buck output current per channel	1 to 2.5 A	1 A		1 to 1.75 A / PF3000 1.25 to 2.75 A / PF3001		2.5 A		2.5 A		2.5 A	
LDO	6ch	3ch		6ch		4ch		2ch		1ch	
LDO output current per channel	100 to 350 mA	300 to 400 mA		100 to 350 mA		400 mA		400 mA		400 mA	
LDO output voltage	0.8 to 1.55 V / 1.8 to 3.3 V	0.75 to 1.5 V / 1.8 to 3.3V		0.8 to 1.55 V / 1.8 to 3.3 V		1.5 to 5 V		0.8 to 5 V		1.5 to 5 V	
Selectable switch mode	—	Yes		—		Yes		Yes		Yes	
Boost regulator	1ch	—		PF3000 only		—		—		—	
Boost output current	0.6 A	—		0.6 A		—		—		—	
Boost output voltage	5.0 to 5.15 V	—		5.0 to 5.15 V		—		—		—	
Battery linear charger	—	PF1550 only		—		—		—		—	
Charger output voltage	—	3.5 to 4.44 V		—		—		—		—	
Charger output current	—	100 to 1000 mA		—		—		—		—	
VSNVS regulator	1ch	1ch		1ch		1ch		2ch		1ch	
VSNVS voltage selection	1.0/1.1/1.2/1.3/ 1.5/1.8/3.0 V	3.0 V		3.0 V		1.8/3.0/3.3 V		VSNVS1 1.8/3.0/3.3 V VSNVS2 0.8/0.9/1.8 V		1.8/3.0/3.3 V	
VSNVS current per channel	400 µA	2 mA		1 mA		10 mA		10 mA		10 mA	
Coin cell charger	Yes	Yes		Yes		Yes		—		—	
AMUX output	—	—		—		1ch		1ch		—	

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

Table 11. PF devices comparison...*continued*

Function	PF0100 PF0200 QM	PF1550 QM	PF1510 QM	PF3000 QM	PF3001 QM	PF8100 QM	PF8200 ASIL B	PF7100 QM	PF7100 ASIL B	PF5020 QM	PF5020 ASIL B
Communication I/F	I2C	I2C		I2C		I2C with CRC		I2C with CRC		I2C with CRC	
Watchdog	—	—		—		Yes		Yes		Yes	
MCU I/F	PWRON, STANDBY, INTB, RESETBMCU, SDWNB	PWRON, STANDBY, INTB, RESETBMCU		PWRON, STANDBY, INTB, RESETBMCU		PWRON, STANDBY, INTB, XINTB, EWARN, FSOB, RESETBMCU, XFAILB, PGOOD, WDI		PWRON, STANDBY, INTB, XINTB, EWARN, FSOB, RESETBMCU, XFAILB, PGOOD, WDI		PWRON, STANDBY, INTB, RESETBMCU, PGOOD, PGOODx, ENx, XFAILB, WDI	
OV/UV monitoring	—	—		—		Yes		Yes		Yes	
OTP program	Yes	Yes		Yes		Yes		Yes		Yes	
ABIST	No	No		No		No	Yes	No	Yes	No	Yes
20 MHz CLK check	No	No		No		No	Yes	No	Yes	No	Yes
OTP CRC check	No	No		No		No	Yes	No	Yes	No	Yes
Fail-Safe state	No	No		No		No	Yes	No	Yes	No	Yes
Secure I2C write	No	No		No		No	Yes	No	Yes	No	Yes
Target ASIL class	QM	QM		QM		QM	ASIL B	QM	ASIL B	QM	ASIL B
Package	QFN56	QFN40		QFN48		HVQFN56		HVQFN48		HVQFN40	

9 References

The following are URLs where the user can obtain information on related NXP products and application solutions.

Ref.	Item	Description	Link
[1]	PF0100	Product summary page	https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/14-channel-configurable-power-management-ic:MMPF0100
[2]	PF0200	Product summary page	https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/12-channel-configurable-power-management-ic:MMPF0200
[3]	PF1550	Product summary page	https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/pmic-with-1a-li-plus-linear-battery-charger-for-low-power-processor-systems:PF1550
[4]	PF1510	Product summary page	https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/power-management-integrated-circuit-pmic-for-low-power-application-processors:PF1510

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

Ref.	Item	Description	Link
[5]	PF3000	Product summary page	https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/12-channel-configurable-pmic:PF3000
[6]	PF3001	Product summary page	https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/10-channel-configurable-pmic:PF3001
[7]	PF5020	Product summary page	https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/multi-channel-5-pmic-for-automotive-applications-4-high-power-and-1-low-power-fit-for-asil-b-safety-level:PF5020
[8]	PF7100	Product summary page	https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/7-channel-power-management-integrated-circuit-for-high-performance-applications-fit-for-asil-b-safety-level:PF7100
[9]	PF8100	Product summary page	https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/12-channel-power-management-integrated-circuit-pmic-for-high-performance-processing-applications:PF8100-PF8200
[10]	PF8200	Product summary page	https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/12-channel-power-management-integrated-circuit-pmic-for-high-performance-processing-applications:PF8100-PF8200
[11]	i.MX 6 Series applications processors	Product summary page	https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-6-processors:IMX6X_SERIES

10 Revision history

Revision history

Rev	Date	Description
1	20201104	Initial version

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

11 Legal information

11.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

11.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer. In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages. Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

11.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

Tables

Figures

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2020. All rights reserved.

Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2020. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 4 November 2020
Document identifier: AN12992