AN13049

Wi-Fi/Bluetooth M.2 Key E Pinout Definition

Rev. 2 — 16 September 2021 Application Note

Contents

1 Introduction

M.2 is a form factor for mobile adapters defined by the PCI-SIG (http://www.pcisig.com). The pinouts for M.2 sockets are defined in the PCI Express M.2 Specification.

M.2 sockets with mechanical Key E are used on platforms based on NXP MPUs and MCUs to support wireless connectivity modules based on NXP Wi-Fi/Bluetooth radios.

Some of the signals defined in the pinout are used to connect optional sideband and debug signals used by NXP Wi-Fi/Bluetooth radios.

In order to ensure the proper connection for sideband and debug signals, this document defines the pin assignments for M.2 sockets (mechanical Key E) on platforms based on NXP MPUs and MCUs.

Before building your board, check the interface connector specification from the wireless module vendor to confirm the pinout used by the module.

For the full definition of the socket pinout, refer to the *PCI Express M.2 Specification*, available from PCI-SIG website (http://www.pcisig.com).

NOTE

All the pins that are not listed in this document are recommended to follow the PCI Express M.2 Type E specification or should *not be connected*.

2 Sideband and debug signals

Table 1 shows the pin assignments utilized for sideband and debug signals.

Note: *Check the module datasheet for details on mandatory and optional lines.*

Table 1. Sideband and debug signals

Pin	PCIe M.2 Signal	Type[1]	Voltage	NXP Usage	Description
20	UART_WAKE#	I	3.3 V	BT_WAKE_HOST	Sideband signal used by the Bluetooth radio to wake up the platform. Active Low by default Connect to Host GPIO Open drain. Pullup required on platform.
21	SDIO_WAKE#	I	1.8 V	WLAN_WAKE_HOST	Sideband signal used by the Wi-Fi radio to wake up the platform. Active Low by default Connect to Host GPIO Open drain. Pullup required on platform.

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Table 1. Sideband and debug signals (continued)

Pin	PCIe M.2 Signal	Type[1]	Voltage	NXP Usage	Description
23	SDIO_RESET#	O	1.8 V	WLAN_INDEPENDENT_ RESET	Sideband signal to independently reset the Wi-Fi radio. Active Low by default Connect to Host GPIO.
38	VENDOR DEFINED	I/O	1.8 V	JTAG_TDO	Used for debug. Connect to JTAG header on platform.
40	VENDOR DEFINED	O	1.8 V	DEV_WLAN_WAKE / COEX4	Sideband signal used by the platform to wake up the Wi-Fi radio. Active Low. Connect to Host GPIO.
42	VENDOR DEFINED	O	1.8 V	DEV_BT_WAKE	Sideband signal used by the platform to wake up the Bluetooth radio. Radio Coexistence line 4. Active Low. Connect to Host GPIO.
44	COEX3	I/O	1.8 V	JTAG_TDI / COEX3	Radio Coexistence line 3. Used for debug. Connect to JTAG header on platform.
46	COEX2	I/O	1.8 V	JTAG TCK / COEX2	Radio Coexistence line 2. Used for debug. Connect to JTAG header on platform.
48	COEX1	I/O	1.8 V	JTAG_TMS / COEX1	Radio Coexistence line 1. Used for debug. Connect to JTAG header on platform.
54	W_DISABLE2#	O	3.3 V	BT_INDEPENDENT_ RESET	Sideband signal to independently reset the Bluetooth radio. Active Low by default Connect to Host GPIO.
56	W_DISABLE1#	O	3.3 V	PDn	Full Power-down for the Wi-Fi/Bluetooth radio: High = normal mode. Low = full power-down mode Connect to Host GPIO.

1. Type refers to the signal direction:
   - Type O means signal is an output from the MPU/MCU to the adapter.
   - Type I means signals is an input to the MPU/MCU from the adapter.

3 Host and audio interfaces

The wireless connectivity modules may support a PCM/I2S audio interface.

The modules may also support various host interfaces including SDIO, UART, or PCI Express. To confirm the supported interfaces, see the module datasheet.

The tables below show the pin assignments for these interfaces.

Table 2. PCM/I2S pin assignments

Pin #	Name	Type	Voltage	Description
8	PCM_CLK/I2S_SCK	I/O	1.8 V	PCM data clock
10	PCM_SYNC/I2S_WS	I/O	1.8 V	PCM frame sync
12	PCM_IN/I2S_SD_IN	I	1.8 V	Receive PCM Input
14	PCM_OUT/ I2S_SD_OUT	O	1.8 V	Transmit PCM Output

Table 3. SDIO pin assignments

Pin #	Name	Type	Voltage	Description
9	SDIO_CLK	O	1.8 V	SDIO Clock
11	SDIO_CMD	I/O	1.8 V	SDIO Command
13	SDIO_DATA0	I/O	1.8 V	SDIO_DATA0
15	SDIO_DATA1	I/O	1.8 V	SDIO_DATA1
17	SDIO_DATA2	I/O	1.8 V	SDIO_DATA2
19	SDIO_DATA3	I/O	1.8 V	SDIO_DATA3

NOTE

CTS and RTS flow control lines are requested for Bluetooth control.

Table 4. UART pin assignments

Pin #	Name	Type	Voltage	Description
22	UART_RXD	I	1.8 V	UART Receive
32	UART_TXD	O	1.8 V	UART Transmit
34	UART_CTS	I	1.8 V	UART Clear-To-Send
36	UART_RTS	O	1.8 V	UART Request-To-Send

Table 5. PCI Express pin assignments

Pin #	Name	Type	Voltage	Description
35	PETP0	O	1.8 V	PCIe Tx
37	PETPN	O	1.8 V	PCIe Tx
41	PERP0	I	1.8 V	PCIe Rx

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Table 5. PCI Express pin assignments (continued)

Pin #	Name	Type	Voltage	Description
43	PERN0	I	1.8 V	PCIe Rx
47	REFCLKP0	O	1.8 V	PCIe Reference Clock
49	REFCLKN0	O	1.8 V	PCIe Reference Clock
52	PERST0#	O	3.3 V	PCIe interface Reset
53	CLKREQ0#	I/O	3.3 V	PCIe Clock Request
55	PEWAKE0#	I/O	3.3 V	PCIe PME Wake
59	PETP1	O	1.8 V	PCIe Tx
61	PETN1	O	1.8 V	PCIe Tx
65	PERP1	I	1.8 V	PCIe Rx
67	PERN1	I	1.8 V	PCIe Rx
71	REFCLKP1	O	1.8 V	PCIe Reference Clock
73	REFCLKN1	O	1.8 V	PCIe Reference Clock

4 Revision history

Table 6 summarizes the changes done to this document since the initial release.

Table 6. Revision history

Revision number	Date	Substantive changes
1	12 November 2020	Initial release
2	16 September 2021	Updated Introduction and Sideband and debug signals

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