1 How to read the application note

All LPC55(S)xx products have two crystal oscillators: A 16 MHz crystal oscillator and a 32 KHz crystal oscillator.

Each crystal oscillator has one embedded capacitor bank, which is always enabled and its capacitance can be adjusted in certain range (IEC equivalent capacitive load: 6 - 10 pF). The capacitor bank can be used as integrated load capacitors for the crystal oscillators, which helps save external load capacitors of the crystal and hence the system BOM cost.

This application note provides a short introduction to this capacitor bank or Cap Bank, and describes how to apply this function to the actual design.

2 Advantage of embedded Cap Bank

The advantages of the embedded Cap Bank are as follows:

- Conserves component area on the PCB.
- Saves Bill of Materials (BOM).
- Maintains a Capacitive Load (CL) between 6 - 10 pF (IEC equivalent).
- Relies on simple APIs to configure the Capacitor Banks based on the crystal Capacitive Load (CL) and measured PCB parasitic capacitances on the XIN and XOUT pins.

3 Understanding Cap Bank

3.1 Cap Bank block diagram

The following figure shows the equivalent internal Cap Bank block with a standard crystal connection diagram.
Figure 1. Cap Bank block diagram

- Cb1, Cb2: Total equivalent capacitor including capacitor bank, package, and pad parasitic capacitors in MCU in single ended mode (i.e., on single crystal pin)
- Cp1, Cp2: Equivalent PCB parasitic capacitances on the PCB board in single ended mode
- Cx1, Cx2: User external crystal load capacitors used in single ended mode (i.e., on each crystal pin)

The single ended total capacitive load seen by the external crystal:

\[
CL_{tot\_se1} = C_b1 + C_p1 + C_x1; \quad (tot \text{ is short for total})
\]

\[
CL_{tot\_se2} = C_b2 + C_p2 + C_x2;
\]

The total IEC equivalent capacitive load seen by the external crystal (or CL) is the series of both single ended total capacitive loads:

\[
CL_{tot\_IEC} = CL = (CL_{tot\_se1} \cdot CL_{tot\_se2})/(CL_{tot\_se1} + CL_{tot\_se2}).
\]

3.2 Cap Bank specification in LPC55(S)xx

- Cb1 and Cb2 are equal.
- Cb1 or Cb2 is 12pF - 20pF, so the range of IEC equivalent crystal load capacitance value for internal Cap Bank is 6pF - 10pF.
- The reset value (default value) of Cb1 or Cb2 is 12pF, so the reset IEC equivalent crystal load capacitance is 6pF.
- All these values are guaranteed at factory across the device working temperature range.

4 Use cases

Crystal Load capacitance (CL) value can be easily found in the crystal data sheet. For example, 6pF, 8pF, 10pF, 12pF, and so on. The aforementioned CLtot_IEC, total IEC equivalent capacitive load needed for crystal is equal to CL.

Firstly, CLtot_IEC (or CL) needs to be converted into single ended total capacitive value as follows:

\[
CL_{tot\_se1} = CL_{tot\_se2} = 2 \cdot CL_{tot\_IEC} = 2 \cdot CL
\]

Secondly, the parasitic capacitances of the PCB (Cp1 and Cp2) related to the crystal on the PCB board need be measured.
Then the following results are calculated:

\[
\begin{align*}
C_{b1} + C_{x1} &= C_{\text{Ltot}\_se1} - C_{p1} = C_L - C_{p1} \\
C_{b2} + C_{x2} &= C_{\text{Ltot}\_se2} - C_{p2} = C_L - C_{p2}
\end{align*}
\]

The following sections show different configurations of \(C_{b1/2}\) and \(C_{x1/2}\) for different use cases.

4.1 Use case 1: \(C_L\) (or \(C_{\text{Ltot}\_IEC}\)) = 8pF, \(C_{p1} = 2pF, C_{p2} = 3pF\)

Assume a crystal with load capacitance \(C_L\) of 8pF is used, then

\[
\begin{align*}
C_{b1} + C_{x1} &= C_{\text{Ltot}\_se1} - C_{p1} = 2*8pF - 2pf = 14pF \\
C_{b2} + C_{x2} &= C_{\text{Ltot}\_se2} - C_{p2} = 2*8pF - 3pf = 13pF
\end{align*}
\]

Because the range of \(C_{b1}\) and \(C_{b2}\) values are 12pF - 20pF, which already covers the above calculated expected capacitance 14pF/13pF, the \(C_{x1}\) and \(C_{x2}\) values can be zero. In other words, there is no need to add \(C_{x1}\) and \(C_{x2}\) on PCB. This can save components and PCB area.

Therefore, just configure \(C_{b1} = 14pF, C_{b2} = 13pF\). Because \(C_{b1}\) and \(C_{b2}\) are equal in LPC55(S)xx, the maximum value between them is taken normally.

Therefore, \(C_{b1} = C_{b2} = 14pF\).

4.2 Use case 2: external crystal load capacitor needed

Assume a crystal with load capacitance \(C_L\) of 15pF is used, then

\[
\begin{align*}
C_{\text{Ltot}\_IEC} &= C_L = 15pF, C_{p1} = 2pF, C_{p2} = 2pF \\
C_{b1} + C_{x1} &= C_{\text{Ltot}\_se1} - C_{p1} = 2*15pF - 2pf = 28pF \\
C_{b2} + C_{x2} &= C_{\text{Ltot}\_se2} - C_{p2} = 2*15pF - 2pf = 28pF
\end{align*}
\]

Because the range of \(C_{b1}\) and \(C_{b2}\) values are 12pF - 20pF, which is below the above calculated expected capacitance 28pF, the \(C_{x1}\) and \(C_{x2}\) are needed. In other words, \(C_{x1}\) and \(C_{x2}\) must be added on PCB.

In this case, the recommended values of \(C_{b1}\) and \(C_{b2}\) are taken as 16pF normally.

Therefore, \(C_{x1}/x2\) can be derived as follows:

\[
\begin{align*}
C_{b1} &= C_{b2} = 16pF \\
C_{x1} &= C_{x2} = 28pF - 16pF = 12pF
\end{align*}
\]

\[\text{NOTE}\]

If Cap Bank is not configured, \(C_{b1}\) and \(C_{b2}\) keep the default value, which is 12pF.

In this case, \(C_{x1}/x2\) can be derived as follows:

\[
\begin{align*}
C_{b1} &= C_{b2} = 12pF \\
C_{x1} &= C_{x2} = 28pF - 12pF = 16pF
\end{align*}
\]

5 Capacitor Banks API description

Capacitor banks API routines are used to configure the Cap Bank values of \(C_{b1}\) and \(C_{b2}\).

For user convenience, it only requires users to provide \(C_{bp}\), \(C_{p1}\), and \(C_{p2}\).

Here, \(C_{bp}\) is the actual IEC equivalent load capacitance from crystal point of view \textbf{without} extra capacitors \(C_{x1}, C_{x2}\), that is, \(C_{bp}\) is:

\[
C_{bp} = (C_{b1} + C_{p1}) * (C_{b2} + C_{p2})/(C_{b1} + C_{p1}) + (C_{b2} + C_{p2})
\]
1. If $C_{bp} = CL$, it does not need to add external crystal load capacitor $Cx_1$ and $Cx_2$. That is, if there is no need to add external crystal load capacitor $Cx_1$ and $Cx_2$ per use case 1 in section 4.1 (i.e., CL is within the range of 6 - 10 pF), then the $C_{bp}$ is equal to total IEC equivalent capacitive load $CL_{tot_IEC}$ or the crystal load capacitance $CL$:

$$C_{bp} = CL_{tot_IEC} = CL;$$

See the equivalent diagram below.

![Equivalent diagram](image1)

**Figure 2. Equivalent diagram**

2. If $C_{bp} < CL$, then the external crystal load capacitance $Cx$ must be added. That is, if there is need to add $Cx_1$ and $Cx_2$ per use case 2 in section 4.2, and $C_{bp} + Cx = CL_{tot_IEC} = CL$, Where $Cx = (Cx_1 \times Cx_2)/(Cx_1 + Cx_2)$, then the external load capacitance $Cx$ can be derived by: $Cx = CL - C_{bp}$.

Assume $Cx_1 = Cx_2$, then $Cx_1 = Cx_2 = 2 \times Cx = 2 \times (CL - C_{bp})$.

In this case, it is recommended that the internal Cap Bank value $Cb_1, Cb_2 = 16$ pF.

See the equivalent diagram below.

![Equivalent diagram](image2)

**Figure 3. Equivalent diagram**

$Cp_1$ and $Cp_2$ are related to the board, the user needs to provide their values to the Cap Bank API function as the second and third parameters after measurement.
CL can be found in the crystal data sheet, so Cbp can be easily derived as mentioned previously and passed to the Cap Bank API routine as the first parameter.

5.1 API routines
There is only one routine for each crystal oscillator as follows.

Table 1. API routines

<table>
<thead>
<tr>
<th>Function prototype</th>
<th>API description</th>
</tr>
</thead>
</table>
| void POWER_Xtal16mhzCapbankTrim(int32_t pi32_16MfXtalIecLoadpF_x100, int32_t pi32_16MfXtalPPcbParCappF_x100, int32_t pi32_16MfXtalNPcbParCappF_x100); | This API configures the internal Capacitor Bank of the 16 MHz crystal oscillator, where parameters:
pi32_16MfXtalIecLoadpF_x100: Cbp (pF) x 100;
pi32_16MfXtalPPcbParCappF_x100: Cp1 (pF) x 100;
pi32_16MfXtalNPcbParCappF_x100: Cp2 (pF) x 100; |
| void POWER_Xtal32mhzCapbankTrim(int32_t pi32_32kfXtalIecLoadpF_x100, int32_t pi32_32kfXtalPPcbParCappF_x100, int32_t pi32_32kfXtalNPcbParCappF_x100); | This API configures the Capacitor Bank of the 32 KHz crystal oscillator, where parameters:
pi32_32kfXtalIecLoadpF_x100: Cbp (pF) x 100;
pi32_32kfXtalPPcbParCappF_x100: Cp1 (pF) x 100;
pi32_32kfXtalNPcbParCappF_x100: Cp2 (pF) x 100; |

In each routine, there are three parameters needed (Cbp, Cp1, Cp2). The unit of parameters is one hundredth pF.

For example, if

Cbp = 8.5pF, Cp1 = 2pF, Cp2 = 3pF.

Then, the call to API should be POWER_Xtal16mhzCapbankTrim (850,200,300).

5.2 API usage examples
This section explains the API usage examples described in the device's user manual.

5.2.1 16 MHz Crystal Oscillator

5.2.1.1 Example 1: 8pF IEC Capacitance Load, 2pF PCB parasitic capacitance on XIN pin, 3pF PCB parasitic capacitance on XOUT pin.

According to the conditions of this example, CLtot_IEC, Cp1/p2 are:

CLtot_IEC = CL = 8pF, Cp1 = 2pF, Cp2 = 3pF.

Because CL is within the range of 6 - 10 pF, it does not need to add external crystal load capacitor Cx1 and Cx2, and the Cbp is equal to CL = 8pF.

Therefore, the call to Cap Bank API routine should be: XTAL_16mhz_capabank_trim(8 * 100, 2 * 100, 3 * 100).

NOTE
Cb1 should be equal to Cb2 and be set to the maximum value of Cb1 and Cb2.

The system connection as follows:
5.2.1.2 Example 2: 15pF IEC Capacitance Load, 2pF PCB parasitic capacitance on XIN pin, 2pF PCB parasitic capacitance on XOUT pin.

According to the conditions of this example, $\text{CL}_{\text{tot}}_{\text{IEC}}$, $C_p1/p2$ are:

$\text{CL}_{\text{tot}}_{\text{IEC}} = \text{CL} = 15\text{pF}$, $C_p1 = 2\text{pF}$, $C_p2 = 2\text{pF}$.

Because $\text{CL}$ exceeds 10 pF, external crystal load capacitance $C_x$ must be added.

In another words, the user needs to add $C_x1$ and $C_x2$ per use case 2 in Section 4.2.

$C_b + C_x = \text{CL}_{\text{tot}}_{\text{IEC}} = \text{CL}$;

Then, the external load capacitance $C_x$ can be derived by:

$C_x = \text{CL} - C_b$;

Assume $C_x1 = C_x2$, then $C_x1 = C_x2 = 2* C_x = 2*(\text{CL} - C_b)$

In this case, it is recommended that the internal Cap Bank value $C_b1$, $C_b2 = 16\text{pF}$.

Therefore:

$C_b = (C_b1+C_p1) * (C_b2+C_p2)/((C_b1+C_p1) + (C_b2+C_p2)) = 9\text{pF}$.

$C_x1 = C_x2 = 2*C_x = 2*(\text{CL} - C_b) = 12\text{pF}$.

The call to Cap Bank API routine should be: `XTAL_16mhz_capabank_trim(9 * 100, 2 * 100, 2 * 100)`;

The system connection as follows:
5.2.2 32 KHz Crystal Oscillator

5.2.2.1 Example 3: 8pF IEC Capacitance Load, 2pF PCB parasitic capacitance on XIN pin, 3pF PCB parasitic capacitance on XOUT pin.

This is the same as example 1 aforementioned.

Therefore, the call to Cap Bank API routine should be: 

```
XTAL_32kHz_capabank_trim(8 * 100, 2 * 100, 3 * 100);
```

it docs not need to add extra capacitors on PCB.

The crystal system connection is as follows:

![Figure 5. System connection](image-url)
5.2.2.2 Example 4: 15pF IEC Capacitance Load, 2pF PCB parasitic capacitance on XIN pin, 2pF PCB parasitic capacitance on XOUT pin.

This is the same as example 2 aforementioned.

Therefore, the call to Cap Bank API routine should be: `XTAL_32kHz_capabank_trim(9 * 100, 2 * 100, 2 * 100);`

And the user needs to add extra capacitors on PCB: \( C_{x1} = C_{x2} = 12\text{pF} \).

The crystal system connection is as follows:
6 SDK example

Here is an example code that shows how to configure the internal Cap Bank, and how to fine tune it to achieve the best accuracy of crystal oscillator output on the existing PCB.

6.1 Hardware preparation

There are two external crystal oscillators on the board: 16 MHz and 32.768 KHz. This application note uses 32.768 KHz as an example to describe how to configure the Cap Bank function.

The part number of the 32k crystal on the EVK board is NX3215SA-32.768K-STD-MUS-2. It can be concluded from the manual that its IEC Capacitance Load (CL) is 12.5 pF, which does exceed the Cap Bank trim range of LPC5500 (6 – 10 pF).

Therefore, Cbp < CL, and the external crystal load capacitance Cx must be added. In another words, the user needs to add Cx1 and Cx2 per use case 2 in Section 4.2, and

\[ C_{xb} + C_x = C_{tot_IEC} = C_L; \]

Where \( C_x = \frac{C_{x1} * C_{x2}}{C_{x1} + C_{x2}} \).

Then, the external load capacitance Cx can be derived by:

\[ C_x = C_L - C_{xb}; \]

Assume \( C_{x1} = C_{x2} \), then \( C_{x1} = C_{x2} = 2*C_x = 2*(C_L - C_{xb}); \)

In this case, it is recommended that the internal Cap Bank value \( C_b1, C_b2 = 16 \) pF, and \( C_p1 = 1 \) pF, \( C_p2 = 1 \) pF.

Therefore,

\[ C_{xb} = (C_{b1}+C_{p1}) * (C_{b2}+C_{p2})/((C_{b1}+C_{p1}) + (C_{b2}+C_{p2})) = 8.5 \text{ pF}. \]

\[ C_{x1} = C_{x2} = 2*C_x = 2*(C_L - C_{xb}) = 8 \text{ pF}. \]

The call to the Cap Bank API routine should be: `XTAL_16mhz_capabank_trim(850, 100, 100);`

That is, user needs to replace C78 and C79 with 8pF capacitors on the board as the following picture shows.
6.2 Software configuration

To configure the Cap Bank and easily check the results, users need to configure 32KHz Crystal Oscillator (XTAL32K) and CLKOUT function, output the trimmed clock directly to the clkout pin, and measure the result with a high-precision instrument.

The following code snippet shows how to configure the Cap Bank and route the crystal oscillator output to the CLKOUT pin:

```c
/* Code snippet */
```

Figure 8. Replacing C78 and C79 with 8pF capacitors
```c
int main(void)
{
    char ch;

    /* Init board hardware. */
    /* set BOD VBAT level to 1.65V */
    POWER_SetBodVbatLevel(kPOWER_BodVbatLevel1650mv, kPOWER_BodHystLevel150mv, false);
    /* attach main clock divide to FLEXCOMM0 (debug console) */
    CLOCK_AttachClk(BOARD_DEBUG_UART_CLK_ATTACH);

    BOARD_InitPins();
    BOARD_BootClockFreq192MHz();
    BOARD_InitDebugConsole();

    PRINTF("capbank configuration demo, please capture the clkout frequency.\r\n");

    while (1)
    {
    }
    
    IOCON->PIO[0][16] = ((IOCON->PIO[0][16] &
        /* Mask bits to zero which are setting */
        (~(IOCONPIOFUNC_MASK | IOCONPIO_MODE_MASK | IOCONPIO_DIGIMODE_MASK)))

    /* Selects pin function.
     * : PORT016 (pin 14) is configured as CLKOUT. */
    | IOCONPIO_FUNC(PIO0_16_FUNC_ALT2)

    /* Selects function mode (on-chip pull-up/pull-down resistor control).
     * : Pull-up.
     * Pull-up resistor enabled. */
    | IOCONPIO_MODE(PIO0_16_MODE_PULL_UP)

    /* Select Digital mode.
     * : Enable Digital mode.
     * Digital input is enabled. */
    | IOCONPIO_DIGIMODE(PIO0_16_DIGIMODE_DIGITAL));
```
Demo

To see the demo result, a frequency meter such as HP 5313A Universal Counter shall be used. Here assume \( C_{p1} = C_{p2} = 1 \text{pF} \). Then the call to Cap Bank API is as follows:

\[
\text{POWER\_Xtal32khzCapabankTrim}(\text{Cbp*100}, 100, 100); \quad \text{by default Cbp = 8.5pF;}
\]

Now you can configure first parameter of this routine \((\text{Cbp})\) to different values other than the default value \((8.5\text{pF})\). Then rebuild and run the code above.

You can see crystal output frequency changes in the frequency meter with different Cbp as follows:

```c
void BOARD_BootClockFROHF6M(void)
{
    ifndef SDK_SECONDARY_CORE
    /* Set up the clock sources */
    /*\*\* Ensure FRO is on */
    POWER_DisableFD(KFPERUNCFG_PD_FRO192M);
    CLOCK_SetupFROClocking(12000000U);
    CLOCK_AttachClk(KFPER12M_to_MAIN_CLK);
    /*\*\* Set up the clock sources */
    /*\*\* Set up the clock sources */
    /*\*\* Set up the clock sources */
    CLOCK_SetupClocking(86000000U);
    /*\*\* Configuring RTC OSC */
    /*\*\* Powered the XTAL 32 kHz RTC oscillator */
    POWER_DisableFD(KFPERUNCFG_PD_XTAL32K);
    POWER_EnableFD(KFPERUNCFG_PD_XTAL32K);
    /*\*\* Configuring RTC OSC */
    /*\*\* Configuring RTC OSC */
    CLOCK_AttachClk(KFPER32K_to_GSC32K);
    /*\*\* Configuring RTC OSC */
    /*\*\* Configuring RTC OSC */
    RTC->CTRL &= ~RTC_CTRL_SSRESET_MASK;
    /*\*\* Configuring RTC OSC */
    /*\*\* Configuring RTC OSC */
    POWER_SetVoltageForFreq(86000000U);
    /*\*\* Set FLASH access cycles for freq(86000000U); */
    /*\*\* Set up dividers */
    /*\*\* Set up dividers */
    /*\*\* Set up dividers */
    CLOCK_SetClkDiv(KCLK_ClkArmToClkDiv, 0U, true);  /*\*\* Set up dividers */
    /*\*\* Set up dividers */
    /*\*\* Set up dividers */
    CLOCK_SetClkDiv(KCLK_ClkArmToClkDiv, 1U, false); /*\*\* Set up dividers */
    /*\*\* Set up dividers */
    /*\*\* Set up dividers */
    CLOCK_SetClkDiv(KCLK_ClkSysToClkDiv0, 0U, true); /*\*\* Set up dividers */
    /*\*\* Set up dividers */
    /*\*\* Set up dividers */
    CLOCK_SetClkDiv(KCLK_ClkSysToClkDiv0, 1U, false); /*\*\* Set up dividers */
    /*\*\* Set up dividers */
    /*\*\* Set up dividers */
    CLOCK_SetClkDiv(KCLK_ClkSysToClkDiv1, 0U, true); /*\*\* Set up dividers */
    /*\*\* Set up dividers */
    /*\*\* Set up dividers */
    CLOCK_SetClkDiv(KCLK_ClkSysToClkDiv1, 1U, false); /*\*\* Set up dividers */
    /*\*\* Set up clock selectors – Attach clocks to the peripherals */
    CLOCK_AttachClk(KOSC32K_to_CLOUT);  /*\*\* Set up clock selectors – Attach clocks to the peripherals */
    CLOCK_AttachClk(KFRO_HF_to_MAIN_CLK); /*\*\* Set up clock selectors – Attach clocks to the peripherals */
    /*\*\* Set up clock selectors – Attach clocks to the peripherals */
    /*\*\* Set up clock selectors – Attach clocks to the peripherals */
    /*\*\* Set up clock selectors – Attach clocks to the peripherals */
    /*\*\* Set up clock selectors – Attach clocks to the peripherals */
    /*\*\* Set up clock selectors – Attach clocks to the peripherals */
    /*\*\* Set SystemCoreClock variable. */
    SystemCoreClock = BOARD_BOOTCLOCKFROHF6M\_CORE\_CLOCK;
} endif

6.3 Demo

To see the demo result, a frequency meter such as HP 5313A Universal Counter shall be used. Here assume \( C_{p1} = C_{p2} = 1 \text{pF} \). Then the call to Cap Bank API is as follows:

\[
\text{POWER\_Xtal32khzCapabankTrim}(\text{Cbp*100}, 100, 100); \quad \text{by default Cbp = 8.5pF;}
\]

Now you can configure first parameter of this routine \((\text{Cbp})\) to different values other than the default value \((8.5\text{pF})\). Then rebuild and run the code above.

You can see crystal output frequency changes in the frequency meter with different Cbp as follows.
Figure 9. Crystal output frequency (1)

Figure 10. Crystal output frequency (2)
The following table summarizes the experimental results for different Cbp with same 32KB crystal on board (Cx1=Cx2=8pF).

Table 2. Experimental results for different Cbp with same 32KB crystal

<table>
<thead>
<tr>
<th>Experiment Number</th>
<th>Code</th>
<th>Cbp  value</th>
<th>Frequency output (Hz)</th>
<th>Target (Hz)</th>
<th>Error (ppm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>POWER_Xtal32khzCapabankTrim(600, 100, 100);</td>
<td>6 pF</td>
<td>32769.773</td>
<td>32768.000</td>
<td>54.108</td>
</tr>
<tr>
<td>2</td>
<td>POWER_Xtal32khzCapabankTrim(700, 100, 100);</td>
<td>7 pF</td>
<td>32769.159</td>
<td>32768.000</td>
<td>35.370</td>
</tr>
<tr>
<td>3</td>
<td>POWER_Xtal32khzCapabankTrim(800, 100, 100);</td>
<td>8 pF</td>
<td>32768.583</td>
<td>32768.000</td>
<td>17.792</td>
</tr>
<tr>
<td>4</td>
<td>POWER_Xtal32khzCapabankTrim(850, 100, 100);</td>
<td>8.5 pF</td>
<td>32768.360</td>
<td>32768.000</td>
<td>10.986</td>
</tr>
<tr>
<td>4</td>
<td>POWER_Xtal32khzCapabankTrim(900, 100, 100);</td>
<td>9 pF</td>
<td>32768.146</td>
<td>32768.000</td>
<td>4.456</td>
</tr>
<tr>
<td>5</td>
<td>POWER_Xtal32khzCapabankTrim(1000, 100, 100);</td>
<td>10 pF</td>
<td>32767.724</td>
<td>32768.000</td>
<td>8.423</td>
</tr>
</tbody>
</table>

Based on the test result above, Cbp = 9pF can achieve the best accuracy of the oscillator output frequency toward the target frequency 32768 Hz, which is only 4.5 PPM deviation.

7 Conclusion

The original intention of the built-in Cap Bank is to allow users to reduce BOM costs and PCB area. The original intention of Cap Bank’s API function is to make it easy for users to configure the internal Cap Bank. These Cap Banks are always enabled, and their capacitance values have a certain adjustable range. In most cases, it is not exceeded. If external crystal’s IEC load capacitance (CL) exceeds this range, please correctly understand the meaning of the first parameter (Cbp) of the API and calculate it according to the calculation methods shown in the aforementioned example 2 and example 4.

When designing a PCB board, ensure that the PCB traces are symmetrical, that is, Cp1=Cp2. Use SDK version 2.8.0 or newer, which can correctly support Cap Bank configuration.
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Date of release: 16 November 2020
Document identifier: AN13057