1 Introduction

CoreMark, developed by EEMBC, is a simple and yet sophisticated benchmark. It is designed specifically to test the functionality of an embedded processor core. Running CoreMark produces a single-number score allowing users to make quick comparisons between processors.

LPC55S1x/LPC551x is an Arm® Cortex®-M33 based microcontroller for embedded applications. These devices include:

• Up to 96 KB of on-chip SRAM, up to 256 KB on-chip flash
• PRINCE module for on-the-fly flash encryption/decryption
• CASPER Crypto/FFT engine
• High-speed and full-speed USB host and device interface with crystal-less operation for full-speed
• One SDIO/MMC
• One CAN-FD
• Five general-purpose timers, one SCTimer/PWM, one RTC/alarm timer
• One 24-bit Multi-Rate Timer (MRT)
• A Windowed Watchdog Timer (WWDT)
• Nine flexible serial communication peripherals (which can be configured as a USART, SPI, high speed SPI, I²C, or I²S interface)
• Programmable Logic Unit (PLU)
• One 16-bit 1.0 Msamples/sec ADC, comparator, and temperature sensor

The Cortex-M33 offers 18.2% performance increase in the same process technology compared to the high embedded performance bars already established by Cortex-M4 processors, while improving power efficiency. Cortex-M33 official CoreMark is 4.02 CoreMark/MHz, Cortex-M4 official CoreMark is 3.40 CoreMark/MHz.

This application note describes how to port CoreMark code to LPC55S1x/LPC551x, which involves setting up software and hardware including memory partitioning, compiler setting, and board setup. It also describes how to measure CoreMark scores on the Cortex-M33 and the result including CoreMark scores and power consumption in μA/MHz. Separate CoreMark projects for different software development tools, Keil MDK, IAR EWARM and MCUXpresso IDE, are also included here for reference.

2 Integration of CoreMark library to SDK2.6 framework

The software package associated with this application note contains SDK2.6 based project framework that allows developers to drop in the CoreMark library sources and quickly get up and running with benchmarking the LPC55S1x/LPC551x. To get started, go to CoreMark. Click the download link as shown in Figure 1, and follow the instructions on that page.
2.1 Port CoreMark library into CoreMark framework

There are four variants of CoreMark projects in this application note for each IDE. Two execute the CoreMark application from internal flash and the others execute the CoreMark application from internal SRAMX.

The various CoreMark projects are:

1. coremark_score_on_flash: Executes CoreMark application from internal Flash.
2. coremark_score_on_sramx: Executes CoreMark application from internal RAM.
3. coremark_uAMHz_on_flash: Measurement current when Coremark execute on Flash.
4. coremark_uAMHz_on_sramx: Measurement current when Coremark execute on RAM.

The CoreMark projects are found in the following locations:

- Keil MDK IDE:
  
  \( \text{lpc55s1x_coremark_mdk}\)/\(\text{lpc55s1x_coremark_mdk.uvprojx}\)

- IAR Workbench IDE:
  
  \( \text{lpc55s1x_coremark_iar}\)/\(\text{lpc55s1x_coremark_iar.eww}\)

Each of executes settings have three frequency settings: 12 MHz (FRO), 96 MHz (FRO), 100MHz (PLL) and 150MHz (PLL).

Depending on the toolchain, the workspace are as shown in following figures. The CoreMark framework requires the addition of the CoreMark files from EEMBC.

2.1.1 Coremark framework for Keil MDK/IAR EWARM/MCUxpresso IDE

The \( \text{lpc55s1x_coremark_xxx} \) project must be set as active before the CoreMark source code files can be added.
Figure 2. Keil MDK CoreMark project configuration select

Figure 3. IAR EWARM workspace
Copy the following files from the CoreMark package downloaded from EEMBC.

- core_list_join.c
- core_main.c
- core_matrix.c
- core_state.c
- core_util.c
- coremark.h
For Keil MDK, place these files in the project directory of `lpc55s1x_coremark_mdk\source`.

For IAR Embedded Workbench, place these files in the project directory of `lpc55s1x_coremark_iar\source`.

For MCUXpresso, place these files in the project directory of `lpc55s1x_coremark_mcux\source`.

The files, `ee_printf.c`, `core_portme.c`, and `core_portme.h` (under the `port_lpc5500` folder, need to be copied to the following folder locations.

- For Keil IDE:
  - Place the files in the `lpc55s1x_coremark_mdk\source\port_lpc5500`.
  - Add the files into the Keil MDK project framework to the respective groups source by double clicking on the groups.

- For IAR Embedded workbench:
  - Place the files in the `lpc55s1x_coremark_iar\source\port_lpc5500`.
  - Add the files into the IAR project framework to the respective groups source by double clicking on the groups.

- For MCUXpresso:
  - Place the files in the `lpc55s1x_coremark_mcux\source\port_lpc5500`.
  - Add the files into the MCUXpresso project framework to the respective groups source by click the Refresh selection.
• For KEIL MDK project:
  — Right-click the source folder and select **Add** and then **Add Files**…

• For IAR Embedded workbench:
  — Right-click the source folder and select **Add** and then **Add Files**…
• For MCUXpresso project:
  — Copy the files into the source folder and then click the Refresh. The files will be added in project automatically.

Use the core_portme.c and core_portme.h files provided with the application note and not the one from the EEMBC CoreMark package. For convenience these files have the required porting changes ready for use.

Copy these files to the source folder for all three tool chains and add the core_portme.c file in the project framework under the source group.

A few files need to be modified to support CoreMark and are described below.

In the project scatter file change the stack size as 0x1000.

```
define symbol __size_cstack__         = 0x1000;
define symbol __size_heap__          = 0x1000;
```

To add the path to the header files used in the project:

• In Keil MDK, under Project -> Options -> C/C++(AC6), click Include path and add the following paths that contain the header files.
In IAR, under Project -> Options -> C/C++ Compiler, click Preprocessor and add the following paths that contains the header files.
In MCUXpresso, under Properties for xxxx -> C/C++ Build -> Settings, click Includes and add the following paths that contains the header files.

- `$PROJ_DIR$/source/port_lpc5500`
Now, the CoreMark files have been successfully ported into the CoreMark project framework.

2.1.2 CoreMark framework to execute from Internal SRAM

The project, `lpc55s1x_coremark_xxx_on_sramx`, executes the CoreMark application from 16 KB SRAMX memory region.

The files, `core_list_join.c`, `core_main.c`, `core_matrix.c`, `core_state.c`, and `core_util.c`, are relocated to execute from SRAMX using the linker scripts.

For Keil MDK, the linker script is located at:

```
.lpc55s1x_coremark_mdk\LPC55S16_coremark_score_sramx.scf
```

Figure 12 shows the linker script settings for `lpc55s1x_coremark_xxx_on_sramx` project.
For IAR EWARM IDE to execute CoreMark in Internal SRAM, to place Coremark operation codes into RAM section, add the following line of code in the icf file, as shown in Figure 13.
For MCUXpresso to execute CoreMark in Internal SRAM, select the linker file as `LPC55S16_coremark_score_sramx.ld` in Managed Linker script, as shown in Figure 14.
2.2 Optimizing the CoreMark framework

There are many factors that affect the CoreMark and µA/MHz score that can be optimized. Some of these factors are IDE-dependent optimizations, while others leverage the MCU architecture for better performance. The goal is to produce the best scores from all three IDEs. It is important to understand that these IDEs are constantly changing and a different version of a given IDE may add or remove features that may make these optimizations obsolete or ineffective.

The followings are the IDE versions that are applicable to this application note:

- Keil MDK v5.28
- IAR EWARM 8.40.2
- MCUXpresso 11.1.0 Build[3209]

2.2.1 Memory considerations

Due to the inherent architecture of SRAM and flash, CoreMark executes faster when running out of SRAM. The LPC55S1x/LPC551x internal memory uses a multilayer AHB matrix system that provides a separate instruction and data bus for Cortex-M33 and SRAMx bank. As shown in Figure 15, SRAM0 to SRAM2 are on System bus. Placing the CoreMark code and data in different SRAM banks minimizes bus contention and improves instruction and data parallelism.

It is important to minimize the flash wait state according to the MCU frequency to optimize the CoreMark score. In contrast, when performing the µA/MHz test, it is possible to save power by disabling the flash’s prefetch ability. For more information about how to correctly configure the flash memory, such as the minimum amount of wait states allowed at a given core frequency, see LPC55S1x/LPC551x User Manual (document UM11295).
The provided CoreMark framework projects include separate SRAM and flash based projects that implement various memory optimizations.

In both the SRAM and flash projects, there is a `COREMARK_SCORE_TEST` macro defined in `core_portme.h`. It indicates whether the project is configured to execute the CoreMark benchmark or the μA/MHz test.

- If this macro is defined, the CoreMark score test will run.
- If this macro is commented out, μA/MHz test will run.

Use this macro to switch between the two benchmarks cases.

### 2.2.2 IDE optimization setting

The following optimizations are compiler-based and therefore IDE dependent. These optimizations apply to both the SRAM and flash based projects.

#### 2.2.2.1 Keil optimizations

There are two compiler optimizations that can be done to improve the CoreMark score. In the Options of each Coremark source code files, on the C/C++(AC6) tab, the optimization level needs to be set as `-mcpu=Cortex-m33 -target=arm-arm-none-eabi -Omax -g -mthumb -mfpu=fpv5-sp-d16 -mfloat-abi=hard -fno-common -ffp-mode=fast` in Include Paths Misc Controls.
When benchmarking the power consumption of the MCU, the optimization setting must be set to Level 0 (-O0) and **Optimized for time** must be unchecked.

Two compiler optimizations can be done to improve CoreMark score. Set the optimization level to **High**, select **Speed** from the drop-down menu, and check the **No size constraints**.
Figure 18. IAR EWARM CoreMark score optimization

When benchmarking the power consumption of the MCU, set the optimization level to None.
2.2.2.3 MCUXpresso Optimization

There are two compiler optimizations that can be done to improve CoreMark score. To set the optimization level to -O3, select Optimize most(-O3) from the drop-down menu.
When benchmarking the power consumption of the MCU, set the optimization level to **None(-O0)**.
3 Measuring CoreMark on board

3.1 LPC55S69Xpresso board

The LPC55S69Xpresso board supports a VCOM serial port connection via J1. To observe debug messages from the board set the terminal program to the appropriate COM port and use the setting **115200-8-N-1-none**. To make the debug messages easier to read, set the new line receive setting to **Auto**.

3.2 Board setup

The LPC55S16-EVK Rev A1 development board is used for benchmarking.
3.2.1 μA/MHz measurement setup

To measure the LPC55S1x/LPC551x power consumption, connect ammeter across JP22, as shown in Figure 23.

NOTE

The current data on EVK maybe little higher than datasheet, due to the EVK have more other components may cost more power.
Users can measurement the current through JP22 with a multimeter.

When performing the μA/MHz benchmark, use J2 USB connector to provide power to the board. Additionally, after the μA/MHz benchmark project has been downloaded, power cycling the board by removing the USB cable and reinserting. It is recommended to make sure the debug probe be not connected.

The core clock frequency can be changed by selecting different configurations through the shell terminal by MCU uart0.

### 3.3 Run CoreMark code

To get CoreMark result:

1. Connect the board's connector J1 with PC,
2. PC recognizes the LPC-Link2 debugger with a Simulate Serial Port, as shown in Figure 24.

   If PC cannot find the serial port driver, please download the LPCScrypt and install on your PC.
3. Open a UART debug terminal, such as, Tera Term, putty, etc, and configure as 115200, 8 data bits, no parity, 1 stop bit, as shown in Figure 25.
4. Once the CoreMark necessary file is added into the project, by following instructions in Port CoreMark library into CoreMark framework, compile the project and download to the LPC55S16-EVK board.

5. Click the Reset button, as shown in Figure 26, and the prompt information is displayed on the terminal. Users can input 1, 2, 3, or 4 from PC keyboard to select the Core frequency like 12 MHz, 96 MHz, 100 MHz (PLL), and 150 MHz (PLL). Once a character is input, the Coremark test program starts immediately and then waits for ten seconds or more. The CeMark benchmark prints on the terminal after a few seconds, as shown in Figure 27.
4 Result

Figure 27 shows the CoreMark benchmark result when running LPC55S1x/LPC551x at 150 MHz core frequency in IAR. The CoreMark benchmark score is the number of iterations per second. The CoreMark/MHz score executing from internal flash for this run is $603.298029/150 \text{ MHz} = 4.021 \text{ CoreMark/MHz}$. 
Table 1 describes typical CoreMark score when benchmarked on Keil MDK, IAR EWARM and MCUXpresso IDE when running from internal flash and SRAM at 12 MHz core frequency.

<table>
<thead>
<tr>
<th>IDE</th>
<th>CoreMark/MHz score (SRAMX)</th>
<th>CoreMark/MHz score (Flash)</th>
</tr>
</thead>
<tbody>
<tr>
<td>KEIL MDK</td>
<td>4.012</td>
<td>3.760</td>
</tr>
<tr>
<td>IAR EWARM</td>
<td>3.872</td>
<td>3.668</td>
</tr>
<tr>
<td>MCUXpresso</td>
<td>2.824</td>
<td>2.715</td>
</tr>
</tbody>
</table>

LPC55S1x/LPC551x CoreMark Porting Guide, Rev. 0, November, 2020
Table 2 describes typical CoreMark score when benchmarked on Keil MDK, IAR EWARM and MCUXpresso IDE when running from internal flash and SRAM at 96 MHz core frequency.

### Table 2. LPC55S16-EVK board CoreMark/MHz score when 96 MHz

<table>
<thead>
<tr>
<th>IDE</th>
<th>CoreMark/MHz score (SRAMX)</th>
<th>CoreMark/MHz score (Flash)</th>
</tr>
</thead>
<tbody>
<tr>
<td>KEIL MDK</td>
<td>4.021</td>
<td>2.514</td>
</tr>
<tr>
<td>IAR EWARM</td>
<td>3.879</td>
<td>2.668</td>
</tr>
<tr>
<td>MCUXpresso</td>
<td>2.830</td>
<td>2.120</td>
</tr>
</tbody>
</table>

Table 3 describes typical CoreMark score when benchmarked on Keil MDK, IAR EWARM and MCUXpresso IDE when running from internal flash and SRAM at 100 MHz core frequency.

### Table 3. LPC55S16-EVK board CoreMark/MHz score when 100 MHz

<table>
<thead>
<tr>
<th>IDE</th>
<th>CoreMark/MHz score (SRAMX)</th>
<th>CoreMark/MHz score (Flash)</th>
</tr>
</thead>
<tbody>
<tr>
<td>KEIL MDK</td>
<td>4.021</td>
<td>2.514</td>
</tr>
<tr>
<td>IAR EWARM</td>
<td>3.879</td>
<td>2.668</td>
</tr>
<tr>
<td>MCUXpresso</td>
<td>2.830</td>
<td>2.120</td>
</tr>
</tbody>
</table>

Table 4 describes typical CoreMark score when benchmarked on Keil MDK, IAR EWARM and MCUXpresso IDE when running from internal flash and SRAM at 150 MHz core frequency.

### Table 4. LPC55S16-EVK board CoreMark/MHz score when 150 MHz

<table>
<thead>
<tr>
<th>IDE</th>
<th>CoreMark/MHz score (SRAMX)</th>
<th>CoreMark/MHz score (Flash)</th>
</tr>
</thead>
<tbody>
<tr>
<td>KEIL MDK</td>
<td>4.021</td>
<td>1.910</td>
</tr>
<tr>
<td>IAR EWARM</td>
<td>3.880</td>
<td>2.129</td>
</tr>
<tr>
<td>MCUXpresso</td>
<td>2.830</td>
<td>1.733</td>
</tr>
</tbody>
</table>

The current data on EVK may be a little higher or lower than what are described in datasheet, as the EVK contains more components and cost more power.

The average current in 100&150 MHz will be higher than other modes, because the two modes enable PLL and the PLL costs more power.

### Table 5. Keil MDK μA/MHz score

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Avg. power consumption (mA, SRAM X)</th>
<th>μA/MHz score (SRAM X)</th>
<th>Avg. power consumption (mA, Flash)</th>
<th>μA/MHz score (Flash)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 MHz</td>
<td>1.01</td>
<td>84.20</td>
<td>1.12</td>
<td>100.00</td>
</tr>
<tr>
<td>96 MHz</td>
<td>2.95</td>
<td>30.72</td>
<td>3.22</td>
<td>33.55</td>
</tr>
</tbody>
</table>

Table continues on the next page...
Table 5. Keil MDK μA/MHz score (continued)

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Avg. power consumption (mA, SRAM X)</th>
<th>μA/MHz score (SRAM X)</th>
<th>Avg. power consumption (mA, Flash)</th>
<th>μA/MHz score (Flash)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100 MHz</td>
<td>3.31</td>
<td>33.10</td>
<td>3.58</td>
<td>35.80</td>
</tr>
<tr>
<td>150 MHz</td>
<td>5.07</td>
<td>33.80</td>
<td>4.90</td>
<td>32.67</td>
</tr>
</tbody>
</table>

Table 6. IAR EWARM μA/MHz score

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Avg. power consumption (mA, SRAM X)</th>
<th>μA/MHz score (SRAM X)</th>
<th>Avg. power consumption (mA, Flash)</th>
<th>μA/MHz score (Flash)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 MHz</td>
<td>0.94</td>
<td>78.50</td>
<td>1.09</td>
<td>91.00</td>
</tr>
<tr>
<td>96 MHz</td>
<td>2.71</td>
<td>28.30</td>
<td>2.93</td>
<td>31.00</td>
</tr>
<tr>
<td>100 MHz</td>
<td>3.06</td>
<td>30.60</td>
<td>3.32</td>
<td>33.20</td>
</tr>
<tr>
<td>150 MHz</td>
<td>4.70</td>
<td>31.50</td>
<td>4.60</td>
<td>31.00</td>
</tr>
</tbody>
</table>

Table 7. MCUXpresso μA/MHz score

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Avg. power consumption (mA, SRAM X)</th>
<th>μA/MHz score (SRAM X)</th>
<th>Avg. power consumption (mA, Flash)</th>
<th>μA/MHz score (Flash)</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 MHz</td>
<td>0.97</td>
<td>80.90</td>
<td>1.12</td>
<td>93.33</td>
</tr>
<tr>
<td>48 MHz</td>
<td>2.85</td>
<td>29.70</td>
<td>3.20</td>
<td>33.40</td>
</tr>
<tr>
<td>96 MHz</td>
<td>3.20</td>
<td>32.00</td>
<td>3.60</td>
<td>36.00</td>
</tr>
<tr>
<td>150 MHz</td>
<td>4.90</td>
<td>32.67</td>
<td>4.90</td>
<td>32.67</td>
</tr>
</tbody>
</table>

5 Conclusion

This application note describes three types of CoreMark benchmarking on the LPC55S1x/LPC551x with different IDEs (Keil, IAR, MCUXpresso): the CoreMark score, power consumption, and the μA/MHz. It also describes how to optimize the benchmark results when running the benchmark out of internal SRAM and flash.

The CoreMark results are measured on LPC55S16-EVK. The best CoreMark number is 4.021, achieved by using KEIL MDK (Arm Compiler 6.12) and running CoreMark from SRAM X. The best CoreMark power consumption in μA/MHz is 28.30, achieved by running CoreMark from SRAM when core frequency is 96 MHz.

6 Reference

1. CoreMark Benchmarking for ARM Cortex Processors
2. LPC5411x CoreMark Cortex-M4 Porting Guide (document AN11181)
3. LPC55S1x User Manual (document UM11295)
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