AN13158

NVT4858/NVT4557 voltage-level translator layout guideline

Rev. 1.0 — 1 July 2021 Application note

Document information

Information	Content
Keywords	NVT4858, NVT4557, Level Shifter, Level Translator, SD card, SIM card, Layout Guideline
Abstract	The NVT4858 is an SD 3.0 compliant dual voltage level translator with auto-direction control. The NVT4557 is a SIM SIO-7816 Smart Card compliant dual voltage level translator with auto-direction control. This application note details the layout guidelines to ensure the optimal operation of the device.

Revision history

Rev	Date	Description
v.1	20210701	Initial version

1 Introduction

High performance digital signals on modern microprocessors are designed using advanced CMOS process to take advantage of its low power consumption. However, CMOS logic has very fast edge rates in the range of 1 ns to 2 ns. PCB traces might exhibit ringing, signal degradation and reflection due to the effect of the signal's fast rise and fall time contributed by the PCB transmission characteristic.

This application note details the general PCB layout guidelines for High Speed Secure Digital (SD), and Smart Card (SIM) in NVT4858 and NVT4557 voltage level shifter application to minimize signal integrity issues.

2 NVT4858/NVT4557 voltage-level translator layout guidelines

To ensure optimal performance and reliability of the device, the following PCB layout guidelines are recommended.

2.1 Power and ground

- A minimum four-layer PCB stack-up is required.
- The level shifter and the card socket should be placed top of a solid, continuous ground plane.
- Preferably, the power for the level shifter should come directly from the power plane underneath it, but if the power trace must be used then the trace should be at least 20 mil wide.
- Bypass capacitors of 0.1 µF should be placed as close as possible to VCCA and VCCB pins with a very short PCB trace.

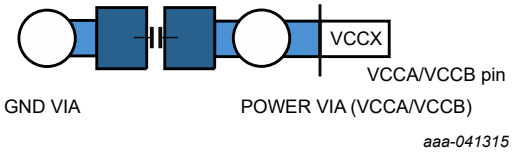

Figure 1. Bypass capacitor placement

2.2 SD and SIM signals from host to level shifter

The SD interface high speed signals SD_DAT[3:0], SD_CDM and SD_CLK are critical and require careful layout and consideration. These signals must be routed above a solid ground plane and should be routed with the following recommendations.

- Component Placement and Trace Impedance – high frequency signals are sensitive to impedance changes and discontinuity introduced by vias. The level shifter and the card socket should be placed on the same layer as the Hot Controller. Placing these devices on the same layer helps to reduce the need to use vias with direct routing between these devices. The PCB traces should be routed with 50 Ω characteristic impedance or close to it to reduce transmission effect. The round-trip delay of the PCB traces should be less than the rise/fall times of the signal driver. If the PCB traces are longer than the rise/fall times, then series termination resistors can be used to minimize signal reflection.
- Series Termination and Placement – if series termination resistors are to be used, the suggested values are 22 Ω to 33 Ω. The termination resistors on the Host Controller

side of the level shifter should be placed close to the level shifter. The termination resistors on the card side of the level shifter should be placed close to the card socket.

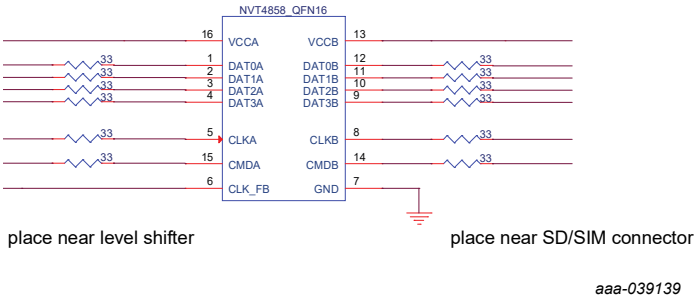

Figure 2. Termination resistors

- PCB trace separation – SD clock and data signals carry high frequency fast rise and fall time signals. Any low capacitive impedance path existed between two traces creates a path for one signal to couple onto another signal next to it. For this reason, SD clock and data must be separate from one another with the following spacing constraint.
  SD_CLK > 2 times the high of SD_CLK to the ground plane underneath it.
  SD_DATA[3:0] > 1.5 times the high of SD_CLK to the ground plane underneath it.
  SD_CMD > 1.5 times the high of SD_CLK to the ground plane underneath it.
- Trace Routing – when routing the PCB traces, it is critical to keep the trace width the same to keep the trace impedance constant from the driver to the receiver. Any trace width deviation creates impedance mismatch and creates signal reflection. Avoid using 90-degree angle and use a 45-degree bend when the trace must be routed perpendicularly.
- PCB Trace length matching - to minimize the skew between traces, route them with the same length.

2.3 SD and SIM signals from level shifter to card socket

The SD interface high speed signals SD_DAT[3:0], SD_CDM and SD_CLK are critical and require careful layout and consideration. These signals must be routed above a solid ground plane and should be routed with the following recommendations.

- Component Placement and Trace Impedance – component placement and trace impedance should follow the guideline as PCB routing from Host Controller to Level Shifter.
- Series Termination and Placement – if series termination resistors are to be used, the suggested values are 22 Ω to 33 Ω. The termination resistors on the card side of the level shifter should be placed close to the card socket as shown in Figure 2.
- PCB trace separation – the trace separation impedance should follow the guideline as PCB routing from Host Controller to Level Shifter.
- Trace Routing – when routing the PCB traces, it is critical to keep the trace width the same to keep the trace impedance constant from the driver to the receiver. Any trace width deviation creates impedance mismatch and creates signal reflection. Avoid using 90-degree angle and use 45-degree bend when the trace must be routed perpendicularly.

- The total capacitance between the level shifter and the card should follow the recommendation in the SD Physical Layer specification[1].

Table 1. I/O driver design target

Drive type	Symbol	Driver rise/fall time requirements				Condition
		Min	Typ	Max	Units	C_L
Type B for UHS104	T_RB, T_FB	0.40	0.88	1.32	ns	15 pF
Type B for UHS50	T_RB, T_FB	0.70	1.83	2.75	ns	30 pF

- PCB Trace length matching - to minimize the skew between traces, route them with the same length.

3 Conclusion

Proper PCB layout is critical for the successful operation of NT4858/NVT4557. All high-speed PCB rules, techniques, component placement and trace routing must be followed and taken into consideration during the PCB layout phase.

4 References

[1] SD Specifications, Part 1, Physical Layer Specification; version 3.01; February 18, 2010

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Date of release: 1 July 2021
Document identifier: AN13158