

# AN13168

## Migration Guide from LPC546xx to LPC54(S)0xx and LPC54(S)0xxJxM

AN13168

Rev. 0 — 03/21

Application Note

### 1 Introduction

This document describes how to migrate from LPC546xx to LPC540xx and LPC540xxJxM, and focuses on addressing the changes in functionality between these two series of LPC MCUs.

For simplicity reasons, this document refers to LPC540xx/LPC54S0xx and LPC540xxJxM/LPC54S0xxJxM as *LPC54(S)0xx* and *LPC54(S)0xxJxM* respectively.

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#### NOTE

LPC54(S)0xx and LPC54(S)0xxJxM are basically the same, the only difference is that LPC54(S)0xx does not have internal flash, while LPC54(S)0xxJxM has on-chip Quad SPI flash (connected on SPIFI interface internally).

### 2 Flash, RAM, and EEPROM

The LPC546xx family of MCUs include up to 512 KB of flash, up to 200 KB of on-chip SRAM, and up to 16 kB of EEPROM memory.

The LPC540xx/LPC54S0xx family includes 360 KB of on-chip SRAM and it supports Quad SPI Flash XIP. However, it does not have internal flash.

LPC54018JxM / LPC54S018JxM family includes up to 4 MB of on-chip Quad SPI Serial Flash (connected on SPIFI interface), 360 KB of on-chip SRAM.

Table 1. Memory comparison

	LPC546xx	LPC540xx / LPC54S0xx	LPC54018JxM / LPC54S018JxM
Flash	up to 512 KB	None	up to 4 MB of on-chip Quad SPI Serial Flash
SRAM	up to 200 KB	360 KB	360 KB
EEPROM	up to 16 KB	None	None

#### NOTE

Memory mapping between LPC546xx and LPC540xx/LPC540xxJxM is different. Please refer to the corresponding User Manual for details.

### 3 Package and pinout considerations

LPC546xx and LPC54(S)0xx have the below four packages:

- 100-pin, TFBGA
- 180-pin, TFBGA
- 208-pin, LQFP



- 100-pin, LQFP

LPC54(S)0xxJxM only has the 180-pin, TFBGA package.

**Table 2. Package comparison**

Package	LPC546xx	LPC54(S)0xx	LPC54(S)0xxJxM
100-pin, TFBGA	✓	✓	×
180-pin, TFBGA	✓	✓	✓
208-pin, LQFP	✓	✓	×
100-pin, LQFP	✓	✓	×

**NOTE**

LPC546xx and LPC54(S)0xx are pin to pin compatible. **However, LPC54(S)0xxJxM is not compatible with them.** It is because some pins of LPC540xxJxM/LPC54S0xxJxM are connected with internal on-chip QSPI flash.

The table below lists the main differences between LPC54(S)0xxJxMET180 and LPC546xx,LPC54(S)0xx. For the hardware design, please refer to [LPC54S018M-EVK](#).

**Table 3. Pinout comparison**

Symbol	LPC54(S)0xxJxMET180
N7(P0_23)	Must be connected to C4(P4_16).
C4(P4_16)	Must be connected to N7(P0_23).
A4(P4_15)	VDD, single 2.7 V to 3.6 V power supply powers internal digital functions and I/Os.
K8(PIO0_25)	Not Connected pins — These pins must be left unconnected (floating).
L9(PIO0_27)	Not Connected pins — These pins must be left unconnected (floating).
M7(PIO0_24)	Not Connected pins — These pins must be left unconnected (floating).
M9(PIO0_28)	Not Connected pins — These pins must be left unconnected (floating).
M13(PIO0_26)	Not Connected pins — These pins must be left unconnected (floating).

## 4 Peripherals and frequency

LPC546xx and LPC540xx/LPC540xxJxM have basically the same peripherals. LPC546xx has up to 10 Flexcomm interfaces, whereas LPC540xx/LPC540xxJxM has up to 11 Flexcomm interfaces (Flexcomm 10 is dedicated for SPI).

LPC546xx can run at a frequency of up to 220 MHz, whereas LPC54(S)0xx/LPC54(S)0xxJxM can run at a frequency of up to 180 MHz.

## 5 Image protection and security

LPC546xx supports ECRP (Enhanced Code Read Protection). However, LPC54(S)0xx and LPC54(S)0xxJxM do not support this feature.

The LPC54S0xx/LPC54S0xxJxM supports CRC integrity verification and secure boot.

**Table 4. image protection and secure boot comparison**

	LPC546xx	LPC540xx / LPC540xxJvM	LPC54S0xx / LPC54S0xxJxM
<b>ECRP</b>	√	×	×
<b>CRC image integrity verification</b>	√	√	√
<b>Secure boot</b>	×	×	√

LPC54S0xx and LPC54S0xxJxM have security enhanced features AES and Physically Unclonable Functions (PUF).

The PUF controller provides secure key storage without storing the key. This is done by using the digital fingerprint of a device derived from SRAM. Instead of storing the key, a Key Code is generated, which, in combination with the digital fingerprint, is used to reconstruct keys that are routed to the AES engine or for use by software. The PUF controller provides generation and secure storage for keys.

AES can use the key from One-Time Programmable (OTP) or PUF. OTP can store a scrambled key, and PUF index 0 key is routed to on-chip AES engine (AES KEY registers are loaded with the reconstructed PUF key) through inaccessible internal bus, protecting or hiding the plain key to runtime software.

**Table 5. Security feature comparison**

	LPC546xx	LPC540xx/LPC540xxJvM	LPC54S0xx/LPC54S0xxJxM
<b>Secure Hash Algorithm (SHA1/SHA2)</b>	√	√	√
<b>AES</b>	×	×	√
<b>PUF</b>	×	×	√

## 6 Conclusion

LPC54(S)0xx/LPC54(S)0xxJxM has more security features than LPC546xx, it also has some improvements in USB. **Therefore, it is strongly recommended to use LPC54(S)0xx/LPC54(S)0xxJxM on new Security/USB products.**

If LPC546xx executes code in internal flash, LPC54(S)0xx executes code in Quad SPI flash. Hence, LPC546xx has better performance than LPC54(S)0xx. **Therefore, for LPC54(S)0xx, it is recommended to put the code with high performance requirements in SRAM.**

Also, as described in the above chapters, it is easy to migrate from LPC546xx to LPC54(S)0xx/LPC54(S)0xxJxM.

## 7 Revision history

The table below summarizes revisions to this document.

**Table 6. Revision history**

Date	Revision	Topic-reference	Change
17/03/2021	0	-	Initial release

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