AN13203

Application and Soldering Information for PCF2131 and PCA2131 RTCs

Rev. 1.1 — 7 November 2025 Application note

Document information

Information	Content
Keywords	AN13203, PCA2131, PCF2131, application, soldering
Abstract	This application note gives additional information about application and soldering of the PCA2131 and PCF2131 Real-Time Clocks (RTCs).

1 Introduction

This application note provides application and soldering information on the PCF2131 and PCA2131 Real-Time Clocks (RTCs).

2 Reflow soldering

This section provides soldering details for the PCF2131 and PCA2131 RTC devices.

2.1 Introduction to reflow soldering

Soldering is one of the most common methods through which packages are attached to Printed-Circuit Boards (PCBs) to form electrical circuits. The soldered joint provides the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one PCB. However, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

The PCF2131 and PCA2131 are intended for use in a reflow soldering process.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in reflow soldering are:

- Board specifications, including the board finish, solder masks, and vias.
- Package footprints, including solder thieves and orientation.
- The moisture sensitivity level of the packages.
- Package placement
- Inspection and repair
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures than a SnPb process, therefore reducing the process window.
- Solder pastes printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board.
- Reflow temperature profile (see Figure 1; this profile includes preheat (T_s), reflow (in which the board is heated to the peak temperature (T_p)) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged.

For further information on reflow soldering IC, refer to ref.[1].

2.2 Reflow soldering of PCF2131 and PCA2131

The PCF2131 and PCA2131 is intended for use in a lead-free reflow soldering process, classified in accordance with ref.[3].

Figure 1 shows the reflow soldering temperature profile according to ref.[3], used for the qualification of the PCF2131 and PCA2131.

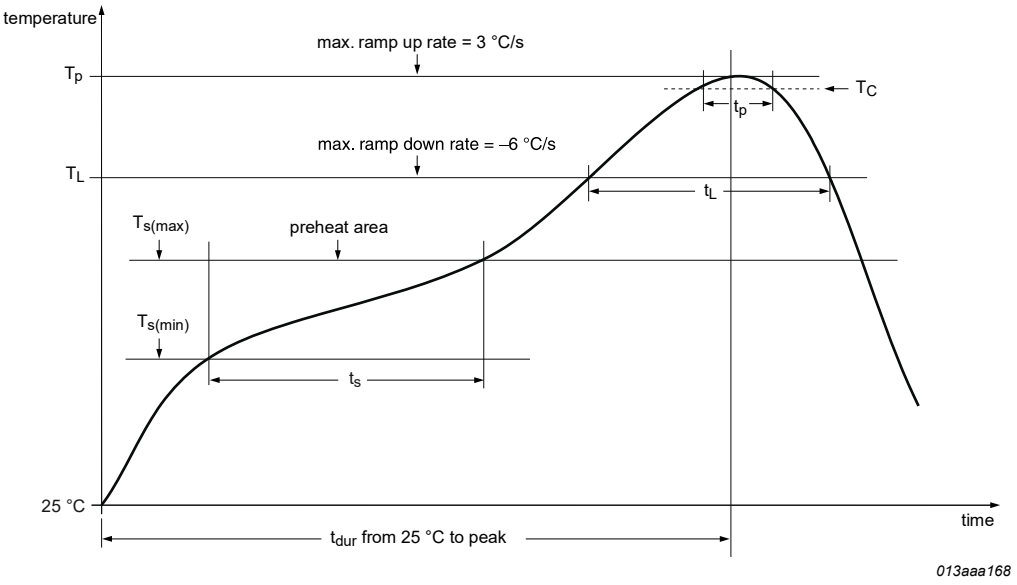

Figure 1. Reflow temperature profile

The reflow profile in this document is for classification/preconditioning and not meant to specify board assembly profiles. Actual board assembly profiles should be developed based on specific process needs and board designs, but must not exceed the parameters shown in Table 1. All temperatures refer to the center of the package, measured on the package body surface that is facing up during the reflow soldering process.

Table 1. Values of reflow temperature profile

Symbol	Value	Unit
T_p	260	°C
T_L	217	°C
T_C	255	°C
$T_{s(max)}$	200	°C
$T_{s(min)}$	150	°C
t_p	30	s
t_L	60 to 150	s
t_s	60 to 120	s
t_{dur}	max 480	s

Recommendations:

1. The reflow soldering profile shown in Figure 1 is recommended. A full convection reflow system, capable of maintaining the reflow profile of Figure 1, is recommended.
2. The peak temperature (T_p) of the reflow soldering process must not exceed 260 °C. If the temperature exceeds 260 °C, the characteristics of the crystal oscillator are degraded or the device can even be damaged.
3. The time, while the PCF2131 and PCA2131 is heated above T_C = 255 °C, must not exceed 30 s (t_p), otherwise the characteristics of the crystal oscillator is degraded or the device can even be damaged.

2.3 Effect of reflow soldering on the frequency characteristics

The reflow soldering process typically generates a negative frequency shift.

After one-time reflow soldering, processed in accordance with the recommended temperature profile shown in Figure 1 and Table 1, a frequency shift of -2 ppm is typical. Any other reflow temperature profile or multiple soldering can cause a different frequency shift after soldering. The frequency shift after soldering can be reduced by lowering the peak temperature T_p and shortening the time t_p of the soldering process (see Figure 1 and Table 1).

2.4 Frequency correction after reflow soldering

Depending on the actual soldering profile used, a frequency offset of some ppm can vary from case to case. To compensate for this shift in frequency due to reflow soldering, a frequency offset can be programmed through bits AO[3:0] of register address 0x30h.

A frequency measurement (see section 7.3.1 of ref.[2]) must be performed after the final assembly of the board if:

- the soldering was processed multiple times, or
- the soldering was not made according to the recommended temperature profile, or
- the best result in accuracy should be achieved.

Then the offset with the appropriate value given in Table 2 must be programmed into AO[3:0]. Deviations caused by assembly steps or due to production tolerances can be compensated with it.

Table 2. Typical frequency correction at 25 °C

AO[3:0]		
Decimal	**Binary**	**ppm**
0	0000	+16
1	0001	+14
2	0010	+12
3	0011	+10
4	0100	+8
5	0101	+6
6	0110	+4
7	0111	+2
8	1000	0
9	1001	-2
10	1010	-4
11	1011	-6
12	1100	-8
13	1101	-10
14	1110	-12
15	1111	-14

3 Application information

This section provides soldering details for the PCF2131 and PCA2131 RTC devices.

3.1 Assembly recommendations

- Take precautions when using the PCA2131 and PCF2131 with general-purpose mounting equipment to avoid excessive shocks that could damage the integrated quartz crystal.
- Avoid ultrasonic cleaning that could damage the integrated quartz crystal.

3.2 General application information

- The IFS pin must be connected to ground (VSS) to select the SPI-bus.
- The IFS pin must be connected to the VDD pin to select the Inter-Integrated Circuit (I^2C) bus.
- The center thermal pad must be left floating.
- Avoid in the board layout running signal traces under the package unless a ground plane is placed between the package and the signal line.
- A backup battery can be attached to the VBAT pin to enable the battery switch-over when the main power VDD fails. If VBAT is not used, it has to be connected to the ground. If VBAT is used, one of the supplies (VBAT or VDD) has to be turned on before the other.
- The battery-backed voltage VBBS can be used to supply an external RAM to retain RAM data in battery backup mode. A low leakage decoupling capacitor should be connected from BBS to VSS: suggested value is 1 nF, max 100 nF. If BBS is not used to supply an external IC, the decoupling capacitor between the BBS and VSS pins must always be connected.
- INTA and INTB are open-drain, active LOW outputs, which require external pullup resistors: The maximum pullup voltage should be limited to the same voltage as VDD.

3.3 Battery switch-over applications

The functionality of the battery switch-over is limited by the fact that the power supply V_{DD} is monitored in every 1 ms to save power consumption. Considering that the battery switch-over threshold value ($V_{th(sw)bat}$) is typically 2.5 V, the power management operating limit ($V_{DD(min)}$) is 1.8 V, and that V_{DD} is monitored in every 1 ms, the battery switch-over works properly in all cases where V_{DD} falls with a rate lower than 0.7 V/ms, as shown in Figure 2.

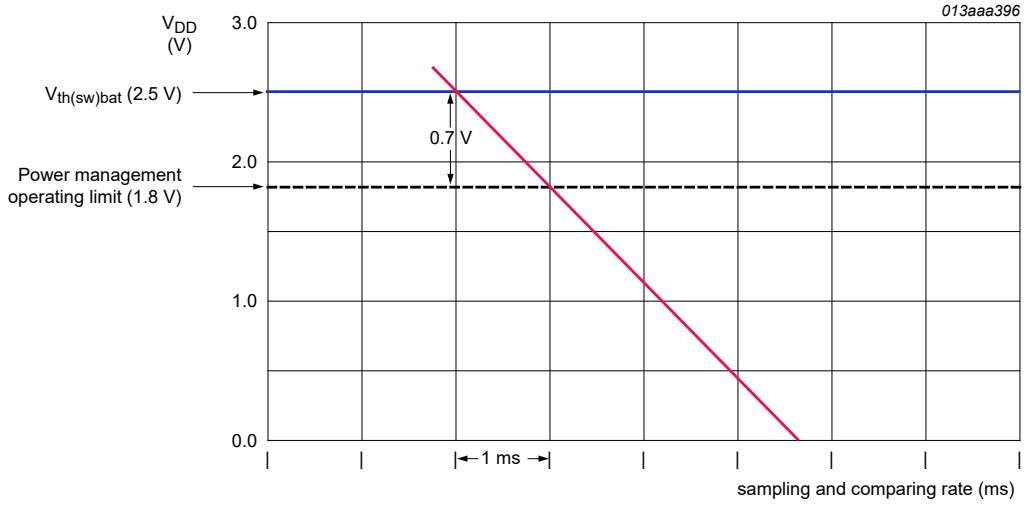

Figure 2. Supply voltage with respect to sampling and comparing rate

In an application where during power-down the current consumption on pin VDD is:

- in the range of a few µA a capacitor of 100 nF on pin VDD is enough to allow a slow power-down and the proper functionality of the battery switch-over;
- in the range of a few hundreds of µA, the value of the capacitor on pin VDD must be increased to force a falling gradient of less than 0.7 V/ms on pin VDD to assure the proper functionality of the battery switch-over;
- higher than some mA it is recommended to add an RC network on the VDD pin, as shown in Figure 3.

A series resistor of 330 Ω and a capacitor of 47 µF assure the proper functionality of the battery switch-over even with fast VDD slope.

Note that:

- It is not suggested to assemble a series resistor higher than 1 kΩ because it would cause a large voltage drop at the VDD pin.
- Lower values of capacitors are possible, depending on the VDD slope at the power supply source in the application.

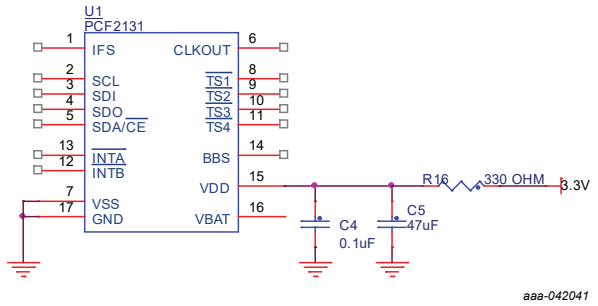

Figure 3. RC network on pin VDD

4 References

This section lists the references used to supplement this document.

[1] NXP Semiconductors, *Surface mount reflow soldering description*, AN10365

[2] NXP Semiconductors, *Highly accurate nano-power RTC with integrated quartz crystal*, PCF2131 datasheet, May 2021

[3] IPC/JEDEC J-STD-020, *Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices*

5 Revision history

This section summarizes revisions to this document.

Table 3. Revision history

Document ID	Release date	Description
AN13203 v.1.1	07 November 2025	Updated as per CIN# 202411003I: • Updated the Section 3.2: changed from *"center pad must be connected to ground (VSS)"* to *"central pad must be left floating"*. • Minor editorial changes
AN13203 v.1.0	26 May 2021	• Initial version

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