**NXP Semiconductors**
Application Notes

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# S32G2 Vehicle Network Processor - Clock Configuration Guide

by: NXP Semiconductors

## Contents



## 1. Introduction

NXP's S32G2 is a family of high-performance vehicle network processors that combines Controller Area Network (CAN), Local Interconnect Network (LIN), and FlexRay networking with high-data-rate Ethernet networking. It also combines a functional safe-core infrastructure with MPU cores and includes high-level security features.

S32G2 supports multiple clock sources for clock generation:

- Fast Internal RC Oscillator (FIRC) (48 MHz)
- Slow Internal RC Oscillator (SIRC) (32 KHz)
- Fast External Crystal Oscillator (FXOSC) (20 – 40 MHz)
- Phase-Locked Loops (PLLs)
- Digital Frequency Synthesizer (DFS) modules

This application note is intended to provide the user values for commonly used PLL/DFS configurations.

This document is accompanied with an attached clock configurator - S32G2_Clock_Configurator.xlsx. The calculator simplifies the clock configuration process by helping user find the recommended and validated values of PLL parameters (MFI, MFN and DIV), DFS parameters (MFI and MFN), MC_CGM parameters

(SELCTL and DIV) to achieve the target clock frequency along with the calculation of STEPNO and STEPSIZE for programming modulation depth and modulation frequency.

This document complements the S32G2 Reference Manual[1] and S32G2 Data Sheet[2]. Readers are advised to read through “Clocking” chapter from S32G2 Reference Manual[1] before further diving into this document.

The following table shows the abbreviations used throughout the document.

**Table1. Acronyms and abbreviations**

| Abbreviation | Explanation |
|---|---|
| DFS | Digital Frequency Synthesizer |
| EMI | Electromagnetic Interference |
| FIRC | Fast Internal RC Oscillator |
| $f_{MOD}$ | Modulation Frequency |
| $f_{PLL\_VCO}$ | PLL VCO frequency with SSCG enabled |
| $f_{REF}$ | PLL Reference Clock |
| FXOSC | Fast External Crystal Oscillator |
| LDF | Loop Division Factor |
| MD | Modulation Depth |
| PLL | Phase Locked Loop |
| SSCG | Spread Spectrum Clock Generation |

# 2. PLL

The document provides the coherent values for the following PLLs:

1. CORE_PLL
2. PERIPH_PLL
3. ACCEL_PLL
4. DDR_PLL

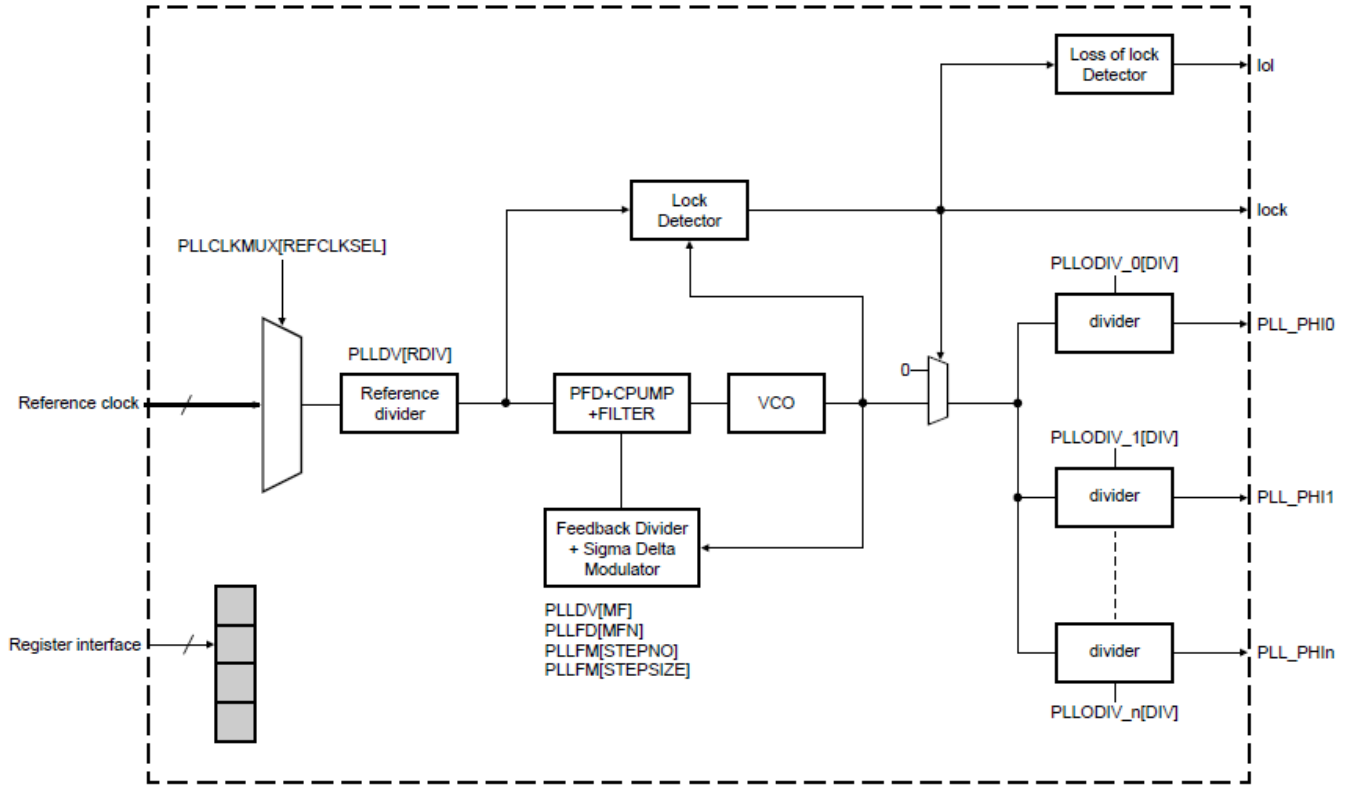


**Figure 1. PLL block diagram**

The user need to configure the value for below parameters to achieve the target frequencies for PLL_VCO and PLL_PHIn.

1. Reference clock : Clock sources for the PLLs can either be the 20 – 40 MHz FXOSC or 48 MHz FIRC. During boot, FIRC_CLK is used as the default PLL reference clock. After boot, the PLL reference must be changed to FXOSC_CLK. Ensure that PLLCLKMUX[REFCLKSEL] is selected accordingly.

   RDIV : PLL input reference clock frequency after pre-divider should be between 20 – 40 MHz, therefore the valid values for RDIV are shown in the following table.

**Table2. RDIV values**

| Frequency | RDIV |
|---|---|
| FXOSC – 20 MHz | 1 |
| FXOSC – 24 MHz | 1 |
| FXOSC – 40 MHz | 1 or 2 |
| FIRC – 48 MHz | 2 |

**NOTE**

For a crystal of 40 MHz, NXP recommends using RDIV = 1 for better jitter performance.

2. MFI : Integer part of LDF
3. MFN : Numerator of fractional LDF
4. DIV : Division value
5. STEPSIZE : Step size for modulation depth and frequency in frequency modulation mode
6. STEPNO : Number of steps to achieve modulation depth in frequency modulation mode.

# 3. DFS

The document provides the coherent values for following DFS:

1. CORE_DFS
2. PERIPH_DFS

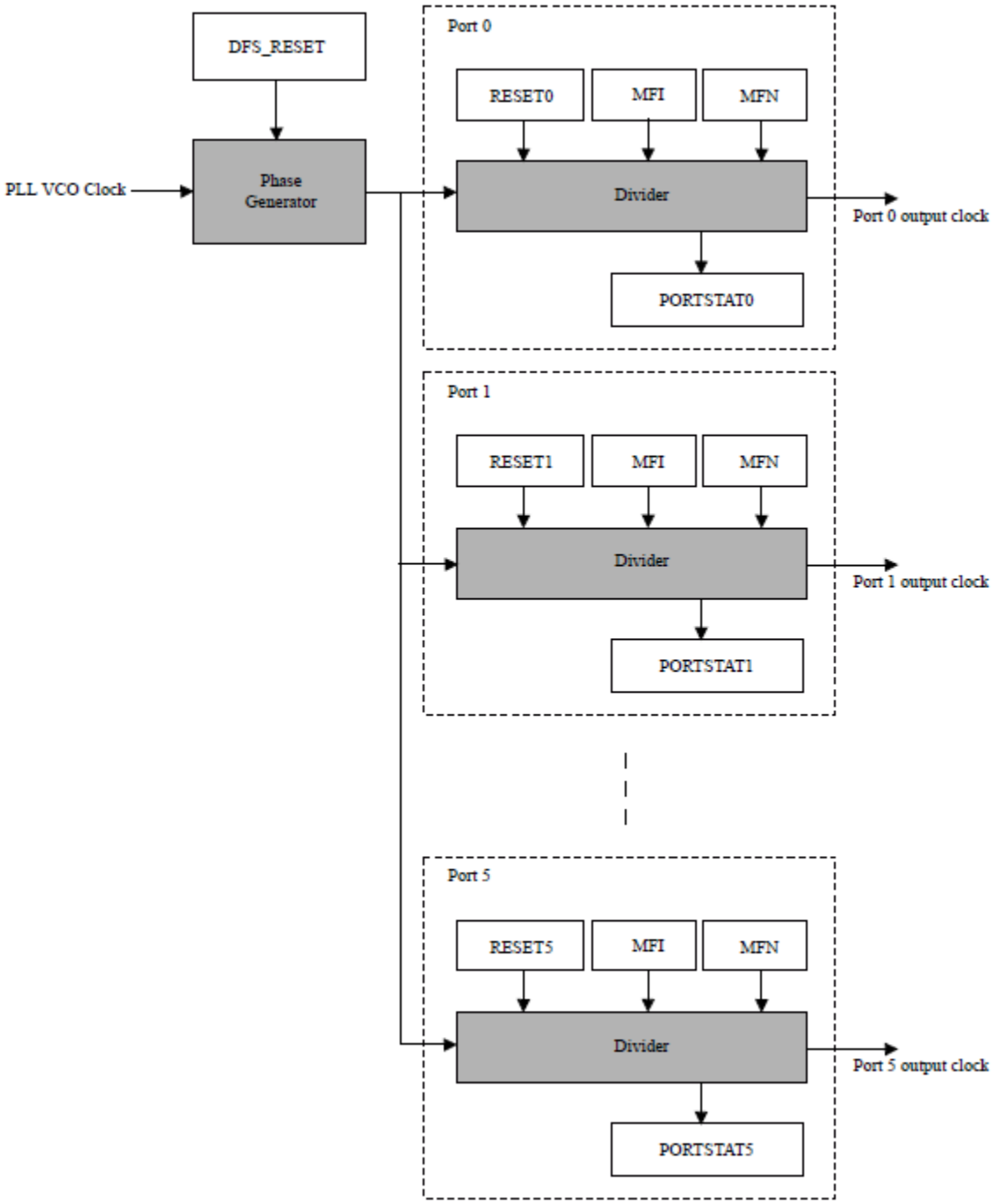


**Figure 2. DFS block diagram**

The user needs to configure the value for the below parameters to achieve the target frequencies for CORE_DFSn and PERIPH_DFSn.

1. PLL_VCO : Respective PLL_VCO frequency serves an input clock source to the DFS block.
2. MFI : Integer part of LDF.
3. MFN : Numerator of fractional LDF

# 4. Clock calculator design

The S32G2 clock configurator is in the form of an interactive Microsoft Excel spreadsheet organized in multiple tabs as explained in below sub-sections.

## 4.1 Options tab

The options tab provides an interface to select the following:

1. FXOSC frequency

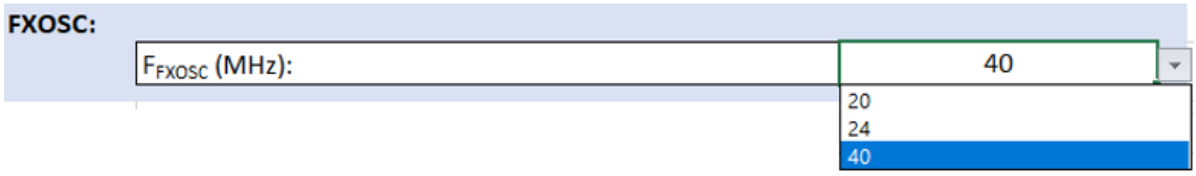


**Figure 3. Selecting FXOSC frequency**

2. RDIV – RDIV is selected individually for each PLL : CORE_PLL, PERIPH_PLL, ACCEL_PLL, DDR_PLL.


**Figure 4. Selecting RDIV value**

RDIV must be selected to ensure that the input frequency of each PLL is between 20 – 40 MHz.

3. Option to enable/disable SSCG for CORE_PLL, ACCEL_PLL and DDR_PLL.

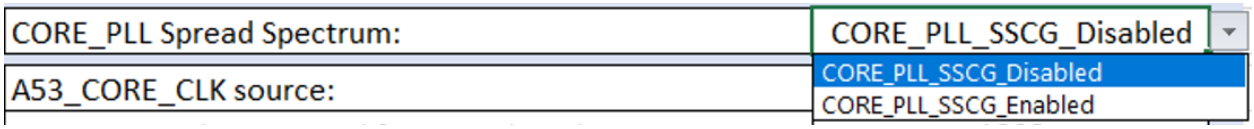


**Figure 5. Enabling/Disabling SSCG**

4. Clock Source – Select the clock source.

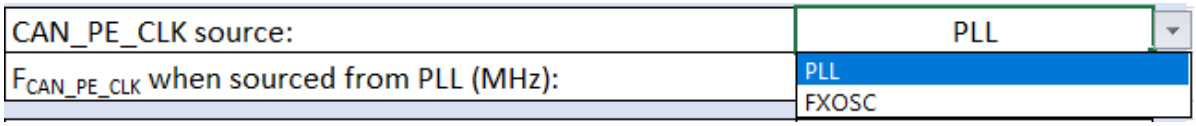


**Figure 6. Selecting the clock source**

5. Target Frequency – Select the target frequency.

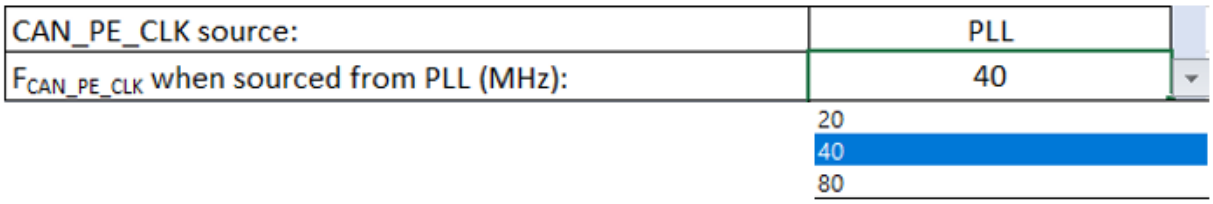


**Figure 7. Selecting the clock frequency**

In case of CORE_PLL, DDR_PLL, ACCEL_PLL, the sheet lists a set of frequencies to support the SSCG disabled case and the corresponding set of frequencies with 1.5% modulation depth for SSCG enabled case.

As an example for A53_CORE_CLK : In case SSCG is disabled, the calculator provides 500 MHz, 800 MHz and 1000 MHz frequency options.

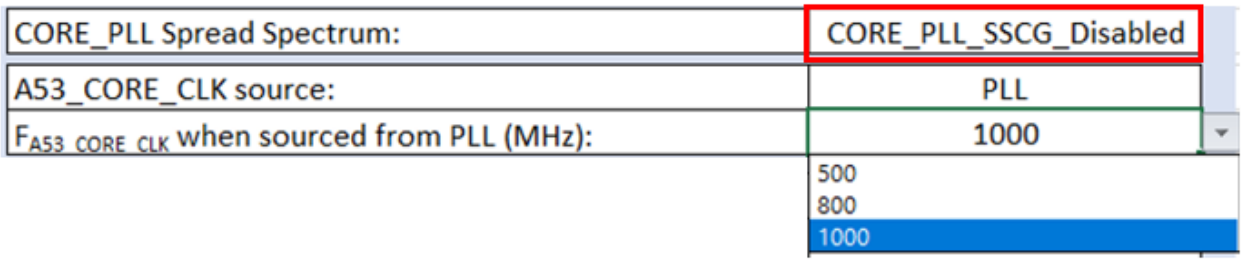


**Figure 8. $F_{A53\_CORE\_CLK}$ with SSCG disabled**

And when SSCG modulation is enabled, the calculator provides frequency options with 1.5% modulation depth - 496.3 MHz, 794 MHz, 992.5 MHz.

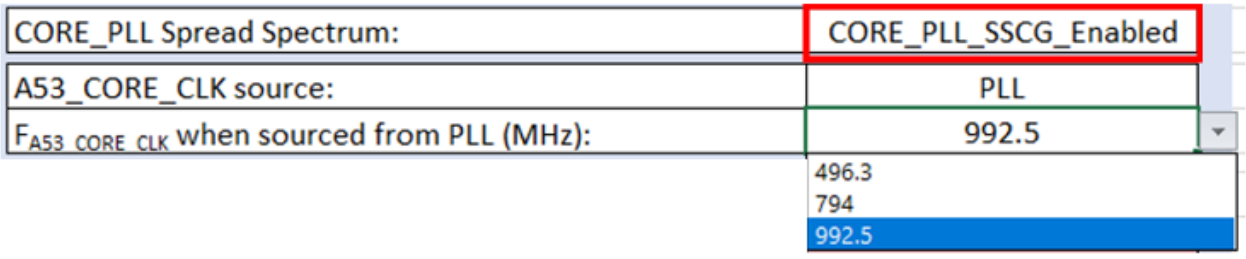


**Figure 9. $F_{A53\_CORE\_CLK}$ with SSCG enabled**

## 4.2 Configuration tab

After selecting the parameters in the options tab, the calculator provides the value for PLL parameters (MFI, MFN, DIV), DFS parameters (MFI, MFN) and MC_CGM parameters (SELCTL, DIV) in the configurations tab on the basis of the selection in the options tab.

As an example if the user selects the clock source for CAN_PE_CLK as PLL and 40 MHz as the target frequency with RDIV and FXOSC value as 1 and 40 MHz respectively, the configuration tab provides the values for clocking parameters as shown in the following image.

| PLL | | | | | | PHI / DFS | | | | MC_CGM | | | | | | Fixed Divider | Clock Domain | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Instance | $F_{REF}$ (MHz) | RDIV | MFI | MFN | $F_{VCO}$ (MHz) | Divider | DIV / MFI | MFN | Freq. (MHz) | Instance | Mux | SELCTL | Divider | DIV | Freq. (MHz) | | Name | Freq. (MHz) |
| PERIPH_PLL | 40 | 1 | 50 | 0 | 2000 | | | | | | | | | | | | | |
| | | | | | | PERIPH_PLL_PHI2 | 50 | - | 40 | MC_CGM_0 | MUX7 | 20 | - | | 40 | - | CAN_PE_CLK | 40 |

**Figure 10. Configurations as per the selected parameters**

## 4.3 Spread spectrum tab

With the help of this tab user can calculate values for STEPNO and STEPSIZE to program the modulation depth and the modulation frequency.

The calculator takes the below input parameters:

1. VCO frequency with SSCG disabled
2. Reference frequency
3. RDIV
4. Modulation frequency
5. Modulation depth

User needs to enter the value for VCO frequency with SSCG disabled, modulation frequency and modulation depth and select reference frequency and RDIV from the drop down list.

An example to calculate STEPNO and STEPSIZE for the CORE_PLL is shown below.

| | |
|---|---|
| $f_{REF}$ (Reference frequency) (MHz) | 40 |
| | |
| **CORE_PLL** | |
| **Parameters** | **Value** |
| MD (Modulation Depth) (%) | 1.5 |
| $f_{MOD}$ (Modulation frequency) (KHz) | 64 |
| $f_{PLL\_CORE\_VCO}$ (MHz) with SSCG disabled | 2000 |
| RDIV | 1 |
| | |
| $f_{PLL\_CORE\_VCO}$ (MHz) with SSCG enabled | 1985 |
| MFI | 49 |
| MFN | 11520 |
| STEPNO | 313 |
| STEPSIZE | 44 |

**Figure 11. Spread spectrum tab**

## 4.4 Clock calculator key considerations

1. RDIV – User must ensure that RDIV value remains in range when selecting or changing a FXOSC frequency and manually update the RDIV value such that an invalid option is not selected for the FXOSC frequency.

   As an example, if the initial values for FXOSC and RDIV are selected as 40 MHz and 2 respectively and the user update the FXOSC frequency to 20 MHz, the RDIV block turns pink to indicate the RDIV holds an invalid option for the selected FXOSC frequency. Therefore, the user must correct the RDIV value in case the FXOSC frequency is updated.

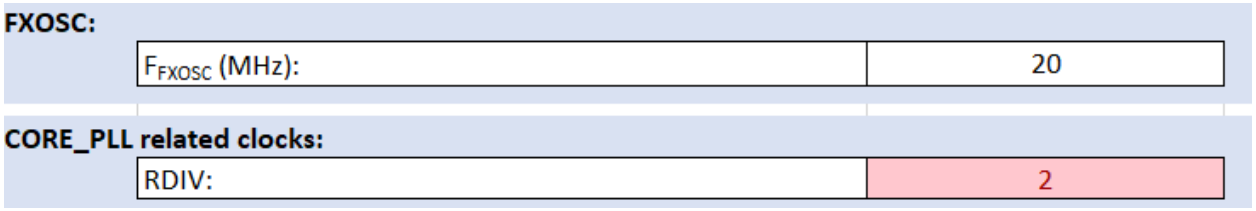


**Figure 12. Invalid RDIV error**

   Same precaution needs to be taken care while updating the FXOSC frequency in Spread Spectrum tab.

2. Target frequency – As explained above, caution needs to be exercised while enabling or disabling the SSCG mode. User should manually update the frequency when SSCG mode is updated.

   As an example, if Spread Spectrum is enabled for DDR_PLL and DDR_CLK is selected as 794 MHz and the user disables the spread spectrum, the $F_{DDR\_CLK}$ block turns pink to indicate user to update the $F_{DDR\_CLK}$ from the list of frequencies in SSCG disabled mode.

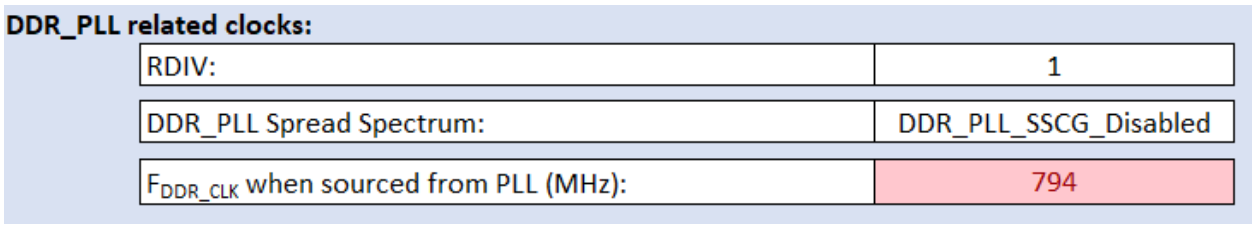


**Figure 13. Frequency update error**

3. In the Spread Spectrum tab, user must ensure that the specified value for VCO frequency with SSCG disabled, Modulation frequency and Modulation depth are within range as specified in section Spread Spectrum Considerations.

   Any invalid value selection leads to the specified parameter block turning pink. User must adjust the value of specified parameter to be within range.

| CORE_PLL | |
|---|---|
| **Parameters** | **Value** |
| MD (Modulation Depth) (%) | 1.5 |
| $f_{MOD}$ (Modulation frequency) (KHz) | 64 |
| $f_{PLL\_CORE\_VCO}$ (MHz) with SSCG disabled | 2400 |
| RDIV | 1 |
| | |
| $f_{PLL\_CORE\_VCO}$ (MHz) with SSCG enabled | 2382 |
| MFI | 59 |
| MFN | 10137 |
| STEPNO | 313 |
| STEPSIZE | 53 |

**Figure 14. VCO frequency out of specified range**

# 5. Spread spectrum

Spread Spectrum clocking is a technique used in electronic design to intentionally modulate the ideal position of the clock edge such that the resulting signal's spectrum is "spread" around the ideal frequency of the clock. Spread Spectrum clocking is often used to help meet the regulated EMI requirements.

This section provides the user instructions on how to enable Spread Spectrum functionality.

For S32G2, Spread Spectrum clock modulation is only available for the Core, Accelerator and DDR PLLs.

PLL operates in frequency modulation mode when the user sets the following bits as shown in the table below –

**Table 3. Mode to enable spread spectrum**

| PLLCR[PLLPD] | PLLFD[SDMEN] | PLLFM[SSCGBYP] | PLLFM[SPREADCTL] |
|---|---|---|---|
| 0 | 1 | 0 | 0 |

## 5.1 Frequency modulation programming

Modulation depth and modulation frequency programming uses step number (PLLFM[STEPNO]) and step size (PLLFM[STEPSIZE]) which can be calculated by using the below equations:

$$PLLFM[STEPNO] = \frac{f_{REF}}{2 \times f_{MOD} \times PLLDIV[RDIV]}$$

**Equation 1**

$$PLLFM[STEPSIZE] = \frac{MD \times LDF}{100 \times PLLFM[STEPNO]} \times 18432$$

**Equation 2**

where,

$$LDF = PLLDIV[MFI] + \frac{PLLDIV[MFN]}{18432}$$

**Equation 3**

Frequency Modulation is only possible if the condition shown in the below equation is met –

$$(PLLFM[STEPSIZE] \times PLLFM[STEPNO]) < 18432$$

**Equation 4**

The maximum possible modulation depth is:

$$Max\ (MD\ \%) = \frac{f_{\text{REF}} \times 100}{PLLDIV[RDIV] \times f_{\text{PLL\_VCO}}}$$

**Equation 5**

**NOTE**

The effective modulation depth may differ from the intended modulation depth because of rounding operations applied to PLLFM[STEPSIZE] and PLLFM[STEPNO].

## 5.2 Spread Spectrum Considerations

User must adhere to the below specification while using Spread Spectrum:

### 5.2.1 PLL VCO

The max frequency in case of center-spread SSCG enabled ($f_{\text{PLL\_VCO}}$) for a modulation depth can be selected as –

$$Max\ frequency(in\ case\ of\ center-spread\ SSCG\ enabled) = Max\ frequency(in\ case\ of\ center-spread\ SSCG\ disabled) - \frac{Modulation\ Depth}{2} * Max\ frequency(in\ case\ of\ center-spread\ SSCG\ disabled)$$

**Equation 6**

### 5.2.2 Modulation frequency

With center-spread SSCG enabled the modulation frequencies for Core, Accelerator and DDR must be within the range as specified in the table below.

**Table 4. Modulation frequency range with center-spread modulation enabled**

| Symbol | Description | Modulation frequency range (KHz) |
|---|---|---|
| fPLL_MOD | Spread Spectrum Clock Modulation Frequency | 30 – 64 |

### 5.2.3 Modulation depth

With center-spread SSCG enabled, the modulation depth for Core, Accelerator and DDR must adhere to below conditions –

1. $PLLFM[STEPSIZE] \times PLLFM[STEPNO] < 18432$
2. $MD\ \% < \frac{f_{REF} \times 100}{PLLDIV[RDIV] \times f_{PLL\_VCO}}$

## 5.3 Example code

This section illustrates how to configure modulation frequency and modulation depth with the help of an example.

Example: Enabling SSCG for CORE_PLL_VCO frequency of 2000 MHz (in case of SSCG disabled), with modulation frequency of 64 KHz and 1.5% modulation depth.

**Table 5. Example values**

| Variables | Value |
|---|---|
| $f_{REF}$ | 40 MHz |
| $f_{MOD}$ | 64 KHz |
| MD | 1.5 |

In the Spread Spectrum tab in the attached Excel tool, enter the following –

$f_{PLL\_CORE\_VCO}$ with SSCG disabled as 2000 MHz,

$f_{MOD}$ as 64 KHz,

MD % as 1.5

And select the FXOSC ($f_{REF}$) frequency and RDIV from the drop list.

| | |
|---|---|
| $f_{REF}$ (Reference frequency) (MHz) | 40 |
| | |
| CORE_PLL | |
| **Parameters** | **Value** |
| MD (Modulation Depth) (%) | 1.5 |
| $f_{MOD}$ (Modulation frequency) (KHz) | 64 |
| $f_{PLL\_CORE\_VCO}$ (MHz) with SSCG disabled | 2000 |
| RDIV | 1 |

**Figure 15. Input parameters in spread spectrum tab**

The configurator will output the value of fPLL_CORE_VCO with SSCG enabled, MFI, MFN, STEPNO and STEPSIZE.

| | |
|---|---|
| $f_{PLL\_CORE\_VCO}$ (MHz) with SSCG enabled | 1985 |
| MFI | 49 |
| MFN | 11520 |
| STEPNO | 313 |
| STEPSIZE | 44 |

**Figure 16. Output of spread spectrum tab**

The user needs to use these values and program the PLL register fields as follows:

```
/* PLL configuration with center-spread enabled --> CORE_PLL VCO frequency = 1985 MHz */
CORE_PLL.PLLDV.B.RDIV = 1;
CORE_PLL.PLLDV.B.MFI = 49;
CORE_PLL.PLLFD.B.MFN = 11520;
/* Enable SSCG at 64 KHz */
CORE_PLL.PLLFM.B.SSCGBYP = 0; /* Spread spectrum modulation is not bypassed */
CORE_PLL.PLLFM.B.SPREADCTL = 0;   /* Center Spread modulation */
/* fMOD = 64 KHz, MD = 1.5% */
CORE_PLL.PLLFM.B.STEPNO    = 313;
CORE_PLL.PLLFM.B.STEPSIZE  = 44;
CORE_PLL.PLLFD.B.SDMEN     = 1;   /* Enable Sigma Delta Modulation */
```

# 6 Clock Configuration using S32DS Clocks Tool

The S32DS Clocks Tool allows the user to easily configure the system clocks, including core and peripheral clocks, and then generate 32 bit register values and C-code.

Visual inspection of the configured clock paths is available using the graphical clock tree.

The Clocks Tool validates clock settings and provides calculations of the resulting clock frequencies.

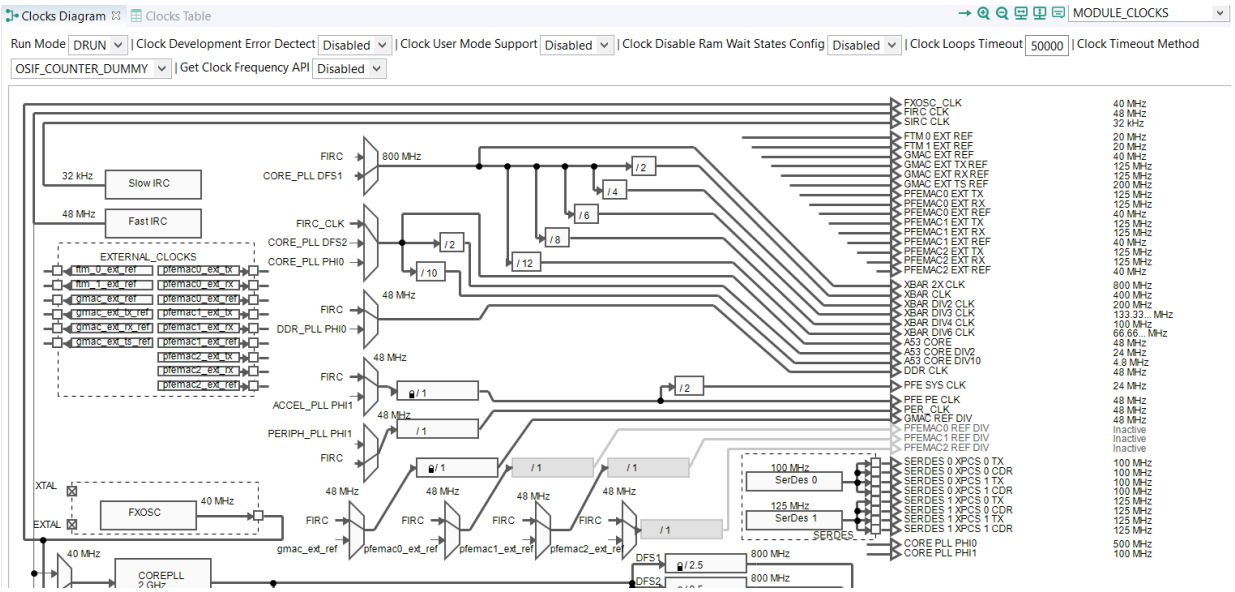


**Figure 17. Clocks diagram view**

Overview | Peripheral Clock View | Code Preview | Registers | Details | Clock Consumers

*all*

type filter text

| Reg. Name | Set Value | Reset Value | Value Description |
|---|---|---|---|
| PERIPH_DFS_DVPORT0 | 0x00000109 | 0x00000000 | Divider for Port 0 |
| PERIPH_DFS_DVPORT1 | 0x00000115 | 0x00000000 | Divider for Port 1 |
| PERIPH_DFS_DVPORT2 | 0x00000109 | 0x00000000 | Divider for Port 2 |
| PERIPH_DFS_DVPORT3 | 0x00000200 | 0x00000000 | Divider for Port 3 |
| PERIPH_DFS_DVPORT4 | 0x00000200 | 0x00000000 | Divider for Port 4 |
| PERIPH_DFS_DVPORT5 | 0x00000200 | 0x00000000 | Divider for Port 5 |
| PERIPH_DFS_PORTRESET | 0x00000000 | 0x0000003f | Port Reset |
| PERIPH_PLL_PLLCLKMUX | 0x00000001 | 0x00000000 | PLL Clock Multiplexer |
| PERIPH_PLL_PLLCR | 0x00000000 | 0x80000000 | PLL Control Register |
| PERIPH_PLL_PLLDV | 0x0c3f1032 | 0x0c3f1032 | PLL Divider |
| PERIPH_PLL_PLLFD | 0x00000000 | 0x00000000 | PLL Fractional Divider |
| PERIPH_PLL_PLLODIV_0 | 0x800f0000 | 0x00000000 | PLL Output Divider |
| PERIPH_PLL_PLLODIV_1 | 0x80180000 | 0x00000000 | PLL Output Divider |
| PERIPH_PLL_PLLODIV_2 | 0x80180000 | 0x00000000 | PLL Output Divider |
| PERIPH_PLL_PLLODIV_3 | 0x800f0000 | 0x00000000 | PLL Output Divider |
| PERIPH_PLL_PLLODIV_4 | 0x80090000 | 0x00000000 | PLL Output Divider |
| PERIPH_PLL_PLLODIV_5 | 0x800f0000 | 0x00000000 | PLL Output Divider |
| PERIPH_PLL_PLLODIV_6 | 0x80130000 | 0x00000000 | PLL Output Divider |
| PERIPH_PLL_PLLODIV_7 | 0x80130000 | 0x00000000 | PLL Output Divider |

**Figure 18. Clock Register view**

**NOTE**

Similar clock configuration can also be done using EB tresos.

# 7 References

1. S32G2 Reference Manual
2. S32G2 Data Sheet

**NOTE**

S32G2-related documents are available on nxp.com

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