AN13416

i.MX 8M Nano with New Package Migration Guide

Migrating from "VT" package to "UC" package

Rev. 1 — 08 June 2022 Application Note

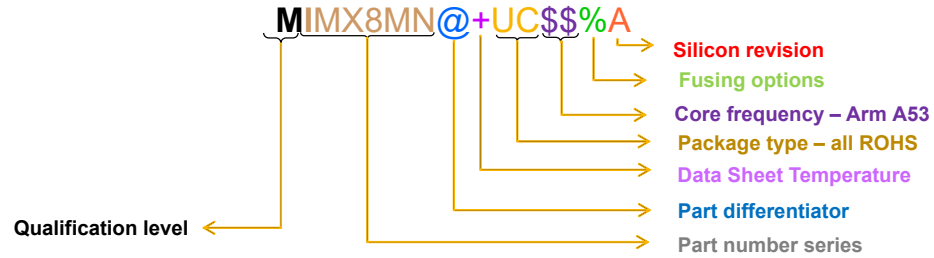
Contents

1 Introduction

This application note introduces the i.MX 8M Nano with replacement new package (UC type) by highlighting the differences from the original discontinued package (VT type). The original part number is discontinued and replaced with new part marking and new orderable part numbers. This migration guide is useful for the i.MX 8M Nano developers that migrate from the discontinued **VT** package to the replacement **UC** package.

1.1 i.MX 8M Nano with new package

NXP is migrating the i.MX 8M Nano to a pin compatible replacement package.



Qualification level	
Samples	P
Mass Production	M

Part number series	Description
IMX8MN	i.MX 8M Nano

Part differentiator	@
i.MX 8M Nano Quad GPU, 4x A53	6
i.MX 8M Nano QuadLite No GPU, 4x A53	5
i.MX 8M Nano Dual GPU, 2x A53	4
i.MX 8M Nano DualLite No GPU, 2x A53	3
i.MX 8M Nano Solo GPU, 1x A53	2
i.MX 8M Nano SoloLite No GPU, 1x A53	1

Temperature Tj	+
Consumer: 0 to +95 °C	D
Industrial: -40 to 105 °C	C

Package Type	ROHS
FCBGA486 14x14 mm, 0.5 mm pitch	UC

A53 core frequency	$$
1.5 GHz	JZ
1.4 GHz	IZ

Fusing	%
Default	A
Immersiv3D	B
Immersiv3D w/ Dolby Atmos	C
Immersiv3D w/ Dolby Atmos & DTS	D

Silicon Rev	A
Rev A0	A

Figure 1. Part number nomenclature – i.MX 8M Nano family of processors

Table 1. Part number changes

Discontinued part numbers: "VT" package	New part numbers: "UC" package	Options	Cortex-A53 CPU speed grade	Qualification tier	Temperature Tj (°C)	Package
MIMX8MN6DVTJZAA	P/MIMX8MN6DUCJZAA	A53, M7, GPU, MIPI DSI	1.5 GHz	Consumer	0 to 95	14 × 14 mm, 0.5 mm pitch
MIMX8MN6DVTJZCA	P/MIMX8MN6DUCJZCA	4 × A53, M7, GPU, Immersiv3D with Dolby ATMOS support, MIPI DSI	1.5 GHz	Consumer	0 to 95	14 × 14 mm, 0.5 mm pitch
MIMX8MN6DVTJZBA	MIMX8MN6DUCJZBA	4 × A53, M7, GPU, Immersiv3D with MPEG, MIPI DSI	1.5 GHz	Consumer	0 to 95	14 × 14 mm, 0.5 mm pitch
MIMX8MN6DVTJZDA	P/MIMX8MN6DUCJZDA	4 × A53, M7, GPU, Immersiv3D with Dolby ATMOS and DTS support, MIPI DSI	1.5 GHz	Consumer	0 to 95	14 × 14 mm, 0.5 mm pitch
MIMX8MN5DVTJZAA	P/MIMX8MN5DUCJZAA	4 × A53, M7, No GPU, MIPI DSI	1.5 GHz	Consumer	0 to 95	14 × 14 mm, 0.5 mm pitch
MIMX8MN4DVTJZAA	P/MIMX8MN4DUCJZAA	2 × A53, M7, GPU, MIPI DSI	1.5 GHz	Consumer	0 to 95	14 × 14 mm, 0.5 mm pitch
MIMX8MN3DVTJZAA	P/MIMX8MN3DUCJZAA	2 × A53, M7, No GPU, MIPI DSI	1.5 GHz	Consumer	0 to 95	14 × 14 mm, 0.5 mm pitch
MIMX8MN2DVTJZAA	P/MIMX8MN2DUCJZAA	1 × A53,	1.5 GHz	Consumer	0 to 95	14 × 14 mm,

Table continues on the next page...

Table 1. Part number changes (continued)

Discontinued part numbers: "VT" package	New part numbers: "UC" package	Options	Cortex-A53 CPU speed grade	Qualification tier	Temperature Tj (°C)	Package
		M7, GPU, MIPI DSI				0.5 mm pitch
MIMX8MN1DVTJZAA	P/MIMX8MN1DUCJZAA	1 × A53, M7, No GPU, MIPI DSI	1.5 GHz	Consumer	0 to 95	14 × 14 mm, 0.5 mm pitch
MIMX8MN6CVTIZAA	P/MIMX8MN6CUCIZAA	4 × A53, M7, GPU, MIPI DSI	1.4 GHz	Industrial	-40 to 105	14 × 14 mm, 0.5 mm pitch
MIMX8MN5CVTIZAA	P/MIMX8MN5CUCIZAA	4 × A53, M7, No GPU, MIPI DSI	1.4 GHz	Industrial	-40 to 105	14 × 14 mm, 0.5 mm pitch
MIMX8MN4CVTIZAA	P/MIMX8MN4CUCIZAA	2 × A53, M7, GPU, MIPI DSI	1.4 GHz	Industrial	-40 to 105	14 × 14 mm, 0.5 mm pitch
MIMX8MN3CVTIZAA	P/MIMX8MN3CUCIZAA	2 × A53, M7, No GPU, MIPI DSI	1.4 GHz	Industrial	-40 to 105	14 × 14 mm, 0.5 mm pitch
MIMX8MN2CVTIZAA	P/MIMX8MN2CUCIZAA	1 × A53, M7, GPU, MIPI DSI	1.4 GHz	Industrial	-40 to 105	14 × 14 mm, 0.5 mm pitch
MIMX8MN1CVTIZAA	P/MIMX8MN1CUCIZAA	1 × A53, M7, No GPU, MIPI DSI	1.4 GHz	Industrial	-40 to 105	14 × 14 mm, 0.5 mm pitch

2 Feature change summary

This topic summarizes any feature changes such as functionality, BSP support, package difference, thermal resistance, and reflow profile.

2.1 Functionality

No change in the functionality.

2.2 BSP support

No change in the software.

2.3 Package difference

The package difference is summarized in Table 2. The replacement package is pin compatible to the discontinued package. Therefore, a board schematic design is not required while board layout might need to be updated if customers meet soldering short issue. See Assembly checklist.

Table 2. Package difference summary

Package	Discontinued "VT" Package (mm)	Replacement "UC" Package (mm)
Thickness	1.15 ± 0.1	0.775 ± 0.1
BGA Ball Coplanarity	0.08	0.1
Shipment trays	ITW 14 × 14 BGA 41414-11-0819-9 (150C)	PEAK TX BG1414 1.25 0717 6 (150C)

Compared to the discontinued package, the thinner replacement package contains a different characteristic shape at solder reflow temperatures, as shown in Figure 2. Certain PC board designs using soldermask defined pads may experience soldering issues with the replacement package. For more details and recommendations, see Board assembly.

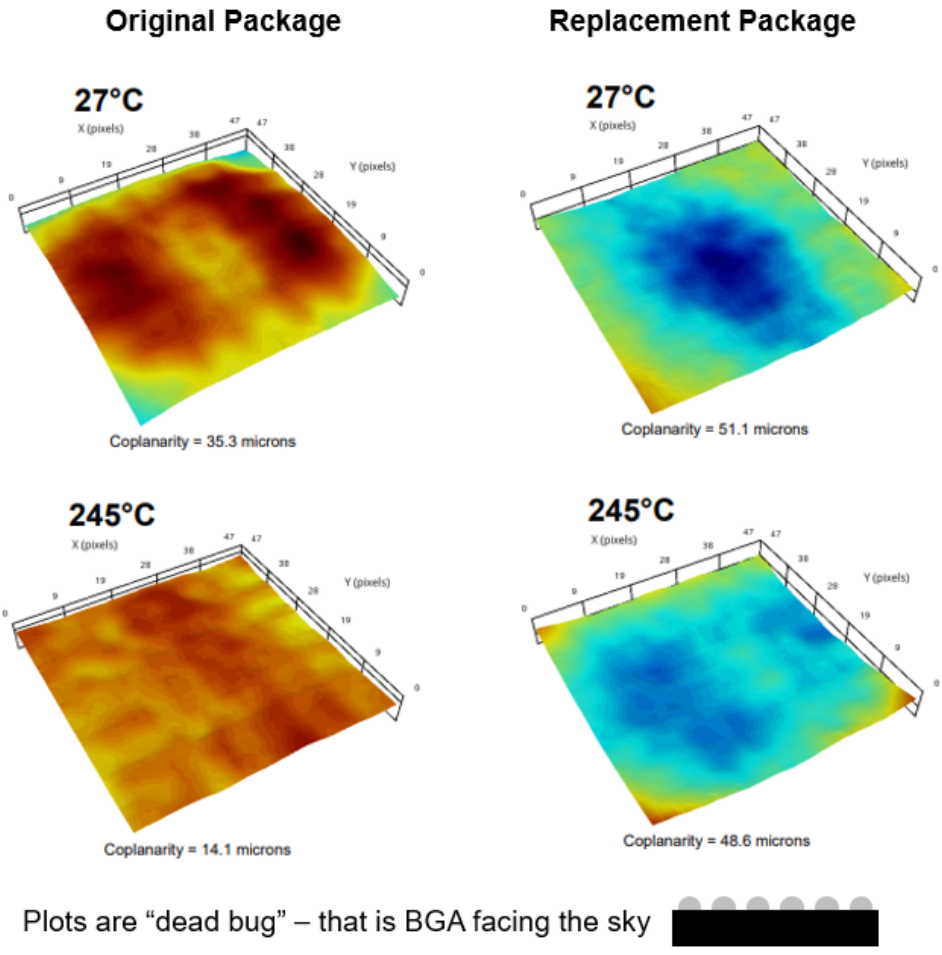


Figure 2. 3-D overview of original and replacement package shapes at room and peak reflow temperatures

2.4 Assembly checklist

To help prepare for conversion to the replacement package, complete the below checklist and then perform a trial assembly run with a minimum of 30 parts.

i.MX 8M Nano new package assembly checklist contains:

1. Component pick-up and place height adjusted to compensate for the thinner package.
2. Check placement force. Excessive placement force may contribute to solder bridging.
3. Board reflow profile verified with temperature sensors located at package top and BGA solder joint. See Reflow profile.
4. Component top and BGA solder joint temperatures less than 245C during reflow. See Reflow profile.
5. Non-soldermask defined PC board pad design. See Printed circuit board pad design.
6. 0.250 mm PC board pad diameter. See Printed circuit board pad design.
7. 0.330 mm PC board soldermask opening. See Printed circuit board pad design.
8. Verify that the PC board design is compliant with the PC board supplier Design For Manufacturability (DFM) rules. Check that the actual PB board pad diameter and soldermask opening match design values. Watch for truncated pads and soldermask openings.
9. Solder stencil aperture diameter matching PC board pad diameter or slightly reduced. See Solder stencil design.
10. Stencil apertures in corner keep-out regions reduced by 10 % to 15 %. See Solder stencil design.
11. Assembly is performed with production board and assembly process (not a rework process).
12. Perform 100 % X-ray and sample cross-section: Check for Head-In-Pillow (HIP) and bridging solder joints.

If customers meet soldering short issue at the four corners of the chip, prioritize to try Reflow profile and Solder stencil design.

2.5 Thermal resistance

Table 3 lists the minor differences in the thermal resistance. According to the simulation result based on 8MNANOLPD4-EVK, thermal redesign should not be required. However, customer must evaluate redesigning based on their board size, thermal design, casing, user case, power data, and so on.

Table 3. Package difference summary

Rating	Test Condition	Symbol	Discontinued 'VT' Package	Replacement 'UC' Package	Unit	Notes
Junction to Ambient Natural Convection	Four Layer Board (2s2p)	$R_{\theta JA}$	**22.9**	**22.2**	°C/W	1, 2, 4
Junction to Case	-	$R_{\theta JC}$	**4**	**5.1**	°C/W	3, 4
Junction to Package Top	Four Layer Board (2s2p)	Ψ_{JT}	**0.2**	**0.2**	°C/W	4, 5

NOTE

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components in the board, and board thermal resistance.
2. Per SEMI G38-87 and JESD51-2a horizontal board.
3. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
4. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standard-specific environment. It is not meant to predict the performance of a package in an application-specific environment.
5. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2a. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

2.6 IBIS model

IBIS model is different due to improvements in RLC of the replacement package. The updated model can be found at https://www.nxp.com/imx8mnano.

NOTE

Better DDR PI/SI simulation result due to overall improvement in parasitic of replacement package.

DDR package trace delays for the replacement package updated in the i.MX 8M Nano Hardware Developer's Guide.

2.7 DDR package trace delays

DDR package trace delay has minor difference from the discontinued package because of substrate change. Table 4 describes the differences between the two packages trace delays. Customers can refer to HDG and check whether their boards with new replacement package can meet the DDR routing constraints or not. Generally it does not require board re-spin because the differences are within the constraints recommended in HDG.

Table 4. i.MX8MN old/new package DDR length

Ball name	Delay (ps)		Ball name	Delay (ps)	
	Old	New		Old	New
DRAM_AC00	51.2	48.2	DRAM_AC32	34.3	33.2
DRAM_AC01	39.9	39.1	DRAM_AC33	38.6	37.8
DRAM_AC02	35.9	37.3	DRAM_AC34	43.1	41.3
DRAM_AC03	44.2	42.7	DRAM_AC35	51.2	49.0
DRAM_AC04	41.1	41.0	DRAM_AC36	26.5	27.0
DRAM_AC05	41.2	41.3	DRAM_AC37	35.1	32.9
DRAM_AC06	45.7	44.2	DRAM_AC38	42.1	39.9
DRAM_AC07	35.8	35.7	DRAM_ALERT_N	36.0	36.8
DRAM_AC08	39.6	36.2	DRAM_RESET_N	38.1	39.4
DRAM_AC09	29.1	28.7	DRAM_DM0	57.2	54.3

Table continues on the next page...

Table 4. i.MX8MN old/new package DDR length (continued)

Ball name	Delay (ps)		Ball name	Delay (ps)	
	Old	New		Old	New
DRAM_AC10	54.8	53.8	DRAM_DM1	58.6	55.4
DRAM_AC11	59.7	58.4	DRAM_DQ00	47.2	45.8
DRAM_AC12	33.8	33.6	DRAM_DQ01	43.0	42.1
DRAM_AC13	32.0	32.2	DRAM_DQ02	54.6	49.9
DRAM_AC14	43.1	42.9	DRAM_DQ03	51.7	49.3
DRAM_AC15	22.4	23.7	DRAM_DQ04	59.9	58.3
DRAM_AC16	39.1	39.7	DRAM_DQ05	58.1	57.9
DRAM_AC17	39.4	39.6	DRAM_DQ06	64.6	61.8
DRAM_AC19	43.4	43.2	DRAM_DQ07	51.4	49.8
DRAM_AC20	51.6	50.1	DRAM_DQ08	45.0	43.8
DRAM_AC21	51.6	50.6	DRAM_DQ09	50.1	47.5
DRAM_AC22	47.7	45.2	DRAM_DQ10	46.2	44.4
DRAM_AC23	40.0	38.4	DRAM_DQ11	47.2	45.0
DRAM_AC24	41.8	42.2	DRAM_DQ12	40.3	39.8
DRAM_AC25	42.2	42.7	DRAM_DQ13	48.8	47.6
DRAM_AC26	53.4	50.8	DRAM_DQ14	58.4	55.5
DRAM_AC27	29.0	27.1	DRAM_DQ15	52.4	50.1
DRAM_AC28	31.9	30.8	DRAM_DQS0_N	58.9	58.0
DRAM_AC29	34.4	32.2	DRAM_DQS0_P	59.0	58.1
DRAM_AC30	59.5	57.3	DRAM_DQS1_N	47.2	47.5
DRAM_AC31	56.5	55.5	DRAM_DQS1_P	48.6	47.8

2.8 Board assembly

2.8.1 Printed circuit board pad design

NXP strongly recommends Non-SolderMask Defined (NSMD) pads for 100 % of the pads on the PC Board. It includes pads formed over ground planes. As mentioned in Package difference, compared to the discontinued package, the thinner replacement package contains a different characteristic shape at solder reflow temperatures. While package flatness is still within NXP specifications, the corners of the replacement package tend to bend down toward the PC board when the package is above the melting temperature of typical SnAg or SAC solders, as illustrated in Figure 3.

Figure 3. Characteristic shape of replacement package at reflow temperature

SolderMask Defined (SMD) or a mixture of NSMD and SMD PC board pads are not recommended because the SMD design can cause solder to flow on top of the soldermask surrounding the pad, potentially resulting in solder bridging, as illustrated in Figure 4.

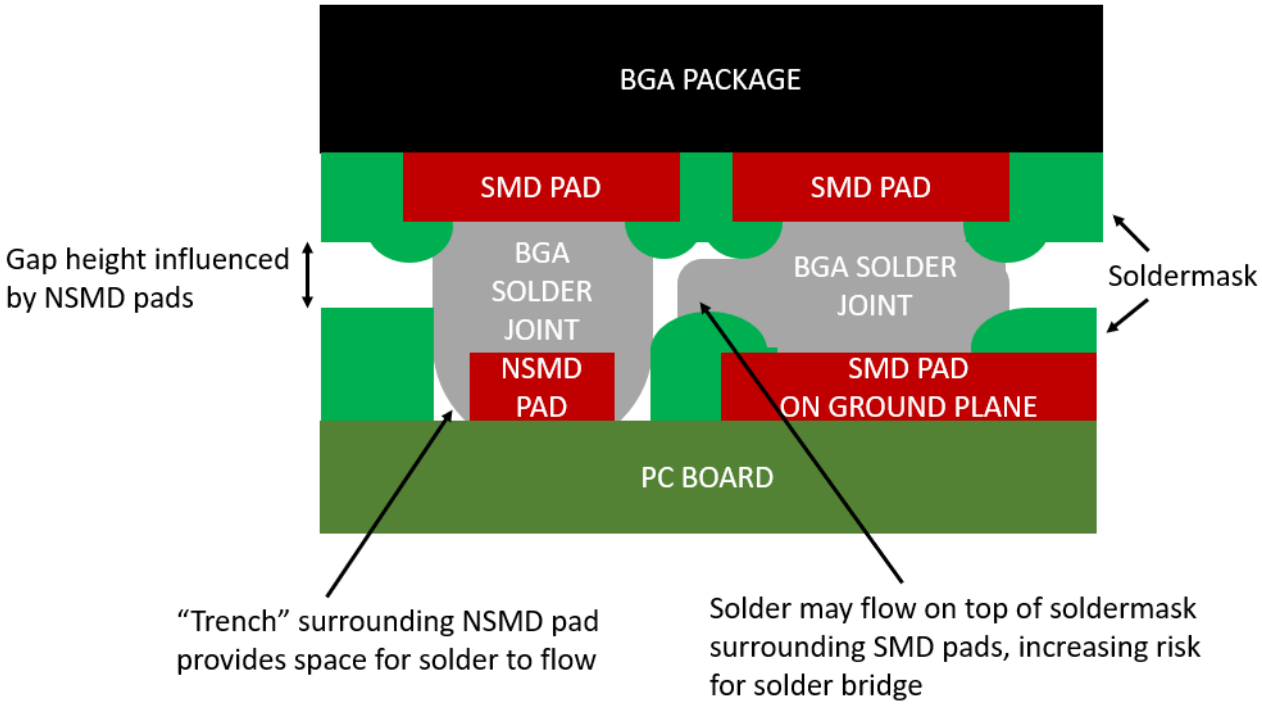


Figure 4. Illustration of solder "squeeze-out" with SMD pad design

Understandably, the preference is often to create an SMD pad over ground planes for electrical and design simplicity motivations. As illustrated above, this may increase the risk of solder bridging. NXP recommends to use a **ground plane relief** design where an opening is created in the plane for placement of an NSMD pad, as shown in Figure 5. The pad is connected to the plane by multiple metal lines. This design maintains the **trench** around the pad to capture molten solder that may be pushed out during the dynamic package bending during reflow. The recommended feature sizes for this NSMD pad design are:

- 0.250 mm round pad
- 0.330 mm round SRO opening
- 0.420 mm diameter **hole** in Cu plane

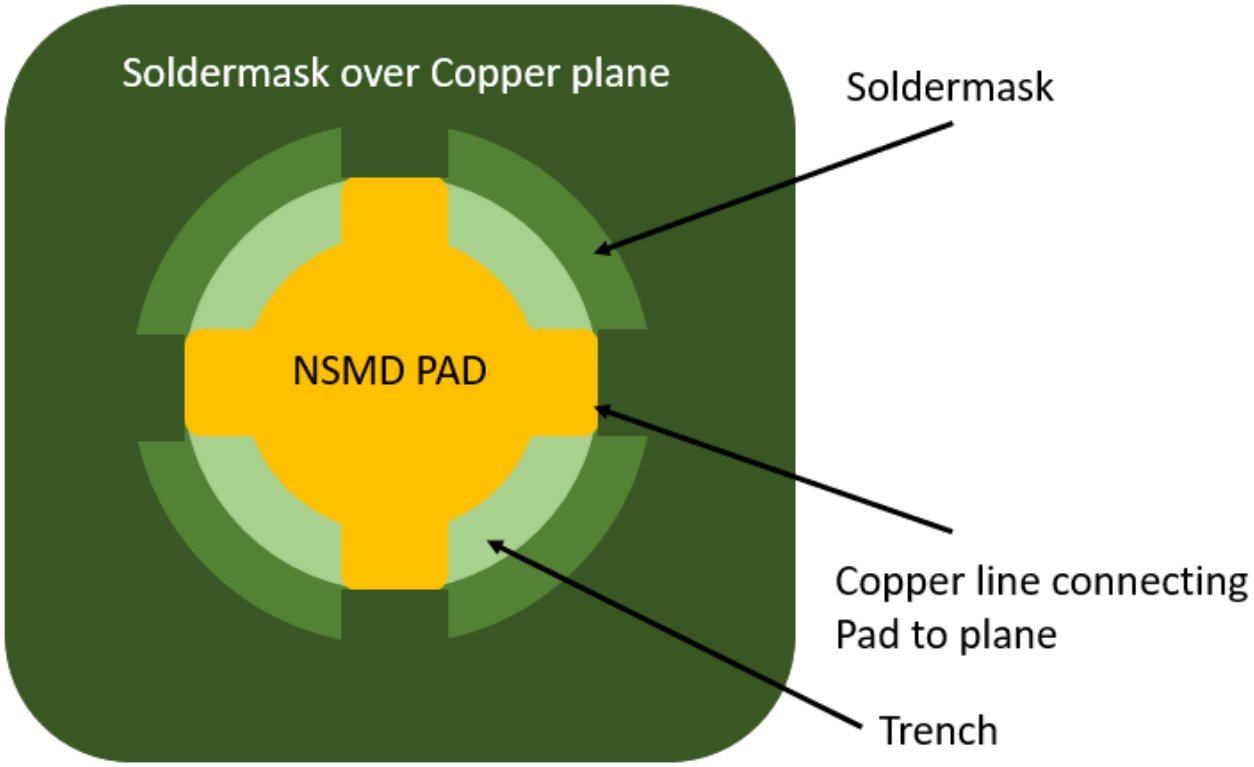


Figure 5. Ground plane relief NSMD PC board pad design

If manufacturing or electrical constraints prohibit the use of NSMD pad design over ground planes, while not recommended, a mixed SMD and NSMD design may be used outside of corner regions which are defined by a 3 × 3 BGA array at each of the four package corners. See Figure 6. NXP strongly recommends that Design For Manufacturability (DFM) checks and electrical simulations are done to realize a design with 100 % NSMD pads. To use SMD pads, use the following feature sizes for the SMD pad design:

- 0.380 mm round pad
- 0.300 mm round SRO opening

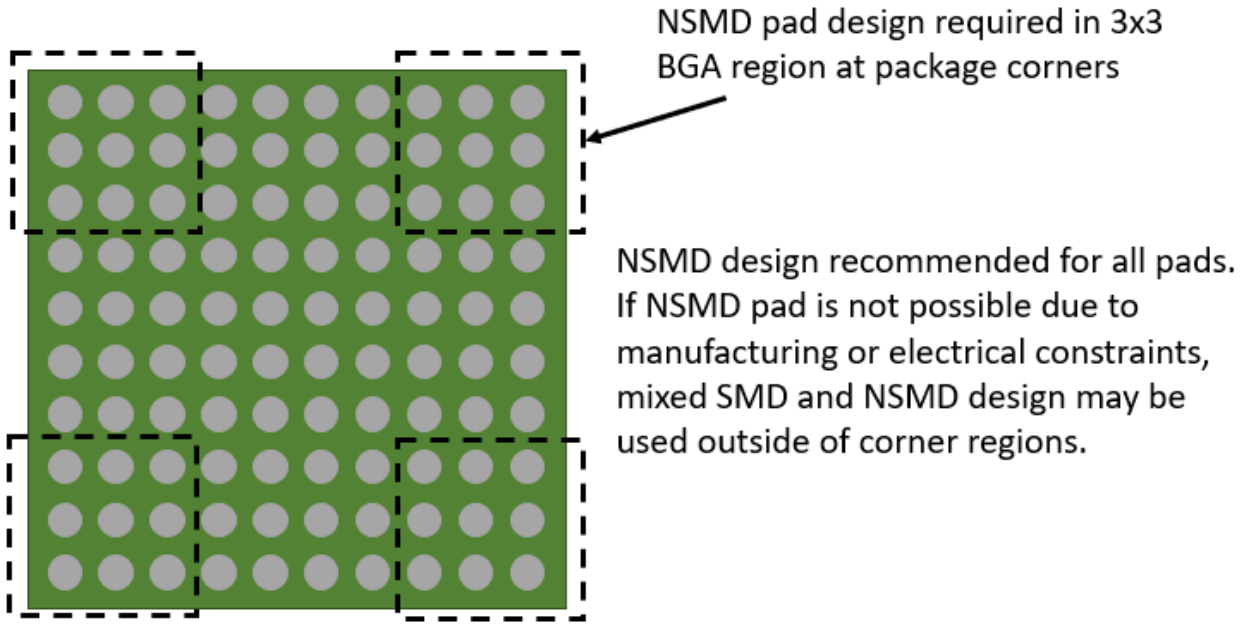


Figure 6. SMD pad design keep-out zones

2.8.2 Solder stencil design

For BGA, the typical stencil aperture diameter should be the same size as the PCB solder pad or solder mask opening for SMD designs. Slight reductions (0.02 - 0.05 mm) of the stencil diameter to the PCB pad diameter may improve gasket between the stencil and PCB. It helps with solder paste release. 100 um thick stencils have been found to give good results. Thin Flip Chip – Chip Scale Packages (FCCSPs) may bend down toward the PC board at the corners during reflow. To reduce the risk of solder bridging at package corners, a slightly reduced (10 -15 %) stencil aperture at the corner BGA locations may be beneficial. The recommended aperture sizes for the replacement package using PC board design rules stated in this document are:

- 0.250 mm round stencil opening in all locations except corner keep-out zones
- 0.230 mm round stencil opening in corner keep-out zones

2.8.3 Reflow profile

The infrared or convection reflow requires a Solder Joint Temperature (SJT) of 235 - 245 °C, not exceeding 245 °C, and should follow the recommendation of solder paste manufacturer including solder alloy being used. It is recommended that Package Peak Temperature (PPT) should not exceed 245 °C as higher temperatures may contribute to soldering defects. For details, see *General Soldering Temperature Process Guidelines* (document AN3300).

It is suggested to confirm SJT and PPT by populating a few target PCBs with the new package and verifying that the temperatures meet target specifications.

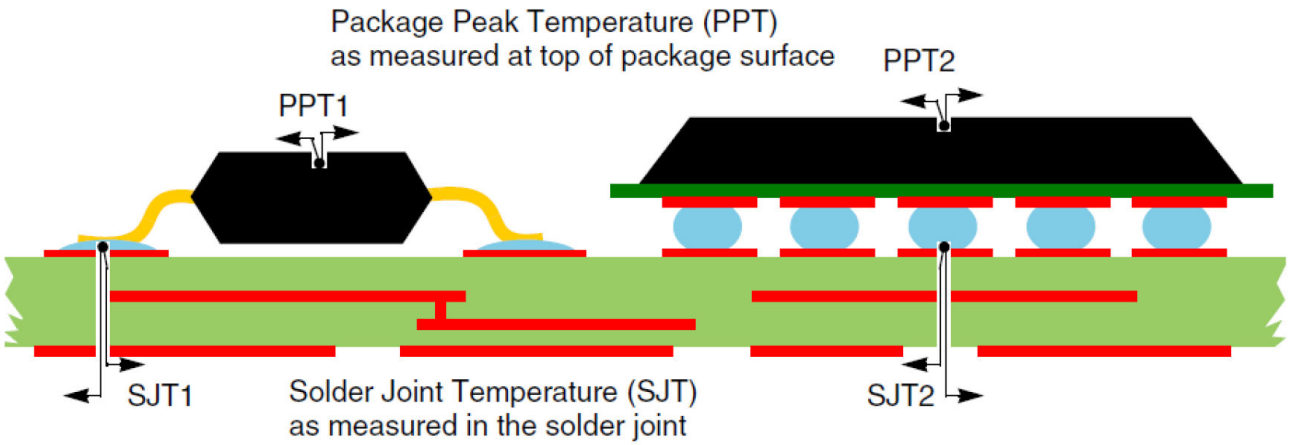


Figure 7. SJT and PPT diagram

NOTE

When doing rework to replace the new package on board, the trend is to adjust the rework station temperature lower to meet the above SJT requirement.

3 Revision history

Table 5. Revision number

Revision number	Date	Substantive changes
1	08 June 2022	Added DDR package trace delays
0	18 January 2022	Initial release

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