# AN13449

Introduction to Dual USB port on LPC5500/LPC54600 Series

Rev. 0 — 11 November 2011

Application Note

# 1 Introduction

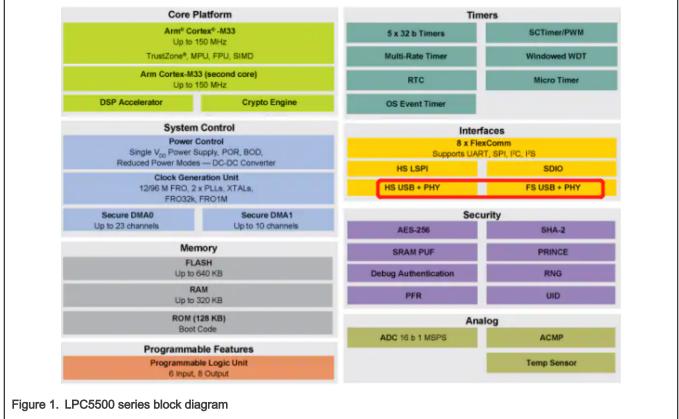
## 1.1 Dual-USB introduction

LPC4300 series, LPC54000 series, and LPC5500 series, contain the feature called dual-USB interface. The feature helps to set the LPC portfolio apart from its competitors. Most of these parts, such as, LPC5500 series, has High-Speed (HS) USB and Full-Speed (FS) USB with on-chip PHY. The dual-USB parts provide up to 480 Mbit/s throughput, which can meet high-speed data transfer requirement for any MCU application.

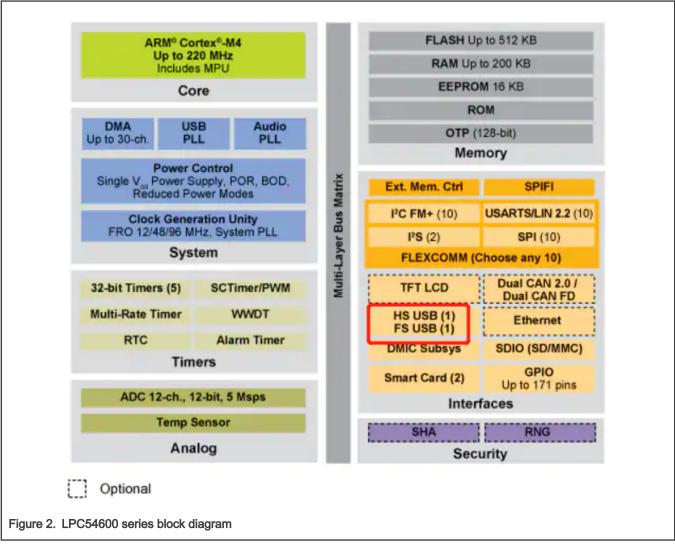
Unlike the competitors with only FS USB PHY, the dual-USB parts contain both FS and HS on-chip PHY, which can greatly reduce design complexity.

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The dual-USB interface enables numerous interesting and useful applications, as seen on LPC5500 MCU Series.

## 1.2 USB history, standard, and speed definition

USB Implementers Forum (USB-IF), a non-profit organization that maintains the USB documents and compliance programs, regulates the USB. The USB specification has undergone multiple revisions.

- 1. USB 1.0 was finalized in January 1996. The original specification only included supports for two speeds:
  - · Low-Speed (LS): Supported 1.5 Mb/s
  - Full-Speed (FS): Supported 12 Mb/s
- USB 1.1 was developed in 1998. In this revision, some clarifications and improvements were added to the USB 1.0 specification.
- USB 2.0 was released in April 2000 and the next major change occurred. In this revision, a new speed, High-Speed (HS), was added to the specification. The speed was up to 480 Mb/s. This specification revision is backward-compatible with USB 1.1 and 1.0.
- 4. USB 3.0 was announced in November 2008 and the same backward compatibility was maintained. This revision provides the speed up to 5 Gb/s. With USB 3.0 came a new physical connector as well.
- 5. More recently, USB-IF announced the plans for USB 3.1, when the speed will increase up to 10 Gb/s.

Standard	Also known as	Year introduced	Max. data transfer speed	Cable length
USB1.1	Full Speed USB	1998	12 Mbps	3 m
USB2.0	Hi-Speed USB	2000	480 Mbps	5 m
USB3.2 Gen1	USB3.0/USB3.1 SuperSpeed	SB3.0/USB3.1 SuperSpeed 2008 5 Gbps		3 m
USB3.2 Gen2	USB3.2 Gen2 USB3.1 Superspeed+		10 Gbps	3 m

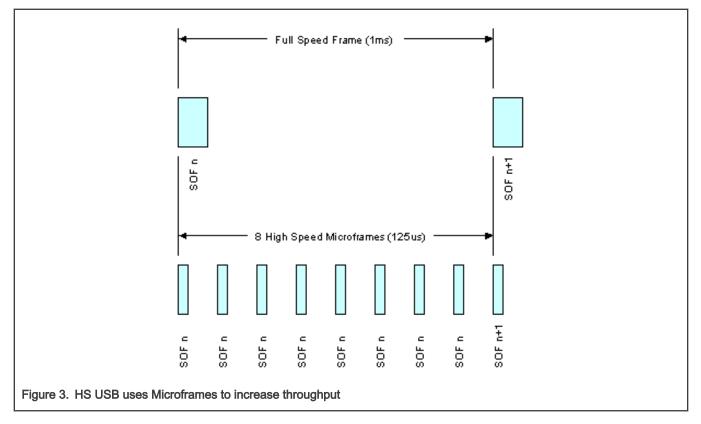
#### Table 1. USB revisions

# 2 Why high-speed USB

The performance enhancement of HS USB depends on new features on USB 2.0 standard.

## 2.1 Lower latency in interrupt transfer

1 ms frame rate, in FS/LS USB, is used for a number of purposes, such as, scheduling access to the bus and working as a timing reference for interrupt and isochronous transfers. For HS, a higher frame rate was introduced, while still maintaining a relationship with the existing 1 kHz rate. HS uses the *Microframes* which are 125 us long (eight *Microframes* per millisecond). The correspondence with the 1 ms frame numbering is maintained in the HS SOF packets by repeating each frame number in eight successive *Microframes*. HS possibly specifies up to three isochronous or interrupt transfers per *Microframes*. FS, with one transfer per frame, provides maximum isochronous or interrupt transfer rate of 192 Mb/s.



## 2.2 Larger packet length

See Table 2 for LS, FS, and HS maximum packet size.

Transfer type	Max. packet size			
	LS	FS	HS	
Control	8	8, 16, 32, 64	64	
Bulk	_	8, 16, 32, 64	512	
Interrupt	Up to 8	up to 64	Up to 1024	
Isochronous		up to 1023	up to 1024	

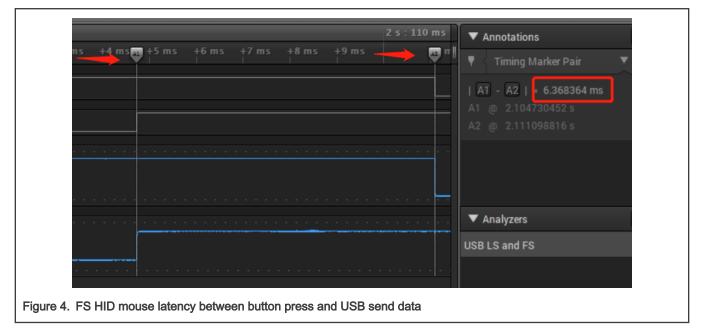
#### Table 2. Packet size

### 2.3 Example for USB HID mouse application

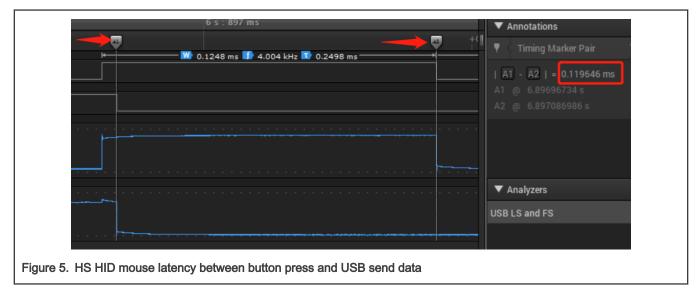
Most on-market USB mouses use 125 Hz update rate which can meet general requirements. But when entering the field of e-sport gaming mouse, 125 Hz update rate is not fast enough.

USB mouse uses USB HID class (interrupt transfer). Figure 4 shows a typical on-market FS USB mouse latency.

A1 is the time when the mouse button is pressed and A2 is the time when USB sends the HID report to PC. As seen in Figure 4, the latency can be large as 6 ms (125 Hz report rate). In worst scenario, the latency can reach 8 ms.

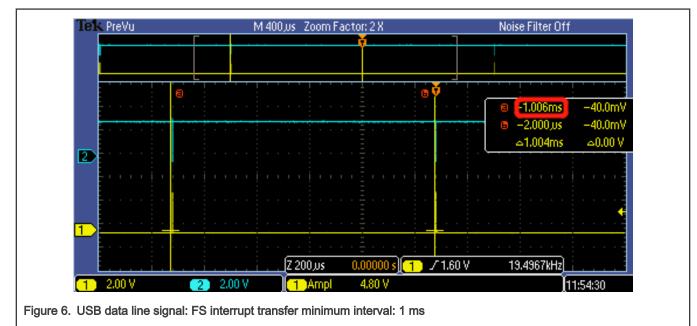


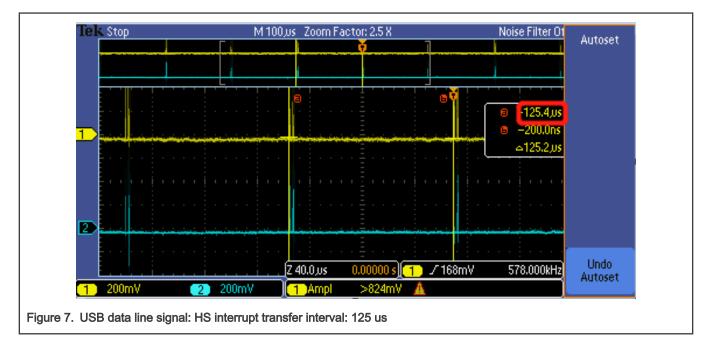
With the same test for HS USB, the report rate configures to maximum 8 kHz and the latency is 119 us. In worst scenario, the latency is only 125 us.



The interrupt transfer interval can also be seen from USB data lines signal:

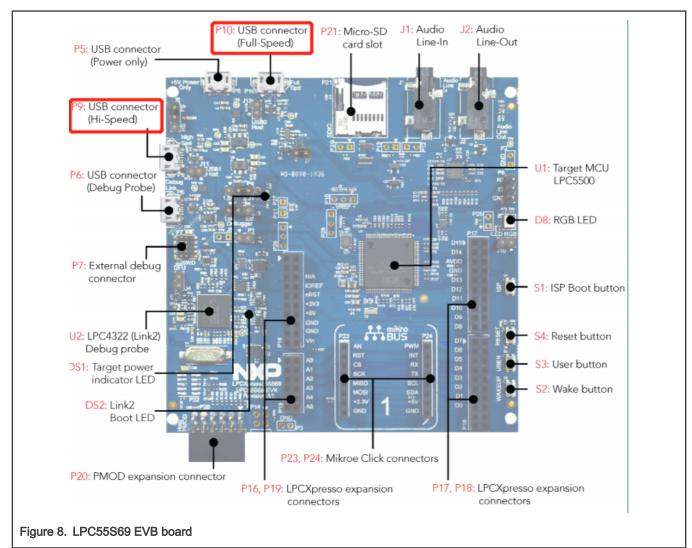
- In FS USB: the minimum interrupt transfer interval is 1 ms.
- In HS USB: the interrupt transfer minimum interval can reach 41.6 us (125/ 3 us, see Lower latency in interrupt transfer). In most use cases, 125 us interval is fast enough.





# 3 Getting started with USB demo with SDK

This section provides a hands-on guide to help you start to evaluate USB demo with SDK. Let us take the LPC55S69 as example. LPC55S69 EVB board has four USB mini connectors: P10, P5, P9, P6.



# Table 3. LPC55S69 EVB board

Circuit reference	Description		
P10	LPC55Sxx USB0 (FS) micro AB port connector		
P9	LPC55Sxx USB1 (HS) micro AB port connector		
P6	Link2 Debug Probe connector Micro USB type B connection for the on-board Link2 Debug Probe NOTE Do not use this connection when using an external Debug Probe.		
P5	External +5 V power Micro USB connection for power to the LPC55Sxx target and peripheral circuitry (excluding Link2 Debug Probe) • For USB device demo, P5 is not used. • For USB host demo, P5 must be powered.		

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For more details about this board, see Getting Started with the LPC55S69-EVK Evaluation Board.

#### 3.1 USB stack configurations

#### 3.1.1 Enable/disable dual USB ports

To switch between USB0 (FS) and USB1 (HS). Change the macro in usb device config.h.

- To enable/disable USB1, change <code>usb\_device\_config\_lpcip3511Hs</code> to 1/0.
- To enable/disable USB0, change <code>usb\_device\_config\_lpcip3511fs</code> to 1/0.

#### 3.2 Hardware connection

- For USB0 (FS) demo, connect P10 to PC.
- For USB1 (HS) demo, connect P9 to PC.
- To download and debug firmware, connect P6 to PC.
- If you have three USB cables, it is OK to connect all three USB connectors to PC.
- Suggest connecting USB port to PC USB port directly, not via USB hub.

## 3.3 USB device example

#### 3.3.1 HID mouse example

#### Demo project location:

```
\boards\lpcxpresso55s69\usb examples\usb device hid mouse
```

The HID transfer interval is controlled in the  ${\tt bInterval}$  filed in the endpoint descriptor.

For FS/LS interrupt endpoints, the value of this field may be from 1 to 255.

• Change the FS\_HID\_MOUSE\_INTERRUPT\_IN\_INTERVAL value in usb\_device\_descriptor.h.

For example:

```
#define FS_HID_MOUSE_INTERRUPT_IN_INTERVAL (0x02U)
```

Change the FS HID transfer interval to 2 ms.

For HS interrupt endpoints, the bInterval value is used as the exponent for a 2 ^(bInterval-1) value. This value must be from 1 to 16.

• Change Hs\_HID\_MOUSE\_INTERRUPT\_IN\_INTERVAL value in usb\_device\_descriptor.h.

For Example, a bInterval of 6 means a period of (2<sup>(6-1)</sup>) = 32 \*125 us = 4 ms.

#define HS HID MOUSE INTERRUPT IN INTERVAL (0x06U) /\* 2^(6-1) = 4ms \*/

Change the high-speed HID transfer interval to 4 ms.

If the bInterval value changes, the mouse movement speed changes too. Also, when using HS ports, you can configure to bInterval 1 to reach 125 us frame interval.

- For FS ports, the minimum frame interval is 1 ms.
- · For HS ports, the minimum frame interval is 125 us.

See Example on USB gaming mouse for details.

## 3.3.2 MSC example

#### Demo project location:

 $\label{linear} boards\lpcxpresso55s69\usb\_examples\usb\_device\_msc\_ramdisk$ 

#### Change the macro:

#define TOTAL\_LOGICAL\_ADDRESS\_BLOCKS\_NORMAL (360U)

Then, RAM disk size can meet the minimum requirement of PC MSC test software: CrystalDiskMark.

• FS USB: Buck transfer speed can reach 1.14 MB/s. See Figure 9 for test result.

🚼 Crysta	DiskMark 4.0.3	- 🗆	×
<u>F</u> ile <u>S</u> etti	ngs <u>T</u> heme <u>H</u> elp <u>L</u> anguage		
All	1 ∨     64 ∨     128KiB ∨       F: 1% (0/0MiB) ∨	5 🗸	
	Read [MB/s]	Write [MB/	's]
Seq Q32T1	1.140	1.14	0
4K Q32T1	0.000	0.00	0
Seq	0.000	0.00	0
4K	0.000	0.00	0
Figure 9. FS USB RAM disk test	speed		

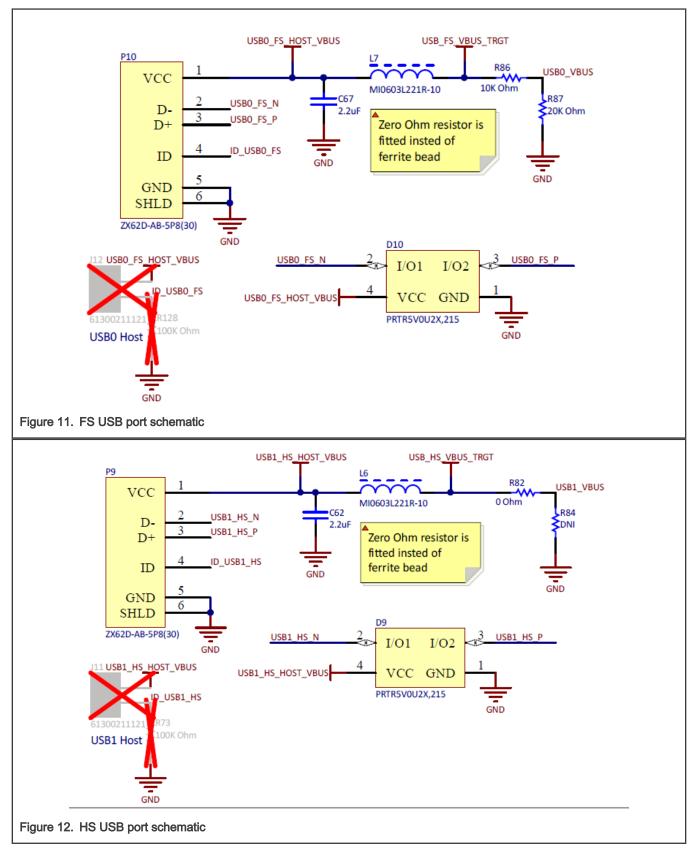
• HS USB: Buck transfer speed can reach 24 MB/s. See Figure 10 for test result.

KrystalDiskMark 4.0.3	_		×
<u>File S</u> ettings <u>T</u> heme <u>H</u> elp <u>L</u> anguage			
1 ∨ 64 ∨ 128KiB ∨           F: 1% (0/0MiB) ∨	5 🗸		
Read [MB/s]	Write	[MB/	's]
Seq 24.11	21	.5	3
4K Q32T1 <b>0.000</b>	0.0	00	0
Seq 0.000	0.0	00	0
<sup>4K</sup> <b>0.000</b>	0.0	00	0
Figure 10. HS USB RAM disk test speed			

For details, see Example for USB HID mouse application.

# 4 Hardware design

Both FS and HS USB ports contain on-chip PHY to make the schematic design much simpler. Figure 11 and Figure 12 are the schematic reference for FS and HS ports.



For USB clock source:

• FS USB ports for device operation. The external crystal is optional since FS USB device support crystal less operation.

• When using FS USB host, HS USB host/device, external crystal must be connected.

For PCB layout:

- · Avoid creating slots, voids, and splits in the reference planes.
- Provide ground return vias within a 100 mil from the signal layer-transition vias when transitioning between different reference ground planes.

To improve EMC performance:

- Recommend using TVS arrays for ESD protection on VBUS, D+, D-, and ID.
- · Connect the common mode choke to USB signal.
- To isolate high frequency noise, use Ferrite beads on power pin (VBUS, GND).

For more details about hardware design guideline, see *Hardware Design Guidelines for LPC55(S)xx Microcontrollers* (document AN13033).

# 5 Summary

This application notes discuss the following topics:

- 1. Dual USB feature introduction in LPC54600 and LPC5500 series.
- 2. Comparison between HS and FS USB and the advantage for using HS USB.
- 3. Hands-on guide to explore USB feature using MCUXpresso SDK (LPC5500 series).
- 4. USB hardware design tips for LPC54000 and LPC5500 series.

## 6 Reference

- 1. LPC55S69-EVK: LPCXpresso55S69 Development Board
- 2. USB Descriptors
- 3. Frames and Microframes
- 4. LPC5500 MCU Series
- 5. USB Document Library
- 6. Guidelines for full-speed USB on NXP's LPC microcontrollers (document AN11392)
- 7. Hardware Design Guidelines for LPC55(S)xx Microcontrollers (document AN13033)

# 7 Revision history

	Rev.	Date	Description	
ſ	0	11 November 2021	Initial release	

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