# AN13537

## Power management solution for Horizon Journey 3

Rev. 1.1 — 4 August 2023 Application note

**Document information**

| Information | Content |
|---|---|
| Keywords | power tree solution, Horizon Journey 3, BYLink system power, functional safety, PMICs attachment |
| Abstract | The Horizon Journey 3 processor is used widely in autonomous driving systems. NXP PF8x00 + PF5024 is an appropriate power solution for use with this processor. This Application Note introduces one NXP BYLink PMIC solution for Journey 3. It introduces solutions for a power tree, power sequence and various power modes, as well as support for functional safety features. This document also supplies the part number of the PMIC used in the Horizon reference design. |

# 1 Introduction

NXP 3rd Generation Functional safety power management ICs (PMICs) are widely used in automotive applications, especially advanced driver assist systems (ADAS), infotainment, connective, domain controller and other complex systems. In these applications, NXP PMICs can be used to supply NXP processors or non-NXP processors and peripheral devices.

Horizon Journey Family processors are popular in artificial intelligence (AI) field applications. They are increasingly chosen by car OEMs and tier 1 automotive suppliers as the main processors in L2-L4 Autonomous Driving Systems, to achieve high computing capability and Edge Detection functionality.

NXP PF8x00 + PF5024 or PF5200 PMICs are appropriate matches for the power requirements of the Journey 3 (J3) System on Chip (SoC). Due to NXP's cooperation with Horizon, NXP PMICs are used in Horizon's J3 reference design and system on module (SoM) boards. NXP defined dedicated One Time Programmable (OTP) PMIC versions for the J3 processor, which customers can order directly.

NXP's BYLInk System Power Platform is a simple and effective way to enable complex applications. It helps customers develop scalable and safe power solutions using the Horizon J3 System on Chip.

# 2 Horizon J3 and NXP PMIC Overview

Because of its strong computing capability and small power consumption, J3 is a popular choice for ADAS and Domain Controller systems.

NXP provides the BYLink System Power platform, which includes high voltage and low voltage PMICs. NXP's PF8x00 and PF502x family devices are high integration PMICs designed for high performance processor-based systems. These PMICs all belong to the low voltage category of the NXP BYLink Power Concept. All PF PMICs have similar structures, and are designed to work together. When connected appropriately, PF8x00 and PF502x can be used together as one PMIC to supply J3 SoC system.

PF8x00 PMICs include seven high efficiency bucks and four LDOs for powering the processor, memory and miscellaneous peripherals. Each buck has a 2.5 A stable current capability, and can work in multi-phase mode to supply up to 10 A of current. Each LDO can output 400 mA of current.

The PF5024 integrates four bucks, each of which can generate a 2.5 A current. A multi-phase arrangement of PF5024 bucks can supply a load up to 10 A.

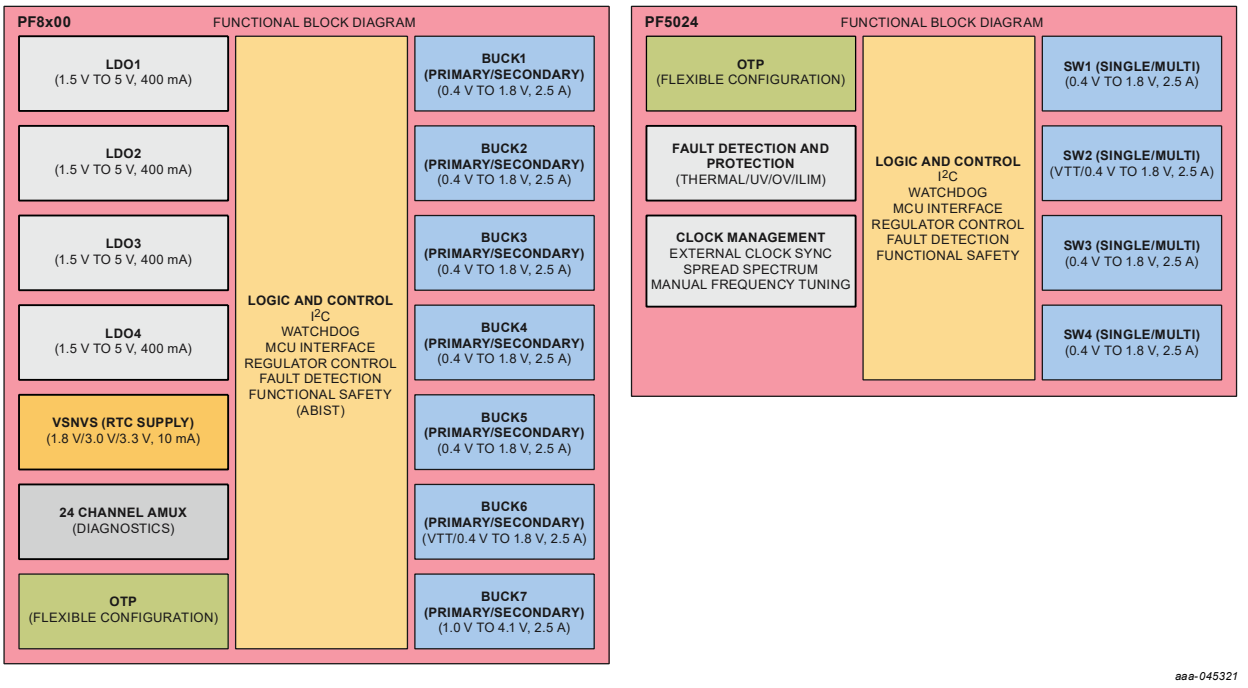


**Figure 1. PF8x00 family and PF5024 device functional block diagrams**

PF8x00 and PF5024 family devices allow scalability in functional safety designs. PF8200 and the ASIL-B version of PF5024 can be used together to support an ASIL-B target system.

For systems with no functional safety requirements, the PF8100 can be used with the PF5024 QM version device. The functional safety features of PF-PMICs for ASIL-B systems are achieved by hardware mechanisms within the chips.

These two solutions (PF8200 + ASIL-B PF5024 and PF8100 + QM PF5024) are hardware and software compatible.

In automotive (car, bus, and truck) applications, the 12 V or 24 V battery voltages are regulated into multiple supply rails to satisfy the power requirements of the system.

PMICs in the high voltage category of NXP's BYLink System Power platform can also be useful in customer systems.The FS56 or FS85 are appropriate as front power devices for a J3 system. NXP provides a complete portfolio of safety PMICs with embedded system features. See Figure 2 for block diagrams of FS56 and FS85 family devices.

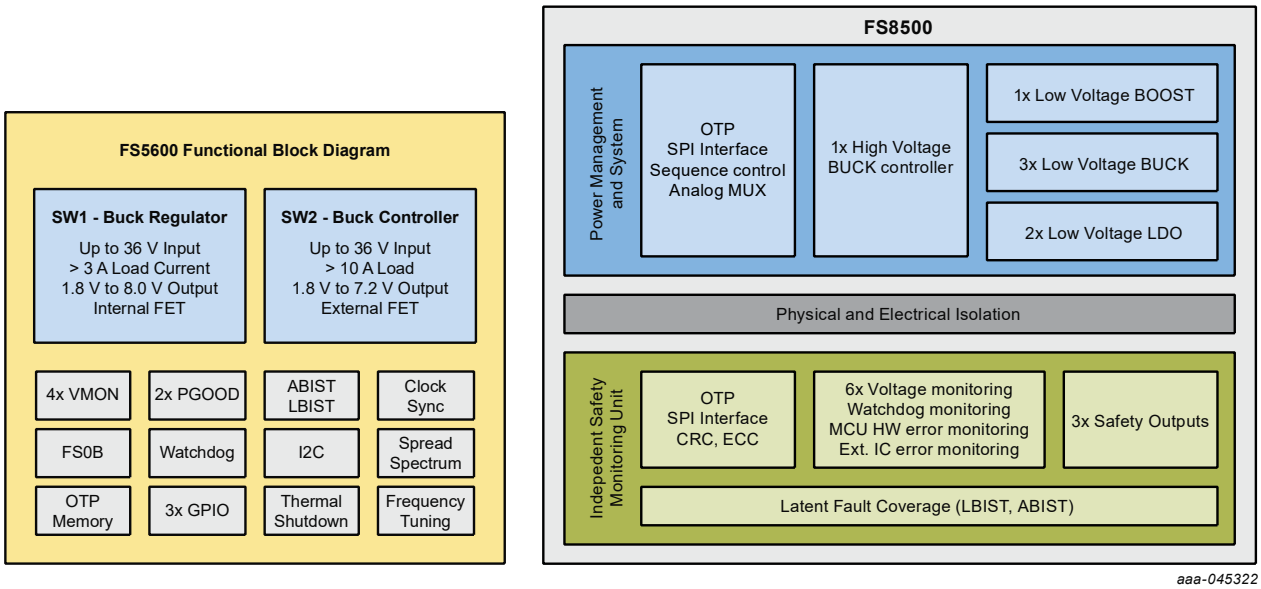


**Figure 2. FS56 and FS85 Family Device Function Block Diagram**

# 3 J3 power solution introduction

## 3.1 Power tree for J3 system

The Horizon reference design board uses a PF8x00 + PF5024 solution to supply a J3 system. If a customer is developing an ASIL-B system, an ASIL-B version of PF5024 should be used with the PF8200. For systems that do not require functional safety, a QM version of PF5024 with PF8100 can be used as one pin-to-pin compatible solution. The power tree for the PF8x00 + PF5024 solution is illustrated in Figure 3.

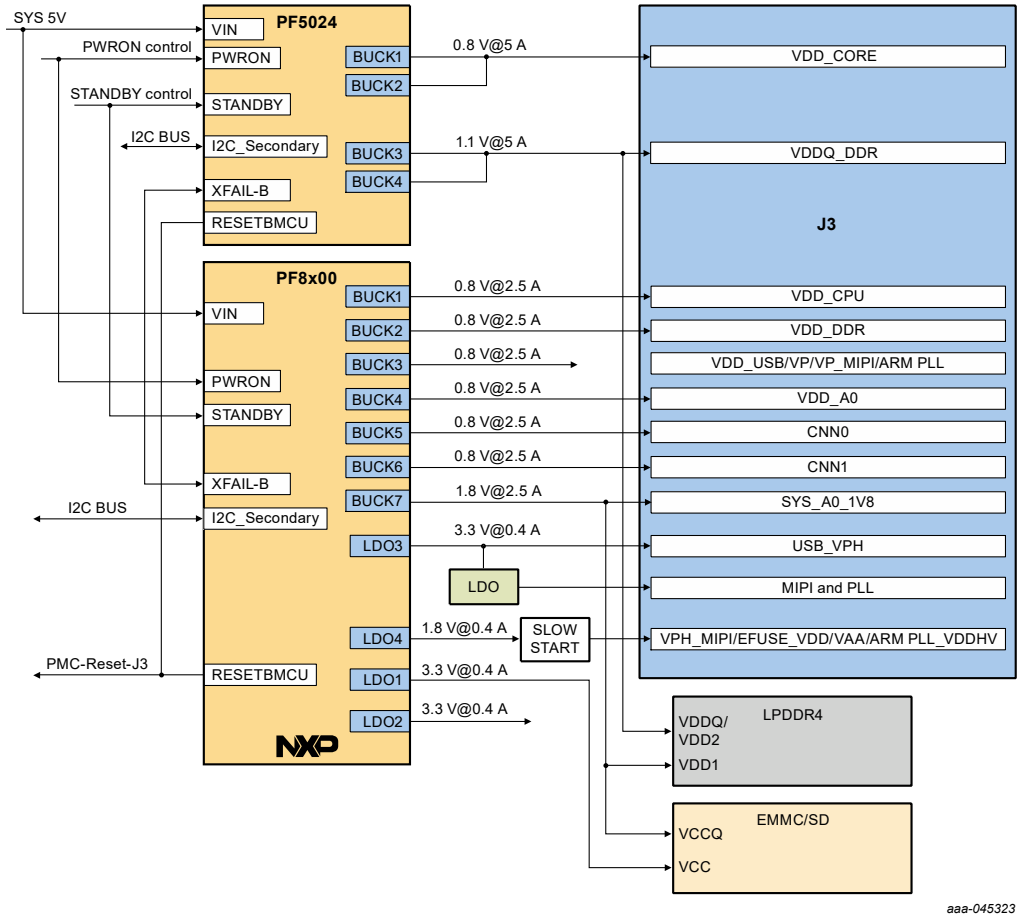


**Figure 3. PF8x00 + PF5024 power solution for J3**

In this solution, the input voltage for the PMICs is SYS_5V.

PWRON of the PF-PMIC can be controlled by the system's MCU. If the input voltage is ready, the power system will start up when PWRON is pulled high. The power rails of PF-PMICs will follow the power up sequence as defined by OTP. RESETBMCU, which is connected with the J3 system Reset, will be released at the end of the power sequence if all the power rails of PMIC turn on with no fault. Then, the J3 system will continue to operate other boot up actions. The power system has been verified and can support J3 normal mode and DDR refresh mode.

For the power tree, customers can order the production OTP part directly. For the QM version, the part numbers are *SC33PF8100JCES* and *SPF5024CMMAWES*. If a customer is using ASIL-B versions, the part numbers should be *SC33PF8200JGES* and *SPF5024CMBAYES*. The OTP version is defined by Horizon and NXP, and the OTP configuration report is available to customers who use the NXP power solution.

See Table 1 for the design parameters of the PF8x00 + PF5024 J3 solution:

**Table 1. Design parameters for PF8200 + PF5024 J3 solution**

| J3 system power rails | Voltage (V) | PMIC source | Current capability (A) | Power up group | Power down group |
|---|---|---|---|---|---|
| VDD_CORE | 0.8 | BUCK1 and BUCK2 of PF5024 | 5 | 3 | 3 |
| VDDQ_DDR | 1.1 | BUCK3 and BUCK4 of PF5024 | 5 | 1 | 1 |
| VDDQ/DD2 of **LPDDR4** | 1.1 | | | | |
| VDD_CPU | 0.8 | BUCK1 of PF8x00 | 2.5 | 3 | 3 |
| VDD_DDR | 0.8 | BUCK2 of PF8x00 | 2.5 | 3 | 3 |
| VDD_USB/VP_MINI | 0.8 | External LDO | 0.4 | 4 | 4 |
| VP/ARM PLL_VDDREF/ ARM PLL_VDDPST | 0.8 | | | | |
| VDD_AO | 0.8 | BUCK4 of PF8x00 | 2.5 | 2 | 2 |
| VDD_CNN0 | 0.8 | BUCK5 of PF8x00 | 2.5 | 3 | 3 |
| VDD_CNN1 | 0.8 | BUCK6 of PF8x00 | 2.5 | 3 | 3 |
| SD_VDDPST33/SYS_ VDDPST/I2C_VDDPST SYS_AO_1V8 | 1.8 | BUCK7 of PF8x00 | 2.5 | 1 | 1 |
| VDD1 of **LPDDR4** | 1.8 | | | | |
| VCCQ of **EMMC** | 1.8 | | | | |
| VCC of **EMMC** | 3.3 | LDO1 of PF8x00 | 0.4 | 1 | 1 |
| USB_VPH | 3.3 | LDO3 of PF8x00 | 0.4 | 4 | 4 |
| PVT_VDDA/ARM PLL_ VDDHV/VAA/EFUSE_ VDD/VPH_MIPI | 1.8 | LDO4 of PF8x00 | 0.4 | 4 | 4 |
| VCC_3V3 | 3.3 | LDO2 of PF8x00 | 0.4 | 1 | 1 |

## 3.2 Power-up and power-down sequence of the J3 system

The J3 processor has a strict power-up and power-down sequence. NXP and Horizon have defined the dedicated OTP version that can achieve the J3's required power sequence. Additional design on the hardware or software is unnecessary. The power-up and power-down sequence will happen automatically if the correct versions of OTP devices are used.

PF8x00 and PF5024 both belong to the set of BYLink Power platform low voltage PMICs, and can be used together to work as one PMIC. To do this, the XFAIL-B pins of the two devices must be connected together. The XFAIL-B pin can sync the power-up and power-down sequences. See Figure 4 for a description of the power-up and power-down sequence of the J3 system.

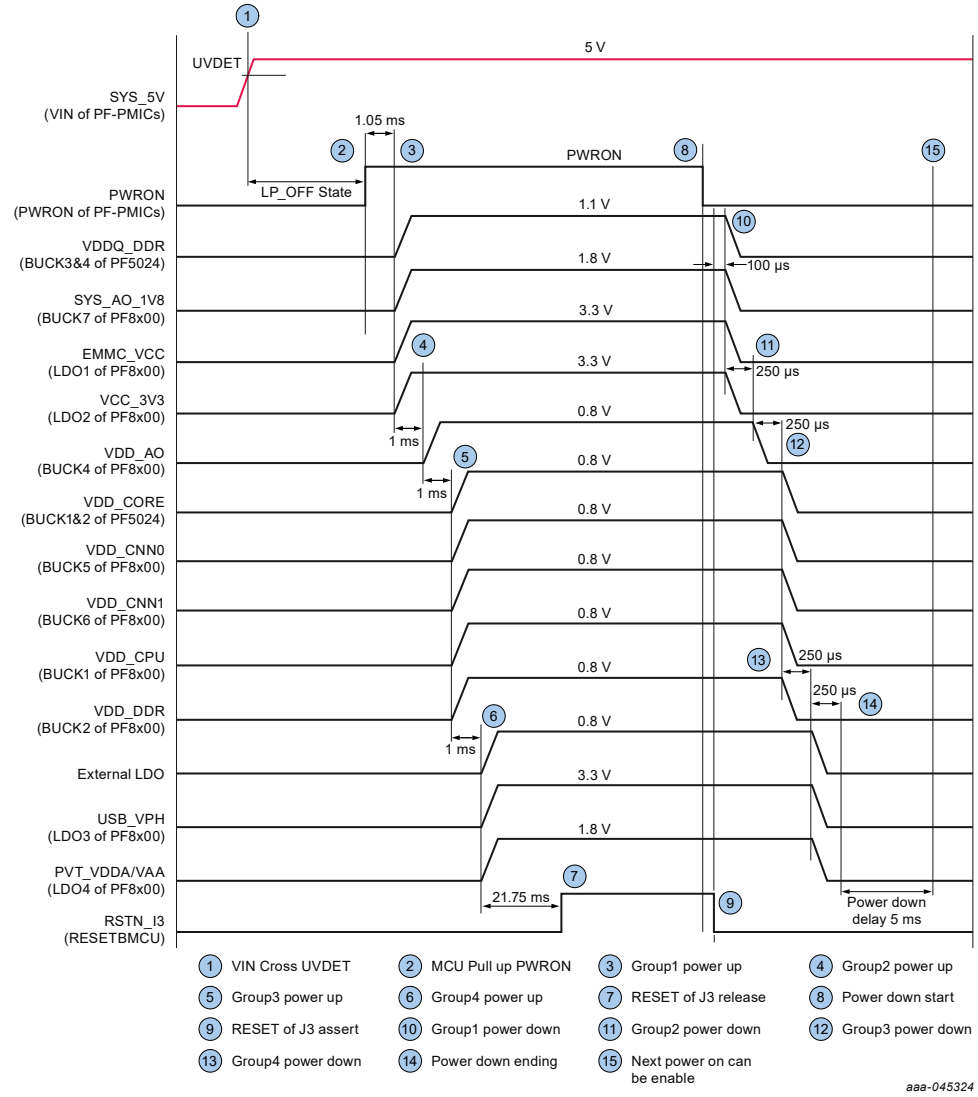


**Figure 4. J3 Power up and down sequence of PF8x00 + PF5024 solution**

In the solution, the power up and down action is controlled by PWRON, and there are four groups of power rails for the J3 system.

The RESETBMCU signal of the PF-PMICs is released at the end of the power-up sequence, and asserted first when power-down is triggered by the PWRON pin. The power-down sequence is not mirrored to power-up. At the end of the power-down sequence, there is a 5 ms power-down delay. During this period, PWRON is masked, and no new power-up activities are allowed for the PMICs.

## 3.3 DDR refresh mode of the J3 system

In the J3 SoC DDR refresh mode, most of the power rails are in off status, with only a few rails powered on. The PF8x00 + PF5024 power solution can achieve this state easily using the PF-PMICs' standby operation functionality.

**Table 2. J3 SoC DDR refresh mode power rails status**

| J3 system power rails | Voltage (V) | PMIC source | Status in DDR refresh mode | I2C configuration after PMIC on |
|---|---|---|---|---|
| VDD_CORE | 0.8 | BUCK1 and BUCK2 of PF5024 | OFF | SW1_STBY_MODE=**00** (PF5024) |
| VDDQ_DDR | 1.1 | BUCK3and BUCK4 of PF5024 | **ON** | — |
| VDDQ/DD2 of **LPDDR4** | 1.1 | | | |
| VDD_CPU | 0.8 | BUCK1 of PF8x00 | OFF | SW1_STBY_MODE=**00** (PF8x00) |
| VDD_DDR | 0.8 | BUCK2 of PF8x00 | OFF | SW2_STBY_MODE=**00** (PF8x00) |
| VDD_USB/VP_MINI | 0.8 | EXTERNAL LDO | OFF | LDO3_STBY_EN=**0** (PF8x00) |
| VP/ARM PLL_VDDREF/ARM PLL_VDDPST | 0.8 | | | |
| VDD_AO | 0.8 | BUCK4 of PF8x00 | **ON** | — |
| VDD_CNN0 | 0.8 | BUCK5 of PF8x00 | OFF | SW5_STBY_MODE=**00** (PF8x00) |
| VDD_CNN1 | 0.8 | BUCK6 of PF8x00 | OFF | SW6_STBY_MODE=**00** (PF8x00) |
| SD_VDDPST33/SYS_ VDDPST/I2C_VDDPST SYS_AO_1V8 | 1.8 | BUCK7 of PF8x00 | **ON** | — |
| VDD1 of **LPDDR4** | 1.8 | | | |
| VCCQ of **EMMC** | 1.8 | | | |
| VCC of **EMMC** | 3.3 | LDO1 of PF8x00 | **ON** | — |
| USB_VPH | 3.3 | LDO3 of PF8x00 | OFF | LDO3_STBY_EN=**0** (PF8x00) |
| PVT_VDDA/ARM PLL_ VDDHV/VAA/EFUSE_VDD/ VPH_MIPI | 1.8 | LDO4 of PF8x00 | OFF | LDO4_STBY_EN=**0** (PF8x00) |
| VCC_3V3 | 3.3 | LDO2 of PF8x00 | **ON** | — |

Table 2 shows the status of power rails in J3 DDR refresh mode.

PF-PMICs work in Normal mode to support J3 normal operation. In Normal mode, the power rails' output voltage will be according to the OTP definition. If a system needs to enter DDR refresh mode, there must be an MCU that can control the PF-PMICs' STANDBY pin. The STANDBY pin is active high by OTP configuration, and the customer should pull STANDBY down to GND on their board to make PMICs work in Normal mode by default. When the system needs to enter DDR refresh mode, the customer should pull STANDBY up through the MCU.

The output voltage and status in Standby mode for the PF-PMICs are defined by a functional register through I2C. The default voltage for all the power rails in Standby mode is the same as in Normal mode. This means the PMIC output will stay the same if there is no I2C configuration after the PMIC starts up, even if the PF-PMICs enter Standby mode. The I2C configuration after PMIC startup will be set in the I2C functional register, directing PMICs to enter Standby mode to support J3 operation in DDR refresh mode. See Table 2 for the I2C configuration that needs to be sent to the PMICs. Note that the I2C addresses of PF8x00 and PF5024 are different. For more details about software development, contact NXP or Horizon.

When PF-PMICs enter or exit Standby mode, the power sequence will follow the power-down and power-up sequence, except for the rails that stay on in DDR refresh mode. RESETBMCU will be deasserted, whether the mode is Standby or Normal.

## 3.4 Additional hardware design guidelines

J3 has special power soft start requirements for some power rails. The PF8x00 + PF5024 power solution can fulfill these requirements.

The typical soft start slew rate output of PF5024 is 3.91 mV/µs, which is in the limitation range for the aggressive J3 request of 5 mV/µs for some dedicated power rails. Because the LDO4 output supplying J3 has a default slew rate faster than 5 mV/µs, NXP recommends using the slow start circuit illustrated in Figure 5 to achieve the J3 requirement.

Contact Horizon for more detailed information and support with MOS selection.

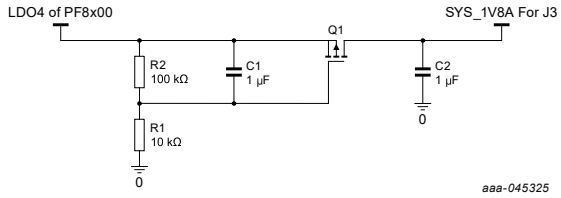


**Figure 5. Slow start circuit**

Because the MIPI and PLL need a power supply with no ripple, one external LDO is needed to supply the power rails. The customer should contact Horizon for details. BUCK3 is not used in the power tree, but the 0.8 V power is enabled, so the customer must keep the external inductor and capacitors in place.

For the VDD_CORE power rails, NXP recommends adding 2 * 100 µF to the BUCK1 and BUCK2 dual-phase output from PF5024.

## 3.5 Replacing PF5024 with PF5200

The typical load of VDD_CORE of J3 is supplied by PF5024 SW1 and SW2 operating in dual phase. In the worst use case, VDD_CORE of J3 requests a higher current capability. This worst-case scenario may happen with ISP with 2*VPU plus JPG_ENC working together, with 125 degree ambient temperature. For a customer with this aggressive use case, NXP recommends replacing PF5024 with PF5200.

The PF5200 family also belongs to the BYLink power platform, and its logical structure is nearly the same as the PF5024. PF5200 integrates two low voltage bucks, each with an 8 A current capability. SW1 can be used to supply VDD_CORE of J3 and SW2 can be used to supply VDDQ_DDR of J3 and LPDDR4. The power tree can be adjusted as in Figure 6.

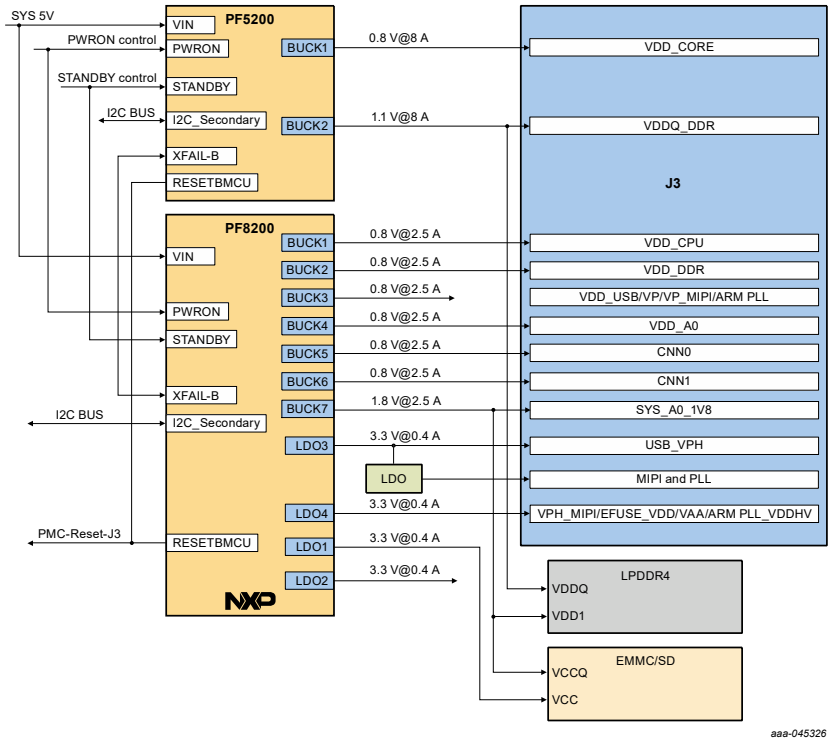


**Figure 6. Power tree using PF5200 instead of PF5024**

See Figure 7 for the structure of PF5200. The PF5200 family has QM and ASIL-B versions. Its package is 5 mm * 5 mm FC-QFN, which is smaller than PF5024. Its performance efficiency is also better than PF5024. If a customer uses PF5200 to replace PF5024, the customized OTP version can be obtained by contacting NXP.

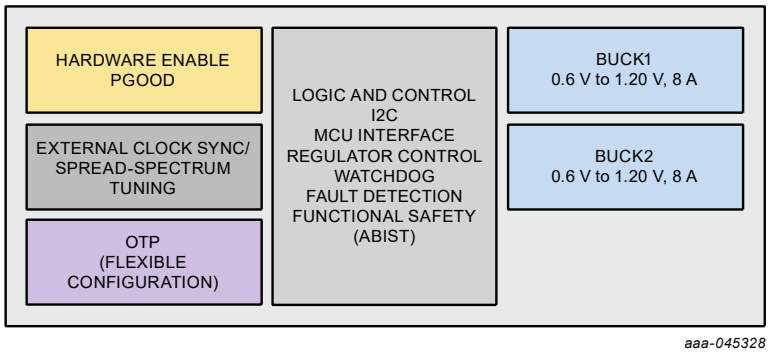


**Figure 7. PF5200 block diagram**

# 4 SoM board power solution for Horizon J3

Horizon developed its own SoM board that uses one NXP PF5024 and three other power devices from another company. See Figure 8 for the power structure. Consult Horizon for a detailed power tree. For this solution, the OTP version has been defined using the part number ***SPF5024CMMAMES***. Customers can order this part directly. This four-chip solution cannot support functional safety requirements, because the PMICs chosen for the Horizon SoM board have no safety features. If functional safety is a design requirement, the power design must migrate to PF8200 + PF5024.

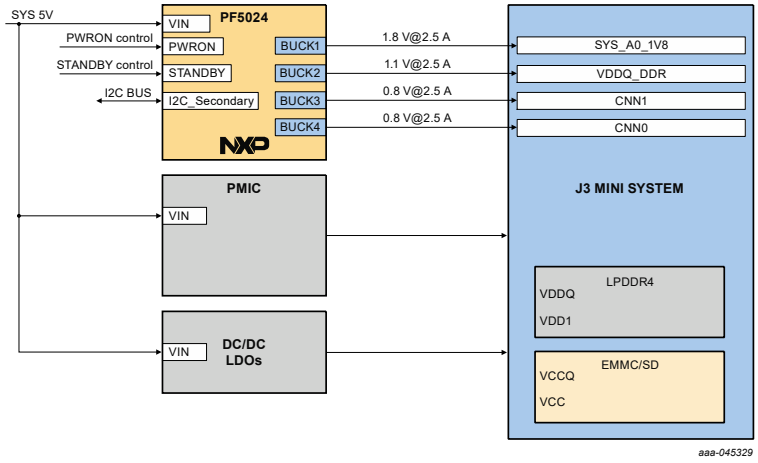


**Figure 8. Horizon J3 SoM board power solution**

# 5 NXP BYLink system power platform for J3

BYLink is a simple and effective way to enable complex applications, such as ADAS and zone controllers. This new power supply concept simplifies the board design, providing power management building blocks and design flexibility, and helping customers achieve a complete automotive system power solution. For more details about the BYLink System Power Platform, visit NXP's official website.

In car and truck systems, the 12 V and 24 V supplies from the battery are regulated and generated into multiple supply rails to satisfy the system power demands. NXP provides a complete portfolio of safety PMICs with embedded system features. They are classified in two main categories: high voltage PMICs and low voltage PMICs. The PF8x00 + PF5024 or PF5200 power solutions for the J3 system that were mentioned earlier belong to the low voltage subset of BYLink PMICs.

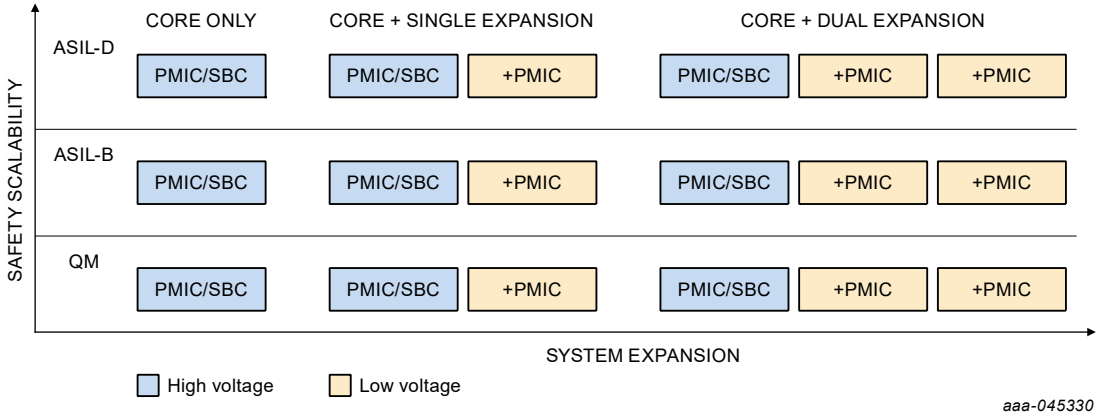


**Figure 9. Safety scalability vs. system expansion**

FS56 and FS85, each of which can be used to connect to a battery input as a high voltage PMIC, are suitable for use in a J3 system for 12 V or 24 V automotive applications. To implement the BYLink system power platform for J3, FS56 or FS85 can be chosen as the front-end power device to generate voltage for low voltage PMICs.

The FS56 can provide input to PF-PMICs and power to other peripherals. Its current capability at SW2 can be 15 A, with a 1.8 V-7.2 V voltage range. SW1 can provide 1.8 V-8.0 V/3 A high efficiency power for an MCU and other peripherals. EN1 and EN2 of the FS56 can be connected to an ignition signal or a CAN Phy wakeup signal. Figure 10 illustrates one real use case for a J3 12 V system.

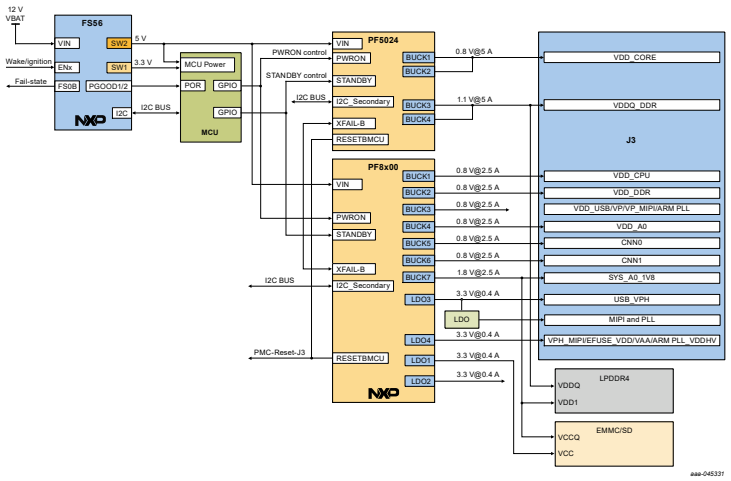


**Figure 10. FS56 + PF8x00 + PF5024 board solution for J3**

For a 24 V and 12 V battery compatible system, FS85 family devices can be used to replace FS56 to work with PF-PMICs. Also, because FS85 is suitable for ASIL-D and ASIL-B systems, it can be integrated closely with an ASIL-D MCU to achieve the ASIL-D target at the system level.

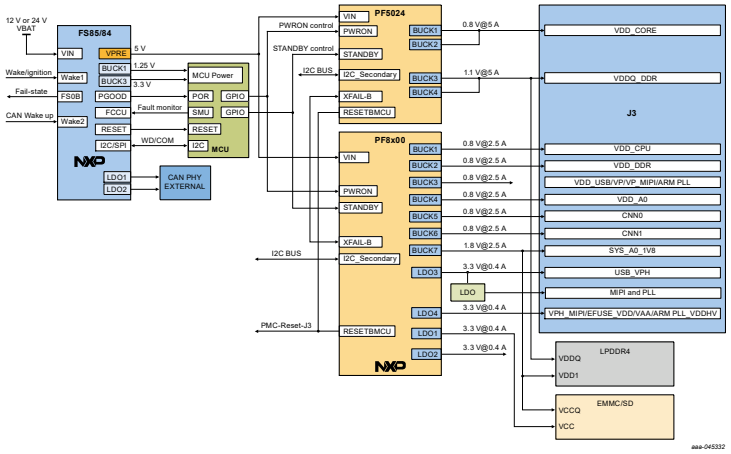


**Figure 11. FS85/84 + PF8200 board solution for J2**

If a customer is using several J3 SoCs in their system, they can choose FS85 + FS56 to support the system. High-voltage PMICs from NXP can work with low-voltage PMICs in synchronization to provide a total solution. Customers can also provide power requirements to NXP, and NXP will support a customized power tree for a dedicated system.

# 6 Functional safety design

## 6.1 3rd generation functional safety PMICs

BYLink System power PMICs are NXP 3rd Generation Functional safety PMICs. The lifecycle of these products follow ISO 26262, and the devices are developed as safety elements out of context (SEooC).

All PMICs in the functional safety system have their own real time OV/UV monitors. When an OV/UV fault is detected, the system can notify the processor or cause entry into a safe state within the Fault Tolerant Time Interval (FTTI).

For ASIL-D power rails requirements, the Single Point Fault Metric must be above 99%. This metric should be above 97% for ASIL-B power rails.The PMICs also have BIST circuits and redundancy design paths, helping the Latent Fault Metric of Powers reach 90% for ASIL-D and 60% for ASIL-B. The Probabilistic Metric for random Hardware Failures (PMHF) of all the power devices is very small, which can provide a buffer for system PMHF.

In additional to safety power, the PMICs provide Watchdog and hardware monitor functionality to monitor the processor and MCU. The PMICs also provide safety outputs at the system level to allow entry into a safe state when a failure occurs, helping to ensure that the desired safety goal is met. Contact NXP to obtain safety manuals and details for applying failure modes, effects and diagnostic analysis (FMEDA).

## 6.2 Functional safety power structure for J3 system

For the ADAS For the ADAS Domain Controller hardware design, the Perception Domain must achieve the ASIL-B functional safety level, and the Control and Decision Domain must achieve ASIL-D. NXP's BYLink system power platform can easily achieve the board level power functional safety requirements to support these requirements for ASIL-D and ASIL-B. Figure 12 shows one real use case for a J3 functional safety system.

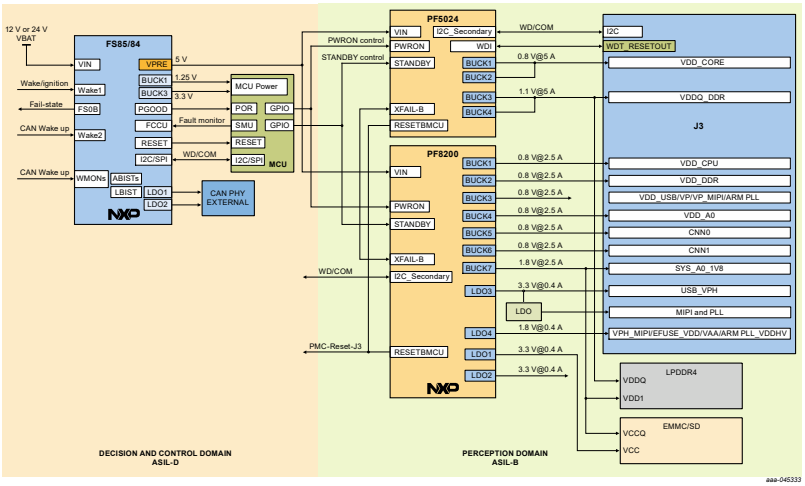


**Figure 12. Functional safety power solution for J3 system**

In this solution, FS85 is used as the Front power device to support an ASIL-D MCU in the Control and Decision Domain. PF8200 + PF5024 support the J3 system to achieve an ASIL-B Perception Domain. In the system level functional safety design, the power solution not only provides the safety power rails for the processors and peripherals, It also provides a safety mechanism for the system functional safety development, in order to request system degradation in case of a fault in the Fault Tolerant Time Interval.

FS85 can be used to attach an ASIL-D MCU and provide ASIL-D Watchdog and Hardware monitoring for the MCU. When a fault or stuck event occurs in the MCU, the FS0B and RESET of FS85 will work according to pre-definition to make the system enter a safe sate. PF8200 and PF5024 work with J3, and J3 can feed the WD in PF5024 or PF8200 through I2C when there is a stuck condition or failure in J3. The PMICs will be reset, in order to reset the J3 system.

As a redundancy measure, there is also one PMIC hardware monitor for J3: WDT_RESETOUT of J3 is connected with WDI on the PMIC. WDI will be asserted when there is a J3 fault, generating a PMIC power down and power up, resetting the J3 system.

### 6.3 Functional safety software development

Because the functional safety mechanisms of NXP PMICs are achieved through hardware operations, there is little need for new development of accompanying functional safety software. NXP does provide safety SDK API code in C languages that customers can download from the NXP website.

NXP is working closely with Horizon to develop functional safety systems. ASIL-B versions of OTP PMICs have been defined, and customers can obtain them directly from NXP. PMIC functional safety drivers will be integrated in J3 code in the future.

## 7 Reference resources

As a result of NXP's cooperation with Horizon, there are defined OTP versions of PF8x00 and PF5024 that work with J3. These devices can be ordered directly from the customer site. Each customer can define their schematic using an existing OTP version. The mass production OTP version for J3 can be found in Table 3. Contact NXP or Horizon for more details about these versions.

**Table 3. Defined PF8x00 OTP version for J3**

| Part Number | Solution | DDR | Comments |
|---|---|---|---|
| SC33PF8100**JC**ES and SPF5024CMM**AW**ES | J3 Reference design | LPDDR4 | QM Version |
| SC33PF8200**JG**ES and SPF5024CM**BAY**ES | — | LPDDR4 | ASIL-B Version |

Design artifacts such as schematics and layout can be obtained from NXP and Horizon, and other tools and information are available at NXP's website.

PF8x00 information and tools can be found at the link: https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/12-channel-power-management-integrated-circuit-pmic-for-high-performance-processing-applications:PF8100-PF8200

PF5024 information and tools can be found at the link: https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/multi-channel-4-pmic-for-automotive-applications-4-high-power-fit-for-asil-b-safety-level:PF5024

PF5200 information can be found at the link: https://www.nxp.com/products/power-management/pmics-and-sbcs/pmics/dual-channel-pmic-for-automotive-applications-2-high-efficient-lvbuck-fit-for-asil-b-safety-level:PF5200

FS56 information can be found at the link: https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/automotive-dual-buck-regulator-and-controller-with-voltage-monitors-and-watchdog-timer:FS5600

FS85 information can be found at the link: https://www.nxp.com/products/power-management/pmics-and-sbcs/safety-sbcs/safety-system-basis-chip-for-s32-microcontrollers-fit-for-asil-d:FS8500

## 8 Revision history

**Table 4. Revision history**

| Rev | Date | Description |
|---|---|---|
| 1.1 | 20230804 | • Figure 3, Figure 4, Figure 6, Figure 10, Figure 11: 1.8 V/3.3 V changed to 3.3 V for LDO2<br>• Figure 12: 1.8 V/3.3 V changed to 3.3 V for LDO2; 3.3 V@0.4 A changed to 1.8 V@0.4A for LDO4<br>• Global change: '3V3 of External Devices' and 'External 1V8/3V3' changed to 'VCC_3V3' for LDO2 |
| 1 | 20220806 | Initial release. |

# 9 Legal information

## 9.1 Definitions

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## Tables



## Figures

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