AN13543

Programming and Booting Images from External NOR FLASH on LPC553x/LPC55S3x

Rev. 1 — 25 May 2022 Application Note

Contents

1 Introduction

1.1 Overview

LPC553x/LPC55S3x is an Arm Cortex-M33-based microcontroller for embedded applications. This document describes how to program and boot image from external NOR FLASH device.

LPC553x/LPC55S3x supports both on-chip FLASH image boot and an external NOR FLASH image boot. To erase/program/read the on-chip or external FLASH, use ROM to download the boot image into the on-chip and external FLASH via the ISP interfaces. ROM also takes responsibility for the boot flow. It decides to boot from on-chip FLASH, external FLASH, or ISP mode.

CMPA/CFPA contains boot-related parameters. To update the setting, use ROM in ISP mode or ROM API in application.

1.2 Memory layout

Figure 1 shows the LPC553x memory layout. For details, see the attachment file in LPC553x UM.

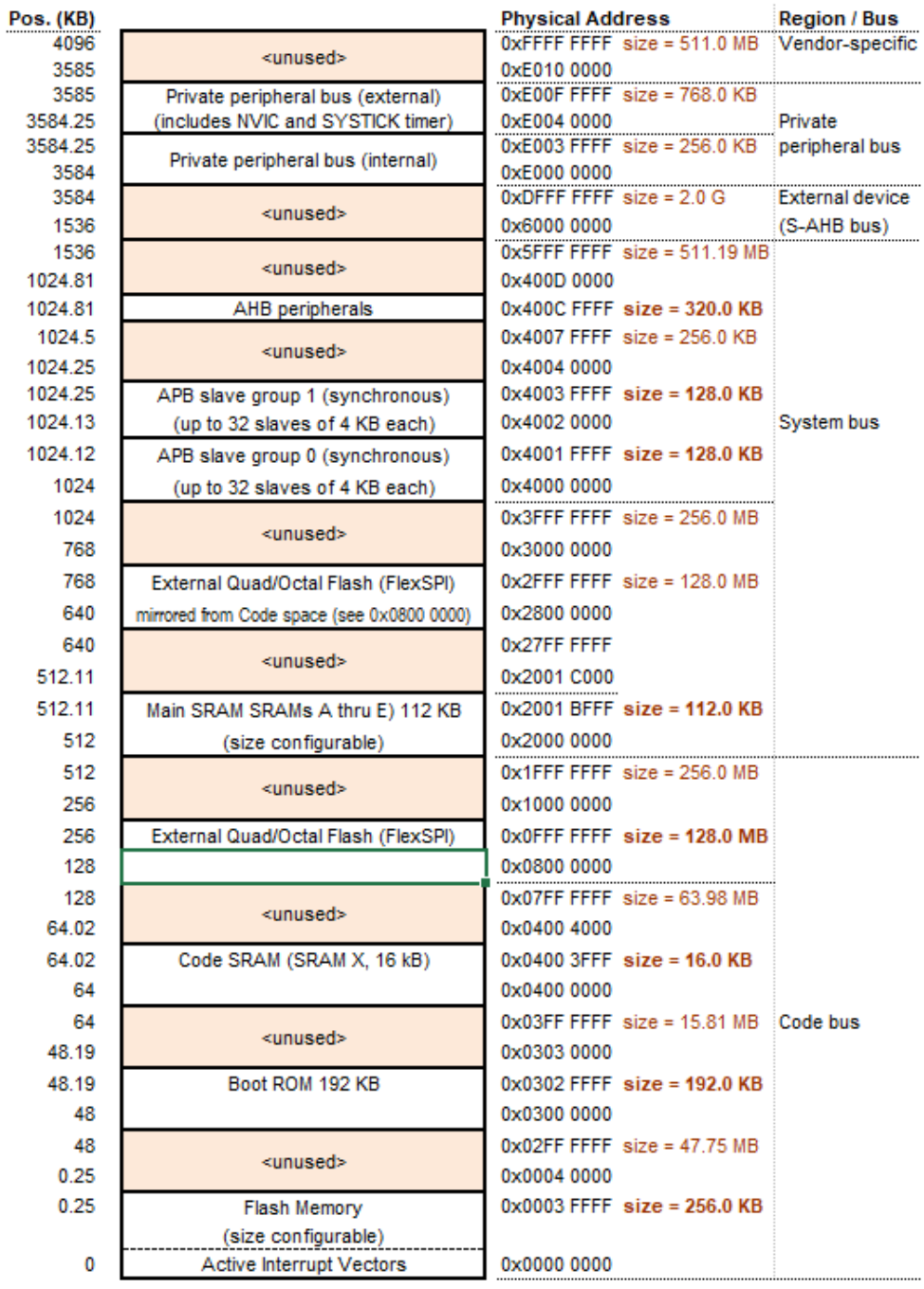

Figure 1. LPC553x series FLASH memory layout

1.3 Boot selection

There are four boot modes for ROM. ROM uses the ISP pins or CMPA configuration to select the boot mode for on-chip FLASH boot, FlexSPI boot, ISP boot, or auto boot mode. For more details, see Boot mode and ISP download mode based on ISP pins.

The default boot source is to use ISP pin. See **CMPA -> BOOT_CFG -> DEFAULT_BOOT_SOURCE** in .

Table 1. Default boot source in CMPA configuration

CMPA->BOOT_CFG->DEFAULT_BOOT_SOURCE	Description
0	ISP pin source (default)
1	FlexSPI FLASH
2	Serial ISP boot
3	Internal FLASH
4	Auto boot similar to ISP auto boot option

When CMPA->BOOT_CFG->DEFAULT_BOOT_SOURCE = 0 (default), ISP pin determines the boot option, as shown in .

Table 2. Boot mode and ISP download mode based on ISP pin

Boot mode	ISP1 (PIO0_7)	ISP0 (PIO0_5)	Description
Internal FLASH boot	LOW	LOW	To boot from internal FLASH.
ISP boot	LOW	HIGH	To download images from UART/SPI/I2C/USB, and so on.
FLEXSPI boot	HIGH	LOW	To boot from external NOR FLASH.
Auto boot	HIGH	HIGH	To boot in priority: Internal boot -> External NOR FLASH boot -> Recovery boot -> ISP mode.

The 3’ bits in CMPA determine the ISP download mode interface. By default, `ISP_MODE0-2` is `3'b0`, which is auto ISP mode. In most cases, there is no need to modify `ISP_MODE` bit in CMPA.

Table 3. ISP download mode based on DEFAULT_ISP_MODE bits (6:4, word 0 in CMPA)

ISP boot mode	ISP_MODE_2	ISP_MODE_1	ISP_MODE_0	Description
Auto ISP	0	0	0	LPC553x/LPC55S3x probes the active peripheral from `UART0`, `I2C1`, `HS_SPI`, `USB0-FS`, or `CAN`. To download images from the probed peripherals.
USB HID ISP	0	0	1	To download images of the **USB0** port.
UART ISP	0	1	0	To download images.
SPI slave ISP (HS-SPI)	0	1	1	To download images.
I2C slave ISP	1	0	0	To download images.
CAN slave ISP1	1	0	1	To download images
Disable ISP	1	1	1	To disable ISP mode.

For descriptions of pins used by each ISP interface, see LPC553x UM.

1.4 Boot image offset

The bootloader looks for the boot image from a specified offset on a boot media. For details, see Table 4.

Table 4. Boot image offset

Boot media	Application image offset
Internal FLASH boot	0x0
FlexSPI NOR FLASH boot	0x1000
SPI 1-bit NOR recovery Boot	0x0

NOTE

Set CPU clock to the boot speed specified in CMPA field. Images boot directly from internal FLASH or external NOR FLASH. If the image is boot from FlexSPI NOR FLASH, the application does not change FlexSPI clock. Otherwise, FlexSPI stops working and the application hangs.

1.5 Boot image header

Once the boot mode is determined (selected as FlexSPI boot) and the boot image is available on NOR FLASH, the ROM bootloader tries to boot image from NOR FLASH. The beginning of the image is compatible with Arm Cortex standard vector table format but it uses the reserved (0 value) slot for special ROM definitions.

For internal FLASH, the base space address is `0x0000_0000`. For FlexSPI, the base space address is `0x0800_0000`.

Table 5. Image header layout

Offset	Size in byte	Symbol	Description
`0x00`	4	Initial SP	Stack pointer.
`0x04`	4	Initial PC	The first execution instruction.
`0x08`	24	Vector table	Cortex-M33 Vector table entries.
`0x20`	4	Image length	The image length.
`0x24`	4	Image type	Image type: • `0x0000` — Plain image • `0x0002` — Plain Image with CRC • `0x0004` — XIP plain signed • `0x0005` — XIP plain with CRC • `0x0006` — SB3 file
`0x28`	4	`offsetToExtendedHeader`	Authenticate block offset or CRC32 checksum.
`0x2C`	8	Vector table	
`0x34`	4	`imageExecutionAddress`	Image load address

Table continues on the next page...

Table 5. Image header layout (continued)

Offset	Size in byte	Symbol	Description
0x38	4	Vector table	

This application note focuses on the easiest one: plain image. In this mode, the image type is **0x0000** and image length is **0**.

2 Programming NOR FLASH via blhost (Non-Secure)

ROM supports access to different Quad/NOR SPI FLASH devices from various vendors via the FlexSPI interface. By employing the FLASH Configuration Block (FCB) located at offset 0x400 on the FLASH device, ROM uses 1-bit, 2-bit (dual), 4-bit (quad), or 8-bit (octal or HyperBus) mode.

To use an external memory device correctly, enable the device with the corresponding configuration profile. If the external memory device is not enabled, then it cannot be accessed with the ROM ISP command. The boot ROM enables specific external memory devices using a pre-assigned memory identifier (FCB), supported external memory devices.

FCB located at offset 0x400 on the FLASH device. It is a 512 bytes pre-assigned memory identifier by ROM and describes every detail of external NOR FLASH. The Boot ROM utilizes FCB to get all the information on NOR FLASH and configure NOR FLASH via FlexSPI. For FCB details, see **Chapter 13.3.1.1.2 FlexSPI NOR FLASH boot** in the LPC553x and LPC55S3x Reference Manual document.

2.1 Connecting to NOR FLASH

This section describes how to use the blhost tool to program the image into external NOR FLASH for booting. The blhost tool uses UART, SPI, I2C, and USB HID to communicate with the ROM code via ROM ISP mode.

Table 6. FlexSPI pin assignments for NOR FLASH connection

FlexSPI pin	GPIO
FLEXSPI_SSEL0	PIO0_21
FLEXSPI_SSEL1	PIO0_22
FLEXSPI_CLK	PIO0_19
FLEXSPI_D0	PIO0_6
FLEXSPI_D1	PIO0_4
FLEXSPI_D2	PIO0_3
FLEXSPI_D3	PIO0_2
FLEXSPI_D4	PIO1_16
FLEXSPI_D5	PIO1_15
FLEXSPI_D6	PIO1_27
FLEXSPI_D7	PIO1_29
FLEXSPI_DQS	PIO0_25

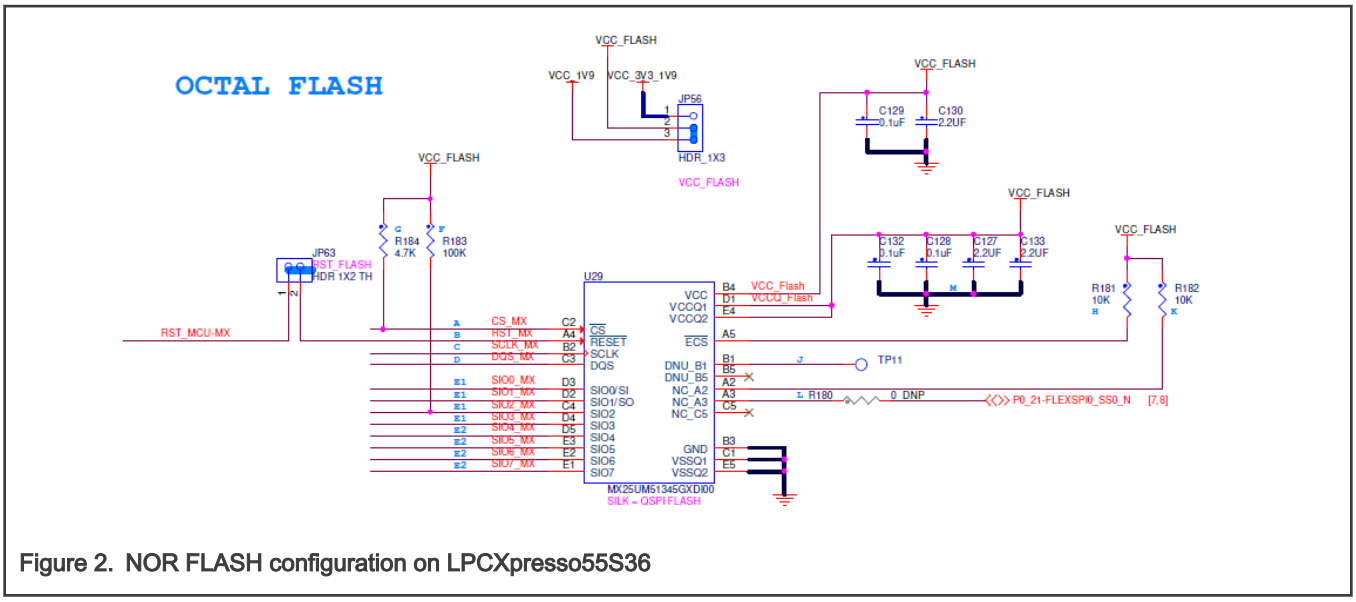

Figure 2. NOR FLASH configuration on LPCXpresso55S36

2.2 Configuring FlexSPI NOR FLASH

The structure of FLEXSPI NOR FLASH configuration parameters is complex but there is a simple way to use it. To encode FCB, NXP defines two `uint32_t` variables, `option0` and `option1`. In most cases, configure only `option0` and leave `option1` as `0x0000_0000`.

For more information, see **Chapter 11.3.1.2.9.2 FLEXSPI NOR FLASH configuration parameters** in LPC553x UM.

Table 7 lists some most used options.

Table 7. Option code

Option0 code	Description
`0xc0000001`	QuadSPI NOR - Quad SDR Read
`0xc0233002`	HyperFLASH 1V8 (50 MHz)
`0xc0333002`	HyperFLASH 3V0 (50 MHz)
`0xc0433005`	MXIC OPI DDR (OPI DDR enabled by default) (50 MHz)
`0xc0600002`	Micron NOR DDR (50 MHz)
`0xc0603002`	Micron OPI DDR (50 MHz)
`0xc0633002`	Micron OPI DDR (DDR read enabled by default) (50 MHz)
`0xc0803002`	Adesto OPI DDR (50 MHz)

2.3 Programming NOR FLASH via blhost

LPCXpresso55S36 uses MX25UM513 to connect to FlexSPI interface.

1. Store the configuration parameters in RAM. These parameters are used to configure the FLEXSPI in the next step. As shown in Figure 4, the configuration parameter for FLEXSPI is `0xC0403001`.
2. Select the configuration parameters according to the FLASH type.

2.3.1 Entering ISP mode

1. To set boot mode to ISP boot, set ISP0 to HIGH and ISP1 to LOW.
2. Connect the FLEXSPI signals with correct pin in the board.
3. Power off the board.
4. Power on the board. Use a USB cable (connect to J3) to connect ISP USB interface to PC.

2.3.2 Testing ISP connectivity

Test whether the MCU enters ISP mode and whether the hardware connection is OK. To ping with ROM, use the `get-property 1` command.

```
$ ./blhost.exe -u 0x1Fc9,0x0025 get-property 1
Inject command 'get-property'
Response status = 0 (0x0) Success.
Response word 1 = 1258488064 (0x4b030100)
Current Version = K3.1.0
```

Figure 3. Ping ISP connectivity

2.3.3 Generating FLASH configuration block

Generate FLASH configuration block with `option0` code and store the configuration block in RAM.

```
$ ./blhost.exe -u 0x1Fc9,0x0025 fill-memory 0x2000F000 4 0xC0000001
Inject command 'fill-memory'
Successful generic response to command 'fill-memory'
Response status = 0 (0x0) Success.
```

```
$ ./blhost.exe -u 0x1Fc9,0x0025 configure-memory 0x9 0x2000F000
Inject command 'configure-memory'
Successful generic response to command 'configure-memory'
Response status = 0 (0x0) Success.
```

Figure 4. Generating FLASH config block(FCB) and configure the FLASH

2.3.4 Erasing/Programming NOR FLASH with blhost

Now, the external NOR FLASH is successfully configured and you can erase/program it.

```
$ ./blhost.exe -u 0x1Fc9,0x0025 flash-erase-region 0x08000000 0x20000
Inject command 'flash-erase-region'
Successful generic response to command 'flash-erase-region'
Response status = 0 (0x0) Success.
```

Figure 5. Erasing NOR FLASH

```
$ ./blhost.exe -u 0x1Fc9,0x0025 read-memory 0x08000400 0x100
Inject command 'read-memory'
Successful response to command 'read-memory'
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
(1/1)100% Completed!
Successful generic response to command 'read-memory'
Response status = 0 (0x0) Success.
Response word 1 = 256 (0x100)
Read 256 of 256 bytes.
```

Figure 6. Reading NOR FLASH

```
$ ./blhost.exe -u 0x1Fc9,0x0025 write-memory 0x08001000 boot_image.bin
Inject command 'write-memory'
Preparing to send 75464 (0x126c8) bytes to the target.
Successful generic response to command 'write-memory'
(1/1)100% Completed!
usbhid: received data phase abort
Response status = 10203 (0x27db) kStatusMemoryCumulativeWrite
Wrote 75464 of 75464 bytes.
```

Figure 7. Programming NOR FLASH

2.3.5 Storing FCB parameter on NOR FLASH

Generate and program the FLEXSPI NOR FCB in FLASH for FLEXSPI boot. It needs an FCB at offset `0x08000400`. This FCB is used to configure the FLEXSPI interface when booting the image from external NOR FLASH via the FLEXSPI interface. The ROM needs FCB every time when it tries to boot image from FLEXSPI FLASH. The FCB is generated from the previous FLEXSPI configuration parameter (`0xc0000002`). Store the generating FCB and programming parameters in RAM. These parameters are used in the next step to generate and program the FCB into FLASH at `0x08000400`.

NOTE

Boot ROM supports programming the generated FCB to the start of the NOR FLASH memory (`0x08000400`) with a specific option `0xF000000F`.

```
$ ./blhost.exe -u 0x1Fc9,0x0025 fill-memory 0x2000F000 4 0xF000000F
Inject command 'fill-memory'
Successful generic response to command 'fill-memory'
Response status = 0 (0x0) Success.
```

Figure 8. Storing the configuration FCB parameter in RAM

```
$ ./blhost.exe -u 0x1Fc9,0x0025 configure-memory 0x9 0x2000F000
Inject command 'configure-memory'
Successful generic response to command 'configure-memory'
Response status = 0 (0x0) Success.
```

Figure 9. FCB generates and programs in FLASH at offset 0x08000400

To check whether FCB is written, read back data at `0x08000400`.

```
$ ./blhost.exe -u 0x1Fc9,0x0025 read-memory 0x08000400 0x200
Inject command 'read-memory'
Successful response to command 'read-memory'
46 43 46 42 00 04 01 56 00 00 00 00 03 03 03 00
00 00 01 00 00 00 00 00 00 00 00 00 01 00 02 00
01 07 00 00 01 0a 00 00 00 00 00 00 00 00 00 00
02 00 00 00 01 00 00 00 00 00 00 00 00 00 00 00
10 00 00 00 01 08 01 00 00 00 00 00 00 00 00 00
00 00 00 04 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
ec 07 13 07 20 0b 04 33 04 27 00 00 00 00 00 00
05 04 04 24 00 00 00 00 00 00 00 00 00 00 00 00
05 07 fa 07 20 0b 04 33 04 27 00 00 00 00 00 00
```

Figure 10. Reading FCB back via blhost tool

As shown in Figure 10, **46 43 46 42** is the ASCII string of **FCFB**. It marks the beginning of the FCB block.

3 Booting from external NOR FLASH (Non-Secure)

This section demonstrates how to boot image from external NOR FLASH. For details, see **Non-Secure Boot ROM** in LPC553X UM.

There are several images type the Boot ROM support, including plain image, plain image with CRC, XIP plain signed, and XIP plain with CRC. This section only deals with the easiest one: plain image.

3.1 FlexSPI NOR FLASH Boot image layout (single image)

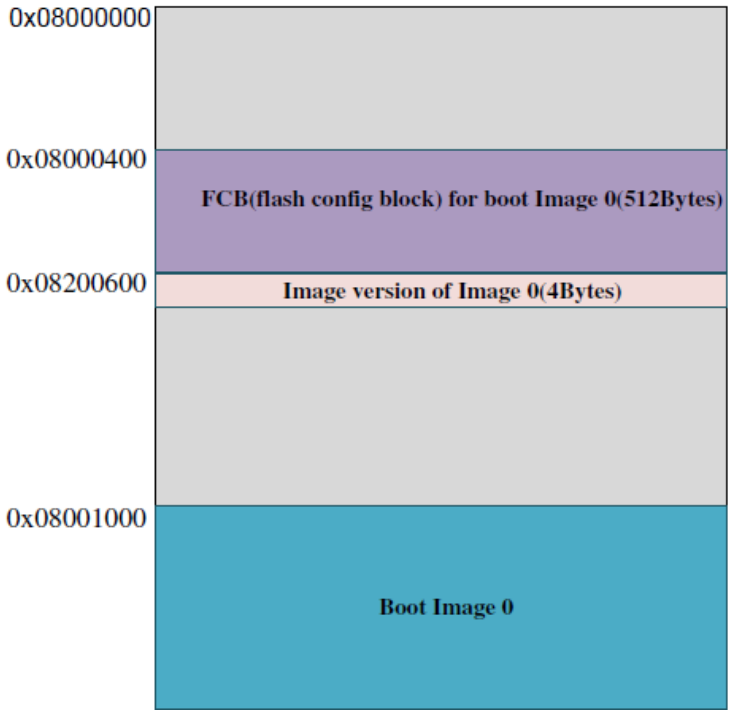

Figure 11. FlexSPI boot image layout (plain, single image)

The FlexSPI boot image address must be at `0x0800_1000` (XIP, loading, and executing address are same). Write a valid FCB block in `0x0800_0400`. The Boot ROM fetches FCB via 1-bit SPI mode, configures the NOR FLASH with FCB information, and tries to boot NOR FLASH image.

3.2 FlexSPI Boot hands on example

3.2.1 Preparing FlexSPI boot image

Take `led_blinky` demo in SDK as example and the project location is:

```
\SDK_2_10_0_LPCXpresso55S36\boards\lpcxpresso55s36\demo_apps\led_blinky
```

1. Change the image start address in the link file. The start address must be `0x0800_1000`.

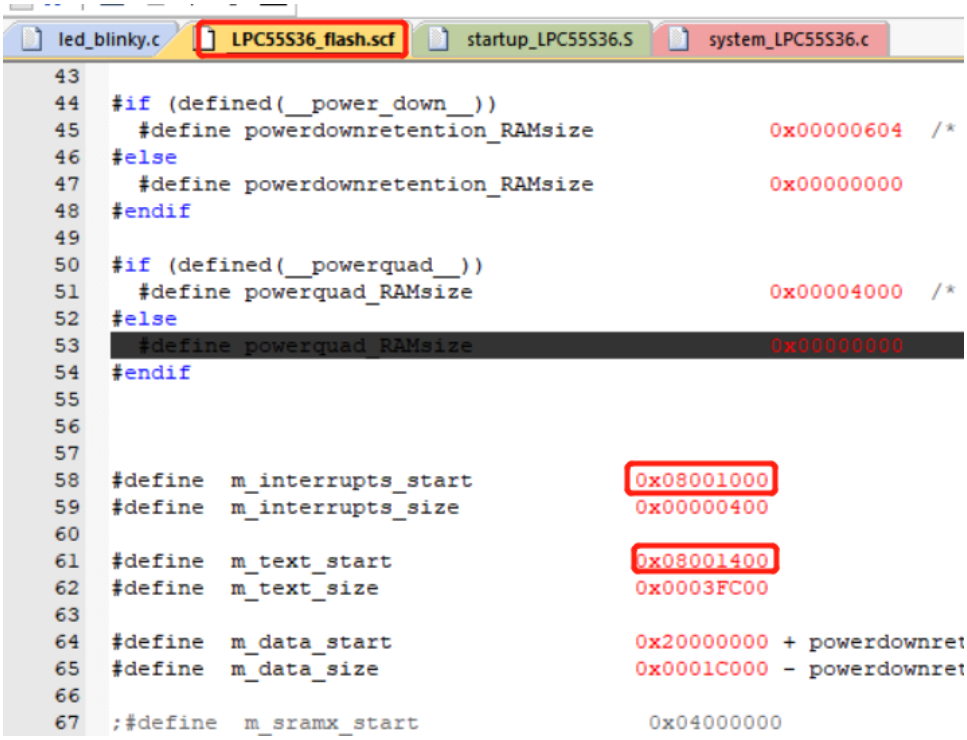

Figure 12. Changing image start address in linker file

2. Comment the line of **BOARD_BootClockFROHF96M** because ROM is using PLL as FlexSPI clock source. When running from external memory, it is not possible to change PLL settings or clock settings. When changing FlexSPI clock settings, the device must run from internal memory (Flash or SRAM).

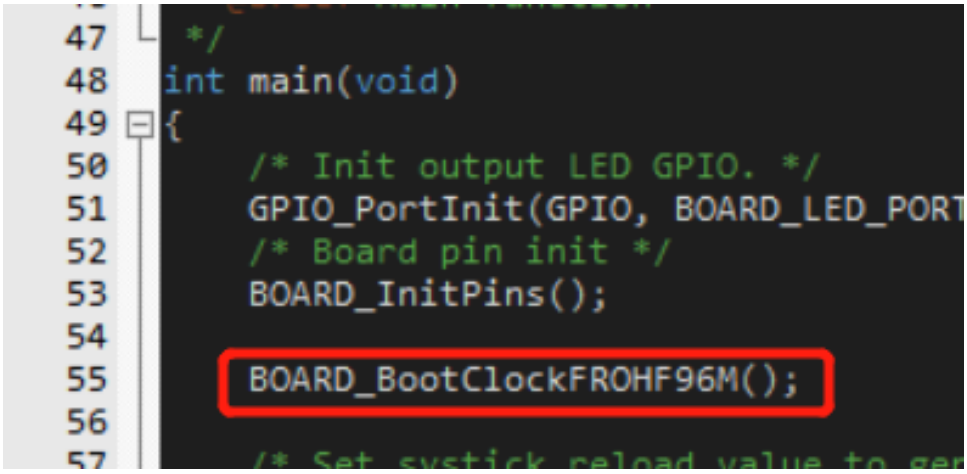

Figure 13. Commenting clock configuration

3. To compile and generate bin file, add the post build command in user option to generate binary file. Compile the project and the **led_blinky.bin** is generated in */mdk/debug* folder.

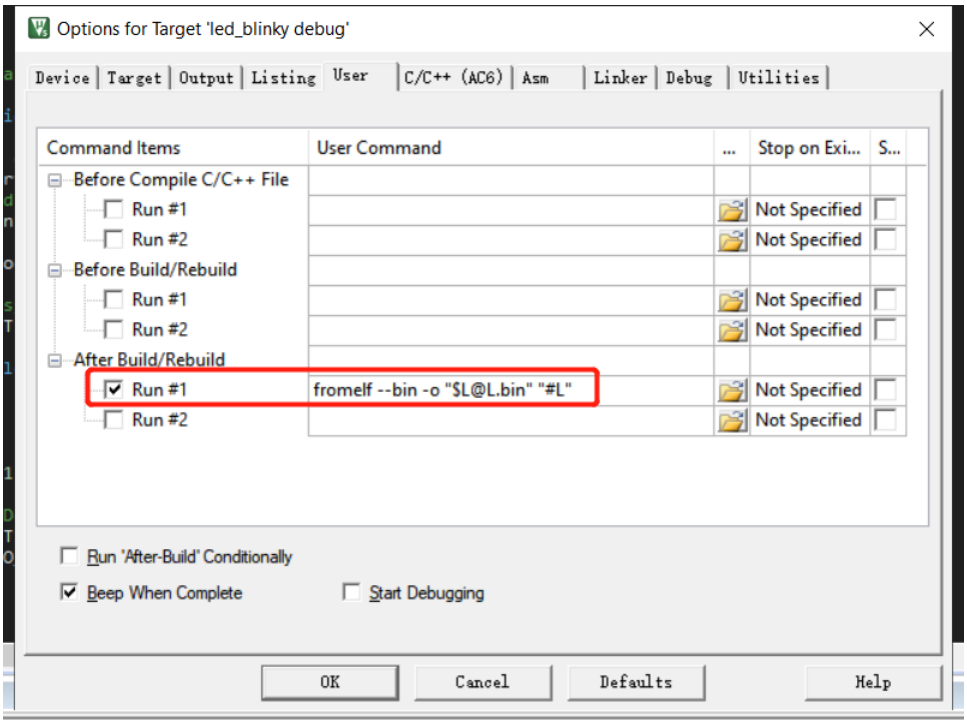

Figure 14. Adding post build command to generate .bin file

3.2.2 Downloading FlexSPI image to NOR FLASH

To write FCB in `0x0800_0400`, follow Programming NOR FLASH via blhost. To download **led_blinky.bin** at `0x0800_1000`, use the `write-memory` command.

Figure 15 shows all required `blhost` commands.

```
C:\Users\YX\Desktop>blhost.exe -u 0x1Fc9,0x0025  fill-memory 0x2000F000 4 0xC0000001
Inject command 'fill-memory'
Successful generic response to command 'fill-memory'
Response status = 0 (0x0) Success.

C:\Users\YX\Desktop>blhost.exe -u 0x1Fc9,0x0025  configure-memory 0x9 0x2000F000
Inject command 'configure-memory'
Successful generic response to command 'configure-memory'
Response status = 0 (0x0) Success.

C:\Users\YX\Desktop>blhost.exe -u 0x1Fc9,0x0025 flash-erase-region 0x08000000 0x20000
Inject command 'flash-erase-region'
Successful generic response to command 'flash-erase-region'
Response status = 0 (0x0) Success.

C:\Users\YX\Desktop>blhost.exe -u 0x1Fc9,0x0025  fill-memory 0x2000F000 4 0xF000000F
Inject command 'fill-memory'
Successful generic response to command 'fill-memory'
Response status = 0 (0x0) Success.

C:\Users\YX\Desktop>blhost.exe -u 0x1Fc9,0x0025  configure-memory 0x9 0x2000F000
Inject command 'configure-memory'
Successful generic response to command 'configure-memory'
Response status = 0 (0x0) Success.

C:\Users\YX\Desktop>blhost.exe -u 0x1Fc9,0x0025  write-memory 0x08001000 led_blinky.bin
Inject command 'write-memory'
Preparing to send 6284 (0x188c) bytes to the target.
Successful generic response to command 'write-memory'
(1/1)100% Completed!
Successful generic response to command 'write-memory'
Response status = 0 (0x0) Success.
Wrote 6284 of 6284 bytes.
```

Figure 15. Programming FCB and download image

3.2.3 Executing NOR FLASH image

Set the ISP boot pin settings to external NOR FLASH boot and press the **Reset** pin on the board. The onboard LED is blinking, which means image executes successfully.

4 Revision history

Rev.	Date	Description
0	10 February 2022	Initial release
1	25 May 2022	Replaced LPC553x with LPC553x/LPC55S3x

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