AN13575

Power Management on LPC55S3x/LPC553x

Rev. 0 — 21 February 2022 Application Note

Contents

1 Introduction

The LPC55S3x/LPC553x family offers a wide peripheral portfolio with focus on low power consumption. This application note describes all the important parts of power management on the LPC553 family and summarizes the main difference and additional features from the previous families.

The following chapters focus on the LPC55S3x/LPC553x power domains, power API, and power-optimization technique. This application note discusses how to use the power management in RT500. The description of the internal DC-DC and LDO regulator functionality on LPC55S3x/LPC553x is in *Using the DC-DC and LDO features* (document AN13528).

2 Power domain and distribution

The LPC55S3x/LPC553x family has 6 power domains. All power domains are powered via the VDD_MAIN power supply, except for PD_AON (Always-On), which is supplied by VBAT. Figure 1 shows the complete schematic of the power management unit:

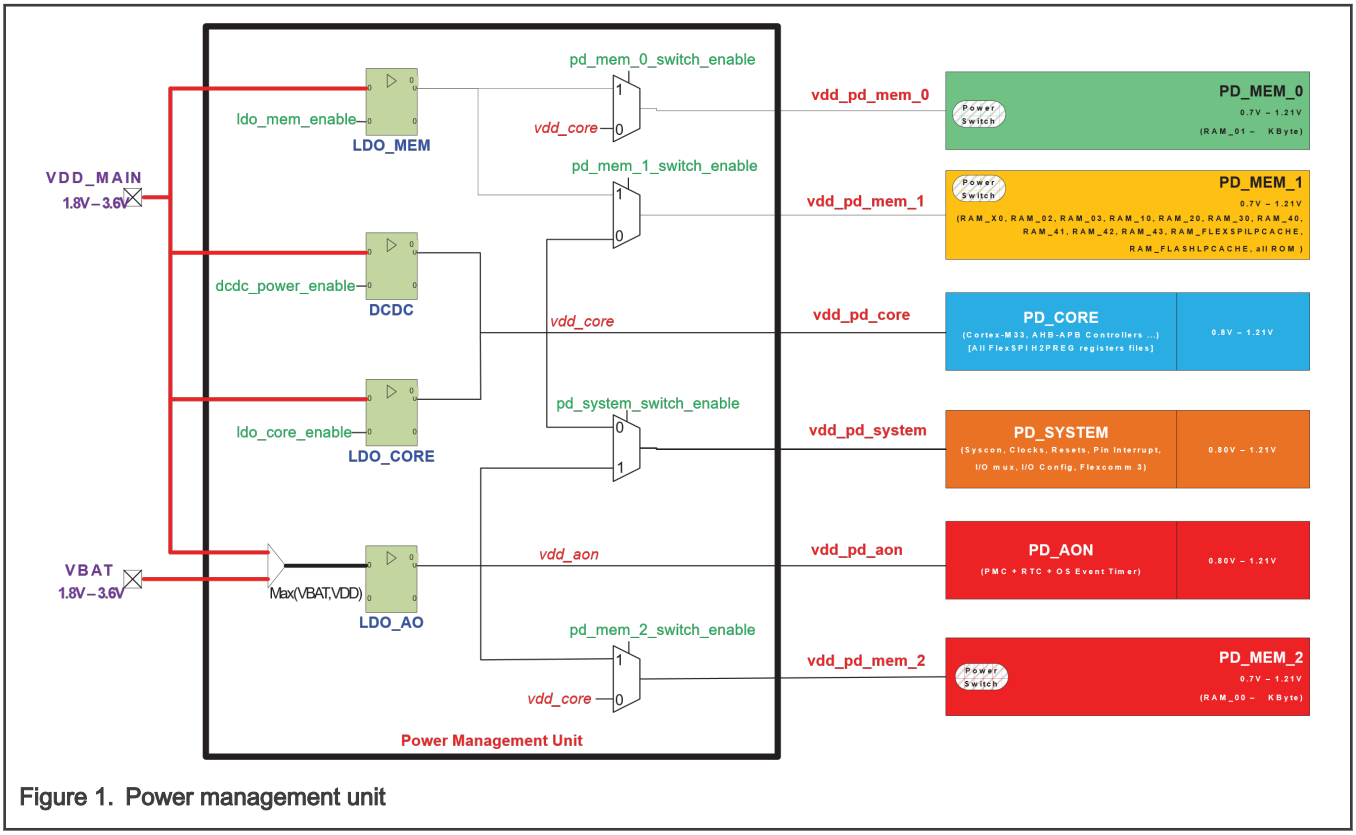

Figure 1. Power management unit

The power domains on LPC553 are the following:

2.1 Always-On Power Domain (PD_AON)

The Always-On Power Domain consists of:

- A set of digital units: Power Management Controller (PMC), RTC, and OS Event Timer.
- Several analog modules located in the Power Management Unit (PMU): FRO32K, XTAL32K, FRO1M, and Analog Comparator.
- 5 wake-up GPIOs.

This power domain has power when VBAT or VDDMAIN are available with a sufficient voltage [1.8 V - 3.6 V].

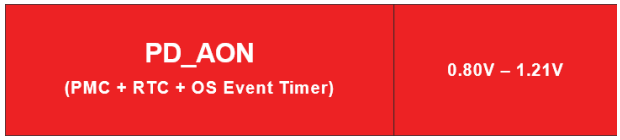

Figure 2. Power domain

2.2 Core Logic Power Domain (PD_CORE)

The Core Logic Power Domain consists of nearly all digital components, such as the Cortex-M33 CPU, system DMA, and almost the whole Flexcom. All digital units not located in the PD_AO or PD_SYSTEM power domains are part of the Core Logic Power Domain.

The Core Logic Power Domain is supplied by:

- The LDO_CORE (configured in the high-power mode) or the DC-DC in ACTIVE.
- The LDO_CORE (configured in the low-power mode) during DEEP-SLEEP.

The Core Logic Power Domain is shut down in the POWER-DOWN and DEEP-POWER-DOWN low-power modes.

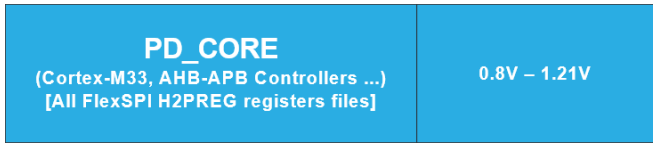

Figure 3. Core Logic Power Domain

2.3 System Power Domain (PD_SYSTEM)

The System Power Domain consists of:

- System-critical digital components: Reset and Clock controllers, System Configuration (SYSCON).
- All GPIOs with their associated configuration and multiplexing (IOCON).
- The Flexcomm3 (UART, SPI, and I2C) and both Group GPIO Input Interrupts (GINT0, GINT1).
- The PUF Keys Store.

The System Power Domain is supplied by:

- The LDO_CORE (configured in the High-Power Mode) or the DC-DC in ACTIVE.
- The LDO_CORE (configured in the Low-Power Mode) during DEEP SLEEP.
- The LDO_AO during POWER DOWN.

The System Power Domain is shut down during the DEEP POWER DOWN low-power mode.

Figure 4. PD_SYSTEM

2.4 First SRAM Power Domain (PD_MEM_0)

The first SRAM Power Domain (PD_MEM0) consists in a single SRAM instance: RAM_01 (4 kB). PD_MEM0 is supplied by:

- The LDO_CORE (configured in the high-power mode) or the DC-DC in ACTIVE.
- The LDO_MEM during DEEP-SLEEP, POWER-DOWN, and DEEP-POWER-DOWN low-power modes.

Figure 5. SRAM Power Domain (PD_MEM_0)

2.5 Second SRAM Memories Power Domain (PD_MEM_1)

The second SRAM Power Domain (PD_MEM1) consists of these SRAM instances: RAM_X0 (16 kB), RAM_02 (4 kB), RAM_03 (4 kB), RAM_10 (32 kB), RAM_20 (32 kB), RAM_30 (16 kB), RAM_40 (4 kB), RAM_41 (4 kB), RAM_42 (4 kB), RAM_43 (4 kB).

PD_MEM1 is supplied by:

- The LDO_CORE (configured in the high-power mode) or the DC-DC in ACTIVE.
- The LDO_MEM during DEEP-SLEEP, POWER-DOWN, and DEEP-POWER-DOWN low-power modes.

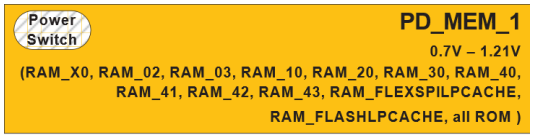

Figure 6. PD_MEM_1

2.6 Third SRAM Memories Power Domain (PD_MEM_2)

The third SRAM Memories Power Domain (PD_MEM2) consists of a single SRAM instance: RAM_00 (4 kB).

PD_MEM2 is supplied by:

- The LDO_CORE (configured in the High-Power Mode) or the DC-DC in ACTIVE.
- The LDO_AO during the DEEP SLEEP, POWER DOWN, and DEEP POWER DOWN low-power modes.

Figure 7. PD_MEM_2

Table 1 summarizes the power state of the different power domains according to the power modes.

Table 1. Power modes vs power domains

MODE	PD_CORE	PD_SYSTEM	PD_AON	PD_MEM_0	PD_MEM_1	PD_MEM_2
ACTIVE	ON	ON	ON	ON	ON	ON
SLEEP	ON	ON	ON	ON	ON	ON
DEEP SLEEP	ON	ON	ON	Configurable	Configurable	Configurable
POWER DOWN	OFF	ON	ON	Configurable	Configurable	Configurable
DEEP POWER DOWN	OFF	OFF	ON	Configurable	Configurable	Configurable

3 Power API

The power API serves as a control of device power consumption. The entry to low-power modes can be configured through simple calls to the low-power profile API. The power API functions are available in the SDK software package at LPC553x-LPC55S3x|ARM Cortex-M33 32-bit Microcontrollers (MCUs)|NXP.

3.1 Power API categories

The power API on LPC55S3x/LPC553x is divided into 5 categories:

- Power-library-initialization function and device wake-up cause function.
- Low-power entry functions prepare the device to enter low-power modes.
- Core power domain supply source functions.
- CPU and system frequency configuration.
- Manages power consumption of device SRAM instances.
- Figure 8 shows the high-level structure of the power-control API function.

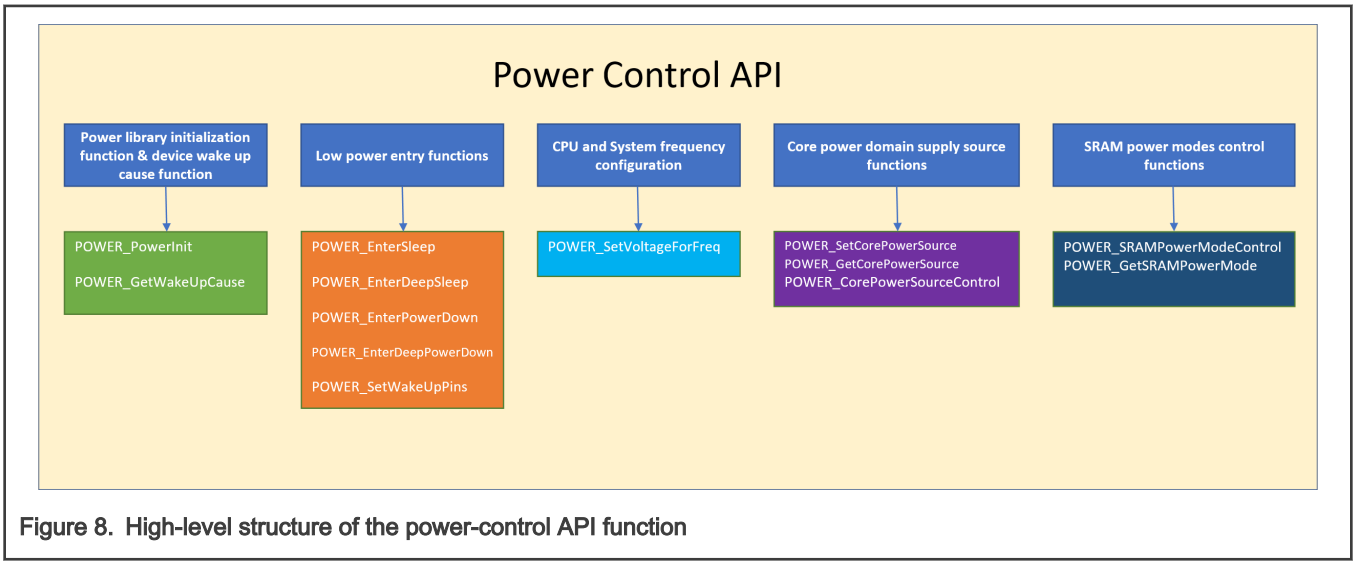

Figure 8. High-level structure of the power-control API function

The following part shortly summarizes the power library API. For detailed information, see the LPC55S3x/LPC553x reference manual or *Low-Power Modes and Wake-Up Time* (document AN13056).

3.2 Power library initialization function and device wake-up cause function

API function POWER_PowerInit:

```
power_status POWER_PowerInit (void);
```

This routine checks the status of the hardware boot sequence and performs a power-related initialization of the system (such as configuring internal voltage regulators).

API function POWER_GetWakeUpCause:

```
void POWER_GetWakeUpCause (power_reset_cause_t * reset_cause,
power_boot_mode_t * boot_mode
power_wakeup_pin_t * wakeup_pin_cause)
```

This routine returns key information related to device events, such as the most recent reset cause, the most recent low-power mode, and the most recent wake-up pin events.

3.3 Low-power entry functions

API Function POWER_EnterSleep:

```
void POWER_EnterSleep(void)
```

The SLEEP mode saves power by stopping the Cortex-M33 execution without affecting peripherals or requiring significant wake-up time.

The part wakes up from the SLEEP mode after:

- Any interrupt enabled in the CORTEX-M33 Nested Vector Interrupt Controller (NVIC) arrives at the processor.
- Any chip reset occurs (Power-on Reset, Brownout detector reset, pin reset, and so on).

API function POWER_EnterDeepSleep:

```
void POWER_EnterDeepSleep ( uint32_t exclude_from_pd[2] uint32_t sram_retention_ctrl uint32_t
wakeup_interrupts[4] uint32_t hardware_wake_ctrl)
```

This routine prepares the part and then enters the DEEP-SLEEP low-power mode. The API function configures which analog/digital components remain running, so that an interrupt from one of these analog/digital peripherals can wake up the part.

API function POWER_Enterpower down:

```
void POWER_EnterPowerDown ( uint32_t exclude_from_pd[1] uint32_t sram_retention_ctrl uint32_t
wakeup_interrupts[2] uint32_t cpu_retention_addr)
```

This routine configures the POWER-DOWN low-power mode. It allows controlling which peripherals are powered up and which SRAM instances are in a retention state during POWER-DOWN.

API function POWER_EnterDeepPowerDown:

```
void POWER_EnterDeepPowerDown ( uint32_t exclude_from_pd[1] uint32_t sram_retention_ctrl uint32_t
wakeup_interrupts[2] uint32_t wakeup_io_ctrl)
```

This routine prepares the part and then enters the DEEP-POWER-DOWN low-power mode. The API function configures which analog/digital components remain running, so that an interrupt from one of these analog/digital peripherals can wake up the part.

API function POWER_SetWakeUpPins:

```
void POWER_SetWakeUpPins ( uint32_t wakeup_io_cfg_sr uint32_t wakeup_io_ctrl)
```

This routine configures the 5 wake-up pins before entering the DEEP-SLEEP or POWER-DOWN modes. It is expected to be called before calling "POWER_EnterDeepSleep" or "POWER_EnterPowerDown". The API function configures which wake-up pins can wake up the device from a low-power mode and sets up some other pin parameters, such as the internal pull-up/pull-down and the rising or falling edge detections.

3.4 CPU and system frequency configuration

API function POWER_SetVoltageForFreq:

```
void POWER_SetVoltageForFreq (uint32_t system_freq_hz)
```

The "POWER_SetVoltageForFreq" API configures the device's internal power-control settings according to the calling arguments. The goal is to prepare on-chip power regulators (DC-DC converter/core and always-on low-drop-out regulators) to deliver the amount of power needed for the requested performance level, as defined by the CPU operating frequency.

3.5 Core power domain supply source functions

API function POWER_SetCorePowerSource:

```
power_status_t POWER_SetCorePowerSource (power_core_pwr_source_t pwr_source)
```

The "POWER_SetCorePowerSource" API selects the core logic supply source from the DC-DC buck converter and the core logic low drop-out regulator (LDO_CORE, in both the high-power and low-power modes). When a supply source is selected, the other internal sources are disabled. For example, if you select the DC-DC buck converter, the LDO_CORE (for both the high-power and low-power modes) will be disabled.

API function POWER_GetCorePowerSource:

```
power_core_pwr_source_t POWER_GetCorePowerSource (void)
```

The "POWER_GetCorePowerSource" API returns the current core logic supply source.

API function POWER_CorePowerSourceControl:

```
power_status_t POWER_CorePowerSourceControl (power_core_pwr_source_t pwr_source
power_core_pwr_state_t pwr_state)
```

The "POWER_GetCorePowerSource" API allows controlling the state (enabled or disabled) of the core logic internal regulators (DC-DC and LDO_CORE).

3.6 SRAM power modes control functions

API function POWER_SRAMPowerModeControl:

```
power_status_t POWER_SRAMPowerModeControl (power_sram_bit_t sram_inst
power_sram_pwr_mode_t pwr_mode)
```

The "POWER_SRAMPowerModeControl" API allows to configure the SRAM instances' (low) power modes when the part is in the ACTIVE mode.

API function POWER_GetSRAMPowerMode:

```
power_status_t POWER_GetSRAMPowerMode (power_sram_index_t sram_index)
```

The "POWER_GetSRAMPowerMode" API allows to determine the power mode of a single SRAM instance when the part is in the ACTIVE mode.

4 LPC55S3x/LPC553x power modes

The LPC55S3x/LPC553x includes the following power-saving modes and wake-ups:

- Integrated PMU (Power Management Unit) to minimize power consumption.
- Configurable wake-up options form peripheral interrupts.
- The Micro-Tick Timer running from the watchdog oscillator can be used to wake-up the device from all low-power modes.
- The Real-Time Clock (RTC), running from the 32.768 kHz clock, can be used to wake up the device from all low-power modes.
- Power-On Reset (POR).
- Brownout Detector (BOD) for VBAT_DC-DC with separate thresholds for forced reset.

The LPC55S3x/LPC553x module implements 4 basic power modes: Active, Sleep, Deep Sleep, Power down, and Deep Power down. The following section explains the difference between the power modes using the following decoding bullets:

- ↑ ON
- ↓ OFF
- ↘ Software selection: ON, OFF, or low power

4.1 Active

This is the default mode after RESET.

- ↑ The clocks to the CPU, memories, and peripherals are enabled.

4.2 Sleep

- ↓ Stops the clock to the CPU (the system clock).
- ↓ Suspends the instruction execution until RESET or an interrupt occurs.
- ↘ The peripherals can be clocked and continue to operate.
- ↘ The peripherals may generate interrupts to resume the CPU operation.
- ↘ The SRAM that was not shut down maintains its content.
- ↑ The CPU state registers and peripheral registers are maintained.
- ↑ The pins' logic levels remain static.

4.3 Deep sleep

This mode is configurable and can potentially turn off almost the whole on-chip power consumption, resulting in longer wake-up times.

- ↓ The CPU clock is shut down.
- ↓ The power consumed by the analog peripherals and the dynamic power used by the processor.
- ↘ The peripherals (if not configured) receive no internal clocks.
- ↘ The individual blocks may be in the on, low-power, or off states; as defined in the software.
- ↘ The device features can be automatically disabled.
- ↘ The SRAM that was not shut down maintains its content.
- ↘ This runs the selectable peripherals.
- ↘ The analog blocks are powered down by default, but they can be configured by software.

- ↑ The device registers maintain their content.

4.4 Power Down

- ↓ Turns off nearly all on-chip power consumption by eliminating power.
- ↘ All registers lose their internal states, except for those located in the PD_SYSTEM and PD_AO power domains.
- ↘ The SRAM and register content is retained (software-configurable via power API).
- ↓ All registers lose their internal states, except for those located in the PD_SYSTEM and PD_AO power domains.
- ↘ The GPIO group interrupts (GINT0 and GINT1), selected serial peripherals in Flexcomm3 (SPI, I2C, USART), RTC, OS, Event Timers, and Analog Comparator can be left running to wake up the device.

4.5 Deep power down

- ↓ The entire chip's clock and power are shut down.
- ↓ Registers are not retained (except for the PMC, RTC, and OS timer).
- ↘ The SRAM and register content is retained (software-configurable via the power API).
- ↓ All functional pins are tri-stated, except for the 5 wake-up pins and the RESET pin.
- ↑ The RTC is on through VDD_AON.

5 Power-optimization techniques

The following tables show various clocks and peripherals that can be software-configured in reduced-power modes, such as Sleep, Deep Sleep, Power Down, and Deep Power Down.

Table 2. Clocks in reduced power modes

Clocks			Device Low-Power Modes		
Clock	Description	Sleep	Deep Sleep	Power Down	Deep Power Down
FRO1MHz	1-MHz Free Running Oscillator	ON	SW configured	SW configured	SW configured
FRO192M	High-Speed Free Running Oscillator	ON	SW configured	OFF	OFF
FRO32K	32-kHz Free Running Oscillator	Same state as in ACTIVE	SW configured	SW configured	SW configured
XTAL32K	32-kHz Crystal Oscillator	Same state as in ACTIVE	SW configured	SW configured	SW configured
XTALHF	High-Frequency Crystal Oscillator	Same state as in ACTIVE	SW configured	OFF	OFF
PLL0	Phase-Locked Loop Module 0	Same state as in ACTIVE	SW configured	OFF	OFF
PLL1	Phase-Locked Loop Module 1	Same state as in ACTIVE	SW configured	OFF	OFF

Table 3. Peripherals in reduced power modes

Peripherals		Device Low-Power Modes			
Peripheral	Description	Sleep	Deep Sleep	Power Down	Deep Power Down
DC-DC	Bulk DC-DC Converter	Same state as in ACTIVE	OFF	OFF	OFF
BIAS	Analog References	ON	ON	SW configured	OFF
BODCORE	Core Logic Supply Brownout Detector	Same state as in ACTIVE	SW configured	OFF	OFF
BODVDDMAIN	VDD_MAIN supply Brownout Detector	Same state as in ACTIVE	SW configured	OFF	OFF
USBFSPHY	USB Full-Speed Physical Interface	Same state as in ACTIVE	SW configured	OFF	OFF
COMP	Analog Comparator	Same state as in ACTIVE	SW configured	SW configured	
LDOEFUSEPROG	eFUSE Programming Low Drop-Out Regulator	Same state as in ACTIVE	SW configured	OFF	OFF
LDOXTALHF	High-Frequency Crystal Oscillator Low Drop-Out Regulator	Same state as in ACTIVE	SW configured	OFF	OFF
LDOFLASHNV	Non-Volatile Flash Macro Low Drop-Out Regulator	ON	OFF	OFF	OFF
PLL0_SSCG	PLL0 Spread Spectrum Clock Generator	Same state as in ACTIVE	SW configured	OFF	OFF
HSCMP 0, 1, 2	High-Speed Comparator	Same state as in ACTIVE	SW configured	OFF	OFF
OPAMP 0, 1, 2	Operational Amplifier	Same state as in ACTIVE	SW configured	OFF	OFF
VREF	ADCs/DACs Analog Reference Module	Same state as in ACTIVE	SW configured	SW configured	OFF
CMPBIAS	High-Speed Comparators Biasing	Same state as in ACTIVE	SW configured	OFF	OFF

Table continues on the next page...

Table 3. Peripherals in reduced power modes (continued)

Peripherals		Device Low-Power Modes			
Peripheral	Description	Sleep	Deep Sleep	Power Down	Deep Power Down
HSCMPx_DAC (0,1,2)	HSCMP1 (Internal) DAC	Same state as in ACTIVE	SW configured	OFF	OFF
DAC 0, 1, 2	Digital-to-Analog Converter	Same state as in ACTIVE	SW configured	OFF	OFF
STOP_DAC 0, 1, 2	DAC Stop Mode	Same state as in ACTIVE	SW configured	OFF	OFF

6 Conclusion

The LPC55S3x/LPC553x family opens the way for a wide range of low-power applications. Including the internal LDO regulator allows using the MCU in more complex systems with their own power domain. The complete description of DC-DC and internal LDO usage is described in *Using the DC-DC and LDO features* (document AN13528).

7 Revision history

Table 4. Revision history

Revision number	Date	Substantive changes
0	21 February 2022	Initial release

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