

1 Introduction

CoreMark of EEMBC is a benchmark that measures the performance of Microcontrollers (MCUs) and Central Processing Units (CPUs) used in embedded systems. It implements the following algorithms:

- List processing (find and sort)
- Matrix manipulation (common matrix operations)
- State machine (determines whether an input stream contains valid numbers)
- Cyclic Redundancy Check (CRC)

FlexSPI is a new peripheral for LPC553x/LPC55S3x series. It expands code of application and data size. It brings opportunities of many new application designs.

This document emphasizes on how to port CoreMark project and run on external FlexSPI interface, including octal NOR flash and HyperRAM. It provides test results of FlexSPI CoreMark performance data.

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NOTE

Two prerequisite application notes are listed here:

1. *LPC553x/LPC55S3x CoreMark on Cortex-M33 Porting Guide* (document [AN12284](#))
This document guides how to port CoreMark project on LPC553x/LPC55S3x and gives comprehensive view of the key point when evaluating CoreMark project.
2. *Programming and Booting Images from External NOR flash on LPC553x/LPC55S3x* (document [AN13543](#))
This document introduces how to create an external NOR flash image and how to boot the image from external NOR flash.

This document heavily reuses the two application notes. If you are not familiar with basic knowledge related to FlexSPI or CoreMark, read them first.

2 Porting CoreMark project to FlexSPI external memory

The difference between a normal internal flash image and a FlexSPI image is the code space address. Because the FlexSPI AHB address space started is `0x0800_0000`. BootROM defines that any FlexSPI image code execution address starts at `0x0800_1000`. We must change linker file of CoreMark project.

2.1 Getting CoreMark demo source code

This document reuses CoreMark demo source code package available with *LPC553x/LPC55S3x CoreMark on Cortex-M33 Porting Guide* (Document [AN12284](#)). It provides ready-to-use CoreMark project package for all three IDEs. For original source code, the CoreMark data are running on internal flash and internal RAM. We recommend running CoreMark demo first and getting familiar with basic download process and hardware setup. Get the CoreMark result on internal flash/RAM. It provides a baseline score that can compare with FlexSPI external memory CoreMark data.



2.2 Changing code execution address

- Keil

Switch the project configuration to `lpc55s3x_coremark_flash` configuration.

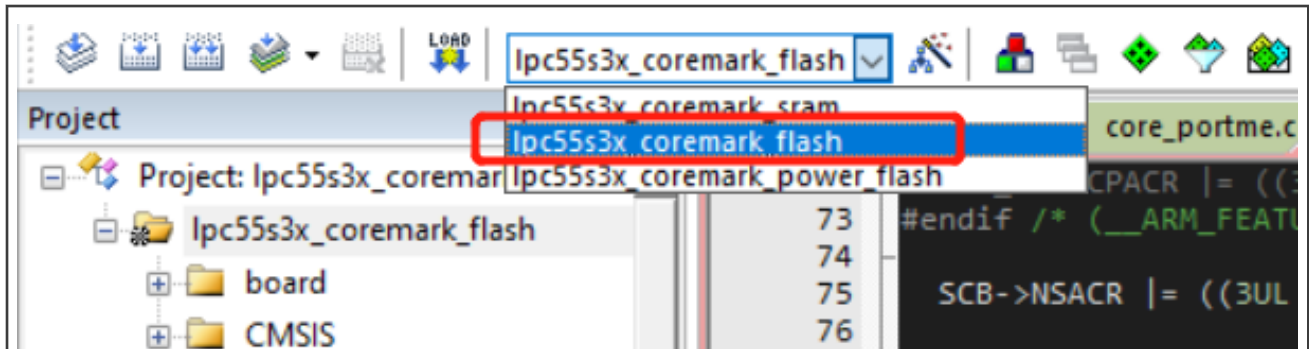


Figure 1. Switching to `lpc55s3x_coremark_flash` configuration

Change the linker file to set code space to start from `0x0800_1000`.

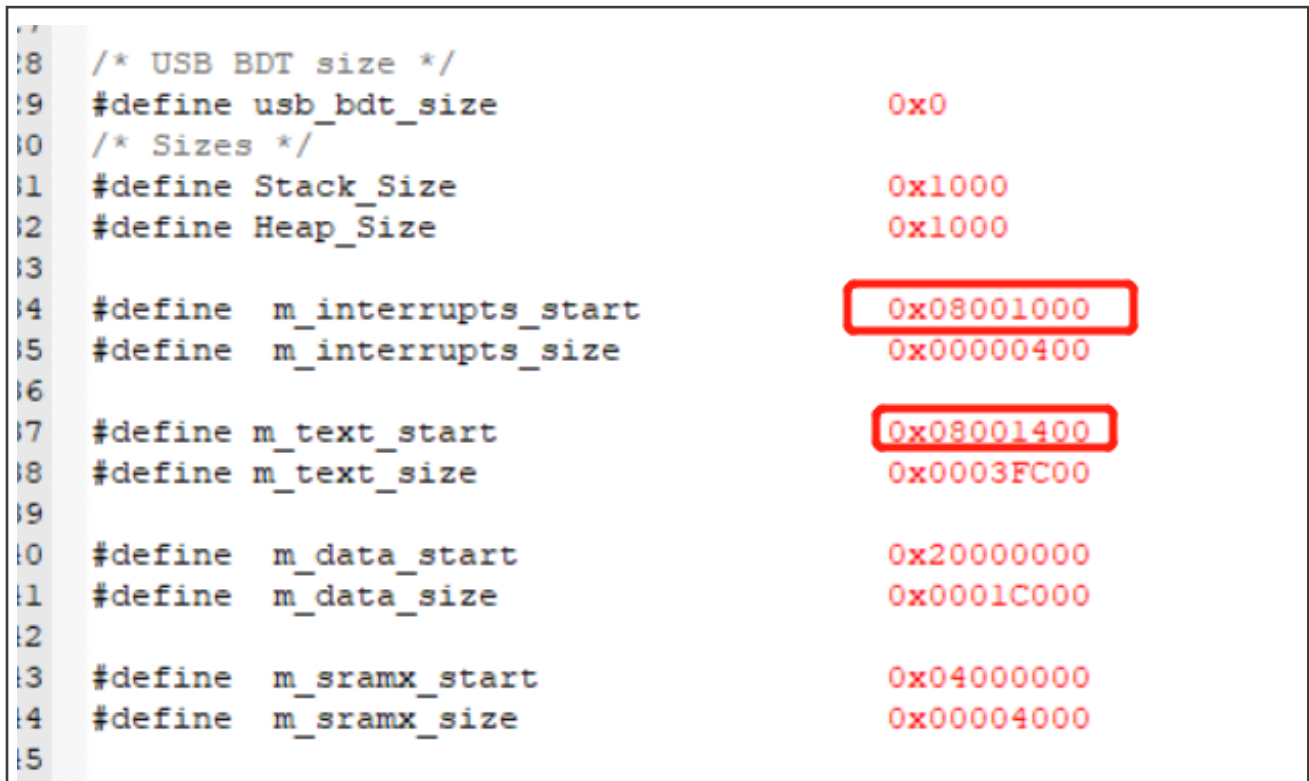


Figure 2. Changing linker file in KEIL

- IAR

Switch the project configuration to `lpc55s3x_coremark_flash` configuration.

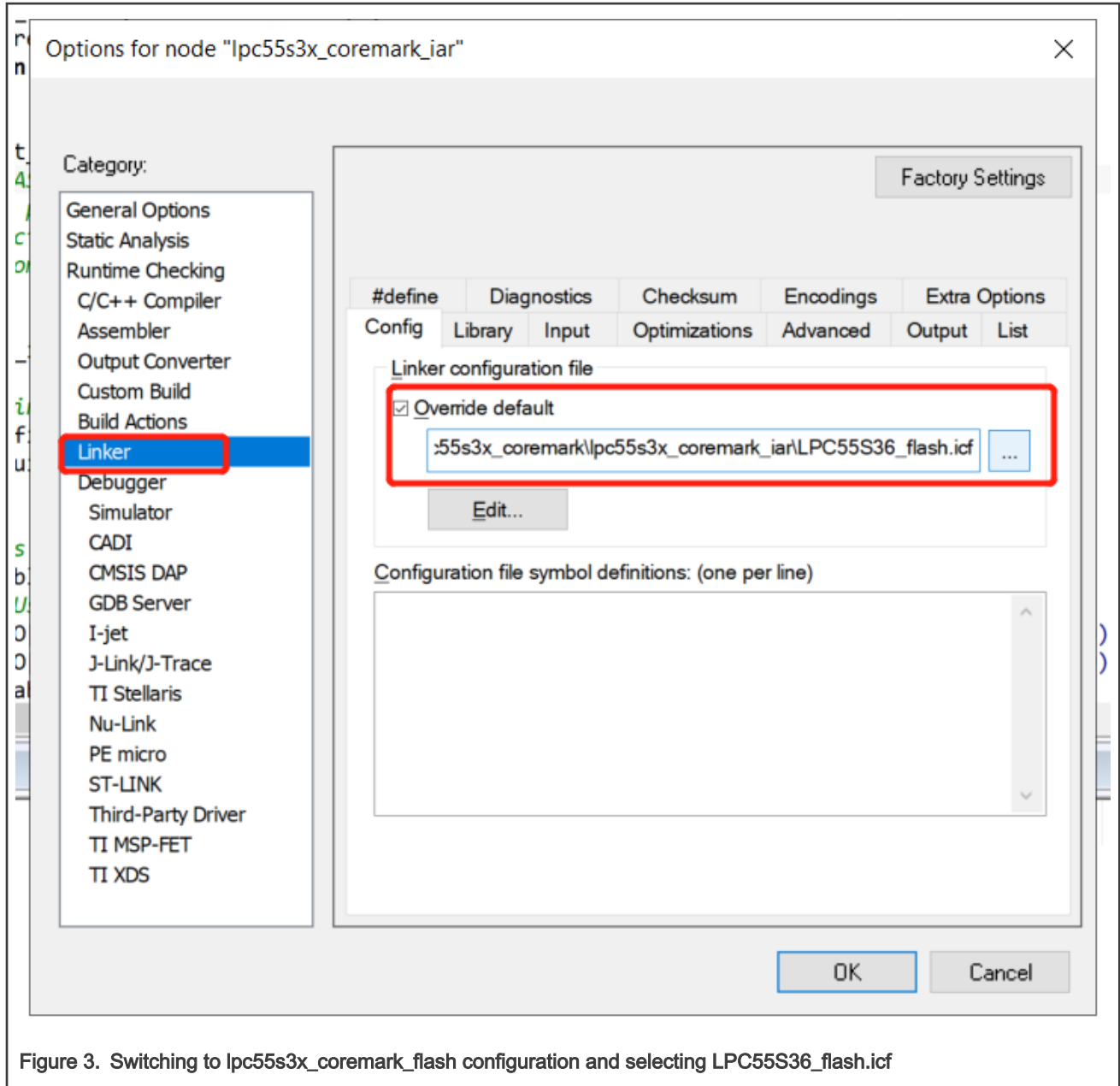


Figure 3. Switching to lpc55s3x_coremark_flash configuration and selecting LPC55S36_flash.icf

```

33
34 define symbol m_interrupts_start           = 0x08001000;
35 define symbol m_interrupts_end           = 0x080013FF;
36
37 define symbol m_text_start               = 0x08001400;
38 define symbol m_text_end                 = 0x0803FFFF;
39
40 define symbol m_data_start                = 0x20004400;
41 define symbol m_data_end                  = 0x20007FFF;
42
43 define symbol m_sramx_start               = 0x04000000;
44 define symbol m_sramx_end                 = 0x04003FFF;
45
    
```

Figure 4. Changing linker file in IAR

• MCUX

Open **Property** -> **C/C++ build** -> **MCU Settings** and change flash location to 0x0800_1000.

Memory details (Generic-M33)*

Default LinkServer Flash Driver:

Type	Name	Alias	Location	Size	Driver
Flash	PROGRA...	Flash	0x8001000	0x40000	LPC553x.cfx
RAM	SRAM	RAM	0x20000000	0x1c000	
RAM	SRAMX	RAM2	0x4000000	0x4000	

Buttons: Add Flash, Add RAM, Split, Join, Delete, Import..., Merge..., Export..., Generate...

Figure 5. Changing linker file in MCUX

All other compile and download step are same as described in *Programming and Booting Images from External NOR flash on LPC553x/LPC55S3x* (document [AN13543](#)).

2.3 Enabling CACHE64

CACHE64 is a peripheral to accelerate FlexSPI performance. By default, CACHE64 is disabled. We need enable CACHE64.

```

cache64_config_t cacheCfg;

/* As cache depends on FlexSPI power and clock, cache must be initialized after FlexSPI power/clock is set */
CACHE64_GetDefaultConfig(&cacheCfg);
CACHE64_Init(CACHE64_POLSEL0, &cacheCfg);
    
```

Figure 6. Adding CACHE64 init function in portable_init()

For more information about CACHE64, see *LPC55S36 Reference Manual*.

3 Coremark result (Octal Flash: MX25UM51345GXDI00)

- **Hardware:**
 - LPCXpresso55S36
 - External nor flash: MX25UM51345GXDI00
- **Internal Flash configuration:**
 - Cache enabled
 - Code in internal Flash
 - Data in SRAM
- **FlexSPI configuration:**
 - FlexSPI clock = FRO96M
 - CACHE64 enabled
 - Octal DDR mode
 - Code in external NOR flash
 - Data in SRAM
- IDE: All IDE optimization setting is same as mentioned in *LPC553x/LPC55S3x CoreMark on Cortex-M33 Porting Guide* (document [AN12284](#)).

Table 1. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 12 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (FlexSPI NOR vs. Internal Flash)
KEIL	4.086	4.170	1.02 %
IAR	4.025	4.081	1.01 %
MCUX	2.964	2.971	1.01 %

Table 2. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 96 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (FlexSPI NOR vs. Internal Flash)
KEIL	3.986	4.011	100 %
IAR	4.023	4.080	101 %
MCUX	2.956	2.952	100 %

Table 3. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 100 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (FlexSPI NOR vs. Internal Flash)
KEIL	3.972	3.995	100 %
IAR	4.01	4.068	101 %
MCUX	2.945	2.938	99 %

Table 4. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 150 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (FlexSPI NOR vs. Internal Flash)
KEIL	3.905	3.874	99 %
IAR	4.004	4.062	101 %
MCUX	2.942	2.936	99 %

4 Coremark result (HyperRAM: W956D8MBYA5I)

By default, the FlexSPI is connected to octal NOR Flash on LPCXpresso55S36. Rework to enable HyperRAM. The LPCXpresso55S36 provides rework guide on schematic. The default configuration is for **4. MX25UM51345GXD100**. Change resistor setting and align to **3. APS6408L-OBM-BA**. For HyperRAM, we choose **W956D8MBYA5I** of Winbond (same configurations as APS6408L).

As HyperRAM cannot save any code and data when power off, you must write a simple loader in internal flash that performs the below tasks:

1. Convert CoreMark image into a C data array and copy to image start address in FlexSPI space.
2. Jump to the start address and execute the image.

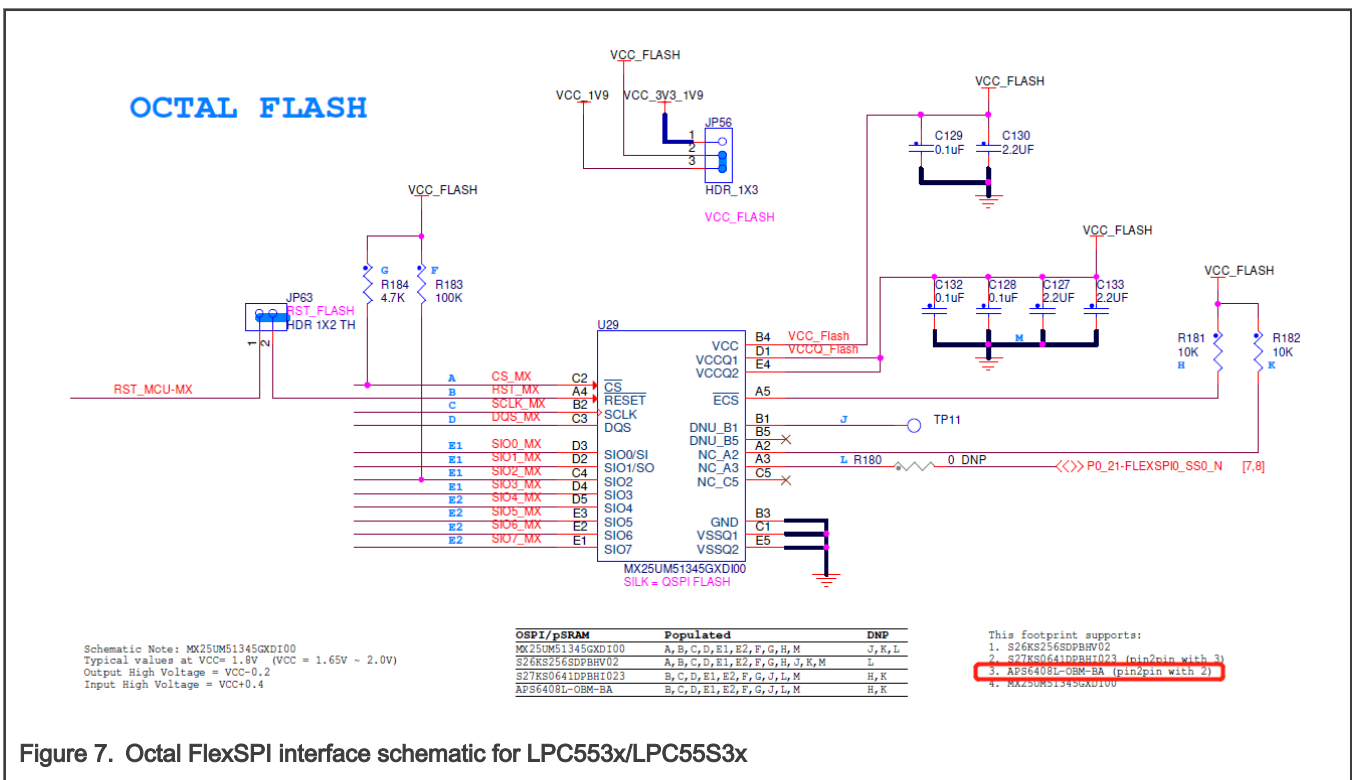


Figure 7. Octal FlexSPI interface schematic for LPC553x/LPC55S3x

- **Hardware:**
 - LPCXpresso55S36
 - HyperRAM: W956D8MBYA5I
- **Internal Flash configuration:**
 - Cache enabled

- Code in internal flash
- Data in SRAM
- **FlexSPI configuration:**
 - FlexSPI clock = FRO96 M
 - CACHE64 enabled
 - Octal DDR mode
 - Code in HyperRAM
 - Data in SRAM
- IDE: IDE optimization setting is same as mentioned in *LPC553x/LPC55S3x CoreMark on Cortex-M33 Porting Guide* (document [AN12284](#)).

Table 5. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 12 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (HyperRAM vs. Internal Flash)
KEIL	4.086	4.173	1.02 %
IAR	4.025	4.041	1.00 %
MCUX	2.964	2.920	0.99 %

Table 6. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 96 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (HyperRAM vs. Internal Flash)
KEIL	3.986	3.991	1.00 %
IAR	4.023	4.010	0.99 %
MCUX	2.956	2.902	0.98 %

Table 7. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 100 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (HyperRAM vs. Internal Flash)
KEIL	3.972	3.971	1.00 %
IAR	4.01	4.039	1.00 %
MCUX	2.945	2.911	0.98 %

Table 8. LPCXpresso55S36 board CoreMark/MHz score when CoreClock = 150 MHz

IDE	CoreMark/MHz (Internal Flash)	CoreMark/MHz (FlexSPI)	Performance (HyperRAM vs. Internal Flash)
KEIL	3.905	3.842	0.98 %
IAR	4.004	4.049	1.01 %
MCUX	2.942	2.916	0.99 %

5 Conclusion

This application note extends the CoreMark project to FlexSPI external memory and gives test result under different Core Clock configuration. Read this document as an extended version of *LPC553x CoreMark on Cortex-M33 Porting Guide* (document [AN12284](#)).

The FlexSPI NOR flash and HyperRAM CoreMark performance are similar to internal flash. There are limitless possibilities to extend the application code size without performance compromise.

6 Revision history

Rev.	Date	Description
0	18 March 2022	Initial release
1	26 May 2022	Replaced LPC553x with LPC553x/LPC55S3x

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