S32G3 Power Estimations
by: NXP Semiconductors

1. Introduction
This application note supports the Power Estimation on S32G3. It describes the basic components and lists the steps to configure and estimate the power consumption on different voltage rails of S32G3.

This document helps enable embedded system designers to gain insights and design energy-efficient automotive gateway applications. It helps the system developer to estimate and design an optimal power supply scheme for their application use case.

The document leverages power consumption data from the device datasheet and additional real measurements or design estimates depending on availability. These estimates are provided “as is” and are not guaranteed within a specified precision. Power consumption depends on electrical parameters, silicon process variations, environmental conditions, and use cases running on the processor during operation. Actual power consumption should be verified in the real and complete system. You must always cross-verify the latest numbers from the device datasheet.
2. Common terms used

**Static consumption** – This is the minimum consumption when the device is powered. It is always present irrespective of any activity.

**Dynamic consumption** – This depends on the activity of the module and must be added to the static consumption to derive total consumption

**S32G3 HDG** – Refers to the S32G3 Hardware design guideline document


3. Attachments with the document

S32G3_PowerEstimator – This sheet provides an estimation of load on various power rails of the PMIC. The details on its usage are covered in section S32G3-PMIC power budgeting.

S32G3_IOpower_estimator – This sheet helps in configuring the IO activity and in estimating the dynamic current for the different IO supply rails. The details on its usage are covered in section **S32G3 IO power estimation**.

4. S32G3 power tree

The S32G3 device has multiple supply pins for the core, I/O, fuses, and, analog supplies. All such pins must be connected to the proper supply voltage for proper operation. NXP recommends using VR5510 and PPF53BDAMMA1ES PMIC in companion mode for S32G3 power requirements. The S32G3 HDG provides further details on power connection recommendations.

The recommended power tree using S32G3, VR5510, and, PPF53BDAMMA1ES is shown below.
When designing an application, the power requirements of the application need to be derived to ensure the functional as well as thermal feasibility of the application. The below sections provides help to the system designer to work out an optimal power topology for their application.

5. S32G3-PMIC power budgeting

Power consumption on 0.8 V rail is the major difference between S32G3 and S32G2. As such an additional regulator (PF5300) is recommended to provide the 0.8 V supply to the S32G3. The PMIC solution of VR5510+PF5300 is capable of meeting S32G3 power requirements. The different power rails are capable of handling different loads and must be used appropriately.

The S32G3_PowerEstimator (see attached) is intended for a quick sanity check of power scheming of S32G3 based applications and to provide an idea of the load on various PMIC power rails. Below are further details on S32G3_PowerEstimator usage.

The ‘S32G3 Silicon Power’ sheet in S32G3_PowerEstimator is filled with inputs from the device datasheet and is used as a reference in the ‘S32G3 Power budget example’ sheet. Since the sheet contains static values from the datasheet, it is not intended to be modified and hence is configured as a protected sheet. The sheet groups the S32G3 supply pins as per the applicable voltage. The sheet only uses max values since these are the ones that need to be taken care of when designing a system.

The ‘S32G3 Power budget example’ sheet is user configurable and can be used to estimate the load on various power rails of the PMIC. The sheet groups power supplies as per PMIC output rails as the constraint on available power comes from the PMIC side. The application designer needs to configure the ‘Conditions’ column from the available drop-down menu wherever applicable. The ‘Power Max’
column accordingly gets updated with the corresponding data referenced from the *S32G3 Silicon Power* sheet.

The *'S32G3 Power Budget example'* sheet can also be observed to see if some of the power rails of the PMIC can be used for supplying power to components other than the S32G3. This sheet already shows examples of adding LPDDR4, QSPI flash, and USB PHY on the PMIC power rails. Power consumption of the additional external components can be accommodated through the ‘Additional components’ rows. The designer must sum up the consumption of external components and provide this as an input in the relevant row. Each of the ‘total’ rows should be reviewed to confirm that the power limits of the PMIC voltage rail outputs are not breached.

Low power mode requirements must also be kept in mind when using this sheet to design the power tree of the system. Refer to S32G3HDG for further details.

In case a user is not using the recommended PMIC solution with S32G3, they can still use this sheet to estimate load and predict any overload condition. The limits on each of the power rails should be updated as per the power solution used.
The S32G3_IOpower_calculator (xlsx attached) can be used to estimate dynamic IO current for the different IO rails. This can then be added to the static power specifications as provided in the device datasheet to estimate the total power on any of the IO rails. There are changes in the static I/O power (refer to the device datasheet) but the dynamic I/O power is same on both the S32G3 and S32G2 devices.
The ‘Overview’ sheet provides a summary of different specified or calculated current parameters and also specifies the IO power estimator use case.

The ‘1.8 V’, ‘3.3 V’, and ‘3.3 VSTB’ sheets detail all the IOs available in respective voltage domains. The green fields in these sheets are modifiable and require you to fill in the inputs as per the activity expected on these IOs. Enabling an IO turns the row blue in the sheet. The dynamic consumption estimate of an IO is calculated based on the activity filled in a row. The total current consumption and total power consumption of all IOs in a VDD domain is calculated and populated at the bottom right of the sheet.

Additionally some of the IOs can be configured for both 1.8 V and 3.3 V operations. These are grouped in ‘dual(VDD_IO_SDHC)’, ‘dual(VDD_IO_GMAC0)’, ‘dual(VDD_IO_GMAC1)’ and ‘dual(VDD_IO_USB)’ sheets. These sheets are also used in a similar way to the fixed voltage sheets. However, these sheets need an additional input in the form of operational voltage which needs to be filled at the bottom left of the sheet. The total power consumption is accordingly calculated in the sheet.
7. Additional considerations

7.1. Power impact for unused module

A system use case may not require each of the components powered by the 0.8 V supply. In such cases, the additional granularity may be required to find the reduced consumption on the respective power rail. The S23G3 does not offer power gating of modules, but there is the possibility to clock gate certain modules using the MC_ME. This means that the dynamic component of the power consumption for these modules would be saved when not using them. Below are the estimates for major modules on 0.8V rail based on module running at full speed with Tj as 125°C.

Table 1 Module power estimates

<table>
<thead>
<tr>
<th>Core / Module</th>
<th>Dynamic Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A53 Cluster (4 cores active – 1 GHz)</td>
<td>385</td>
</tr>
<tr>
<td>A53 Cluster (4 cores active – 1.3 GHz)</td>
<td>500</td>
</tr>
<tr>
<td>A53 Cluster (2 cores active – 1.3 GHz)</td>
<td>328</td>
</tr>
<tr>
<td>A53 Cluster (1 core active – 1.3GHz)</td>
<td>242</td>
</tr>
<tr>
<td>M7 Cluster (1 lock step instance)</td>
<td>51</td>
</tr>
<tr>
<td>DRAM Controller</td>
<td>473</td>
</tr>
<tr>
<td>PFE</td>
<td>165</td>
</tr>
</tbody>
</table>
### Additional considerations

<table>
<thead>
<tr>
<th>Core / Module</th>
<th>Dynamic Power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LLCE</td>
<td>27</td>
</tr>
<tr>
<td>PCIe (per module)</td>
<td>82</td>
</tr>
</tbody>
</table>

It should be noted here that the figures provided in the above table are design estimates based on simulations only. As such these should only be used for guidance purpose and must not be treated as a specification. These values are for the VDD domain only and do not take into consideration any analog or I/O impact of the module. These should be calculated separately. The power consumption for cores take into account the core/cluster only and do not account for the corresponding savings in traffic across the bus fabric etc.

#### 7.2. Power impact for reduced operation frequency

The impact of operational frequency on dynamic power should be assumed to be linear for further estimation. For example, if one Cortex-A53® core running at 1.3 GHz is estimated to consume ~90 mW then the same cluster when run at 650 MHz would consume ~45 mW.

#### 7.3. Power profile with temperature

The power consumption of a module can be broadly divided into dynamic and static consumption. The dynamic component remains stable across temperature, however the static consumption varies with temperature. The graph below shows the leakage power (static component) on the 0.8 V VDD power domain across temperature for a device taken from the worst case leakage corner of the process. The graph is derived from limited bench experiments and hence should be taken only for guidance and should not be treated as a specification. The power shown in the below graph is for the 0.8 V VDD domain only and does not take into consideration any analog or I/O leakage power.
8. References

S32G3 Hardware Design Guidelines (S32G3HDG)
S32G3 Reference Manual
S32G3 Datasheet
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