### Document information

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<tr>
<td>Keywords</td>
<td>AN14110, i.MX 93, FlexIO, iMX93EVK</td>
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<tr>
<td>Abstract</td>
<td>This document describes the emulation of I2C with the FlexIO module of i.MX 93 device based on different operating systems, such as Linux, BareMetal, and Zephyr.</td>
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</table>
1 Introduction

Flexible input/output (FlexIO) is a highly configurable module, which is capable of emulating a wide range of communication protocols, such as UART, I2C, SPI, and I2S. FlexIO was originally exclusive to NXP MCU products. However, due to its ability to emulate various interfaces easily, it has now been ported to various MPU platforms, such as i.MX 93.

In this document, the FlexIO emulation of the I2C bus master is taken as an example to introduce a new module in MPU. It covers the basic principles, hardware implementation, and the software implementation in different operating systems, such as Linux, BareMetal, and Zephyr.

2 FlexIO module overview

The i.MX 93 SoC features two FlexIO instances. Figure 1 shows a high-level overview of the FlexIO module. The rich resources of shifters, counters, and pins make the module work with different functionalities.

![FlexIO block diagram](image)

Figure 1. FlexIO block diagram

The hardware resources in the FlexIO module are:
• 32-bit shifter x 8
• 16-bit timer x 8
• Pin x 32

Shifter operations:
• Transmit mode
• Receive mode
• Match Store mode
• Match Continuous mode
• State mode
• Logic mode

Timer operations:
• Timer 8-bit Baud Counter mode
• Timer 8-bit High PWM mode
• Timer 16-bit Counter mode
• Timer 16-bit Counter Disable mode
• Timer 8-bit Word Counter mode
• Timer 8-bit Low PWM mode
• Timer 16-bit Input Capture mode

Pin operations:
• Parallel interface
• Pin synchronization
• Pin override
• Pin interrupt

3 Emulating I2C bus master

This section describes how to emulate the I2C bus master with FlexIO. For this application, the NXP i.MX 93 11x11 EVK FlexIO emulates an I2C interface to communicate with the NXP USB PD PHY IC PTN5110NHQZ.

3.1 General description

I2C controller mode can be supported using two timers, two shifters, and two pins. One timer is used to generate the SCL output and another timer is used to control the shifters. The two shifters are used to transmit and receive each word. When receiving, the transmitter must transmit FFh to the 3-state output. FlexIO inserts a stop bit after every word to generate and verify the ACK or NACK.
The detailed configurations and usage information are provided in the following sections.

3.2 Configuration

This section provides detailed configurations of the shifters and timers.

NOTE

The items listed in this section are the initial settings of the shifters and timers. The software updates some of these settings according to the transmissions.

- Shifter 0 is used as the transmitter. Shifter 1 is used as the receiver. They have the following initial configurations.
Table 1. Configurations for Shifter 0 and Shifter 1

<table>
<thead>
<tr>
<th>Items</th>
<th>Shifter 0 configurations</th>
<th>Shifter 1 configurations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Shifter mode</td>
<td>Transmit</td>
<td>Receive</td>
</tr>
<tr>
<td>Timer selection</td>
<td>Timer 1</td>
<td>Timer 1</td>
</tr>
<tr>
<td>Timer polarity</td>
<td>On posedge of shift clock</td>
<td>On negedge of shift clock</td>
</tr>
<tr>
<td>Pin selection</td>
<td>Pin 28</td>
<td>Pin 28</td>
</tr>
<tr>
<td>Pin configuration</td>
<td>Open-drain or bidirectional output enable</td>
<td>Output disabled</td>
</tr>
<tr>
<td>Pin polarity</td>
<td>Active low</td>
<td>Active high</td>
</tr>
<tr>
<td>Input source</td>
<td>From pin</td>
<td>From pin</td>
</tr>
<tr>
<td>Start bit</td>
<td>Value 0</td>
<td>Disabled</td>
</tr>
<tr>
<td>Stop bit</td>
<td>Value 1</td>
<td>Value 0</td>
</tr>
<tr>
<td>Buffer used</td>
<td>Bit Byte Swapped register</td>
<td>Bit Byte Swapped register</td>
</tr>
</tbody>
</table>

• Timer 0 is used to generate SCL output and to trigger timer 1. Timer 1 is used to control the Shifter 0 and Shifter 1.

Table 2. Configurations for Timer 0 and Timer 1

<table>
<thead>
<tr>
<th>Items</th>
<th>Timer 0 configurations</th>
<th>Timer 1 configurations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer mode</td>
<td>Dual 8-bit baud/bit mode</td>
<td>Single 16-bit counter mode</td>
</tr>
<tr>
<td>Trigger selection</td>
<td>Shifter 0 status flag</td>
<td>Shifter 0 status flag</td>
</tr>
<tr>
<td>Trigger polarity</td>
<td>Active low</td>
<td>Active low</td>
</tr>
<tr>
<td>Trigger source</td>
<td>Internal</td>
<td>Internal</td>
</tr>
<tr>
<td>Pin selection</td>
<td>Pin 29</td>
<td>Pin 29</td>
</tr>
<tr>
<td>Pin configuration</td>
<td>Open-drain or bidirectional output enable</td>
<td>Output disabled</td>
</tr>
<tr>
<td>Pin polarity</td>
<td>Active high</td>
<td>Active low</td>
</tr>
<tr>
<td>Timer initial output</td>
<td>Output logic 0 when enabled and not affected by timer reset</td>
<td>Output logic 1 when enabled and not affected by timer reset</td>
</tr>
<tr>
<td>Timer decrement source</td>
<td>Decrement counter on FlexIO clock. Shift clock equals timer output</td>
<td>Decrement counter on pin input (both edges). Shift clock equals pin input.</td>
</tr>
<tr>
<td>Timer enable condition</td>
<td>On Trigger high</td>
<td>On timer 0 enable</td>
</tr>
<tr>
<td>Timer disable condition</td>
<td>On timer compare (upper 8 bits match and decrement)</td>
<td>On timer 0 disable</td>
</tr>
<tr>
<td>Timer reset condition</td>
<td>On timer pin equal to timer output</td>
<td>Never reset</td>
</tr>
<tr>
<td>Start bit</td>
<td>Enabled</td>
<td>Enabled</td>
</tr>
<tr>
<td>Stop bit</td>
<td>Enabled on timer disable</td>
<td>Enabled on timer compare</td>
</tr>
<tr>
<td>Timer compare value</td>
<td>(((N^9+1)*2-1)&lt;&lt;8)</td>
<td>(8\times2-1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\text{&quot;8&quot; means the number bits in a single frame})</td>
</tr>
</tbody>
</table>
3.3 Hardware design

By default, the i.MX 93 Evaluation Kit (EVK) configures PTN5110NHQZ using LPI2C3. However, GPIO_IO28 and GPIO_IO29 can be muxed as two FlexIO pins. You can test the FlexIO emulation of I2C without any hardware rework. Figure 3 shows the related parts of the schematic.

<table>
<thead>
<tr>
<th>iOPAD</th>
<th>Alt1</th>
<th>Alt7</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPIO_IO28</td>
<td>i2c3.SDA</td>
<td>flexio1.FLEXIO[28]</td>
</tr>
<tr>
<td>GPIO_IO29</td>
<td>i2c3.SCL</td>
<td>flexio1.FLEXIO[29]</td>
</tr>
</tbody>
</table>

Table 3. IOMUX of I2C Pins

3.4 Software implement

This section describes the software implementation as per the following:
• Implementation based on Linux with A55
• Implementation in SDK with M33

3.4.1 Linux with A55

This section describes the software implementation based on Linux L6.1.36_2.1.0. The kernel driver can be divided into two parts. The multifunction driver (MFD) is applied as the FlexIO core driver. FlexIO I2C master driver node is the child node of the core driver node.

```plaintext
## kernel driver files
include/linux/mfd/imx-flexio.h
drivers/mfd/imx-flexio.c //compatible = "nxp,imx-flexio"
drivers/i2c/busses/i2c-flexio.c //compatible = "nxp,imx-flexio-i2c-master"
```

The dts file below is a merge of the following two files: arch/arm64/boot/dts/freescale/imx93.dtsi and arch/arm64/boot/dts/freescale/imx93-11x11-evk-flexio-i2c.dts

```plaintext
## dts
/
aliases {
i2c8 = &flexio_i2c;
};

&lpi2c3 {
    status = "disabled";
    /delete-node/ tcpc@51;
};

flexio1: flexio@425c0000 {
    #address-cells = <1>;
    #size-cells = <1>;
    compatible = "nxp,imx-flexio";
    reg = <0x425c0000 0x10000>;
    interrupts = <GIC_SPI 53 IRQ_TYPE_LEVEL_HIGH>;
    clocks = <&clk IMX93_CLK_FLEXIO1_GATE>,
        <&clk IMX93_CLK_FLEXIO1_GATE>;
    clock-names = "per", "ipg";
    assigned-clocks = <&clk IMX93_CLK_FLEXIO1_GATE>;
    assigned-clock-parents = <&clk IMX93_CLK_FLEXIO1>;
    assigned-clock-rates = <24000000>;
    status = "okay";
}

flexio_i2c: i2c-master {
    #address-cells = <1>;
    #size-cells = <0>;
    compatible = "nxp,imx-flexio-i2c-master";
    clock-frequency = <1000000>;
    pinctrl-names = "default", "sleep";
    pinctrl-0 = <&pinctrl_flexio_i2c_master>;
    pinctrl-1 = <&pinctrl_flexio_i2c_master>;
    sda = /bits/ 8 <28>;
    scl = /bits/ 8 <29>;
    status = "okay";
};
```
In the FlexIO core driver imx-flexio.c, some basic setup functions are implemented. When more interfaces are implemented with FlexIO, more functions can be added to work as common codes.

### Table 4. ICore functions of FlexIO

<table>
<thead>
<tr>
<th>Register</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>FlexIO Control Register (CTRL)</td>
<td>void flexio_sw_reset(void *base, unsigned int reg); void flexio_get_default_ctrl(struct flexio_control *ctl); void flexio_setup_ctrl(void *base, struct flexio_control *ctl, unsigned int reg);</td>
</tr>
<tr>
<td>Shifter Control N register</td>
<td>void flexio_setup_shiftctl(void *base, struct flexio_shifter_control *ctl, unsigned int reg);</td>
</tr>
<tr>
<td>Shifter Configuration N register</td>
<td>void flexio_setup_shiftcfg(void *base, struct flexio_shifter_config *cfg, unsigned int reg);</td>
</tr>
<tr>
<td>Timer Control N register</td>
<td>void flexio_setup_timerctl(void *base, struct flexio_timer_control *ctl, unsigned int reg);</td>
</tr>
<tr>
<td>Timer Configuration N register</td>
<td>void flexio_setup_timercfg(void *base, struct flexio_timer_config *cfg, unsigned int reg);</td>
</tr>
</tbody>
</table>

In the FlexIO I2C master driver, the most configurations in Section 3.2 are done in `imx_flexio_init_hardware()`. The driver behavior is described with `i2c_adapter` and `i2c_algorithm` since the I2C subsystem framework is applied.

```c
struct i2c_algorithm {
    int (*master_xfer)(struct i2c_adapter *adap, struct i2c_msg *msgs, int num);
    ....
};
```

```c
static int imx_flexio_i2c_master_xfer(struct i2c_adapter *adap, struct i2c_msg *msgs[], int num);
```

--> //one more byte is slave addr, only 1 bit for STOP/Repeated START
xfer_len = msg->len + 1;

--> //Max bytes is 14 because high 8bit of TIMCMP can only reach 255. 10*N + 1 < 255, so N <=14
setup_xfer_count(i2c_dev, xfer_len);

--> //Write or read according to the xfer_msg flag
i2c_master_write or i2c_master_read

Then another important function is the interrupt processing function of FlexIO, which is the key part of the driver.

```c
static irqreturn_t imx_flexio_i2c_isr(int irq, void *dev_id);
```

--> //Responsible for writing date and sending ack signal
if (shiftstat & TRANSMIT_STAT) {

--> //Responsible for reading date and checking ack signal
if (shiftstat & RECEIVE_STAT) {

```
The specific process of ISR is complicated. For details, refer to FlexIO I2C driver in BSP release.

Once the FlexIO I2C driver is ready, it can be used as a common I2C driver. The proper I2C device nodes can be added into the device tree as follows.

```c
&flexio_i2c {
    ptn5110_2: tcpc@51 {
        _compatible = "nxp,ptn5110";
        reg = <0x51>;
        interrupt-parent = <&gpio3>;
        interrupts = <27 IRQ_TYPE_LEVEL_LOW>;
        status = "okay";
        ....
    }
};
```

### 3.4.2 BareMetal with M33

This section describes the software implementation in SDK with M33 running. The driver can be divided into two parts, one is the FlexIO core driver and the other is the interface driver for specific cases.

#### driver files
- `devices/MIMX9352/drivers/fsl_flexio.h`
- `devices/MIMX9352/drivers/fsl_flexio.c`
- `devices/MIMX9352/drivers/fsl_flexio_i2c_master.h`
- `devices/MIMX9352/drivers/fsl_flexio_i2c_master.c`
- `boards/mcimx93evk/driver_examples/flexio/i2c/read_accel_value_transfer`

The demo `read_accel_value_transfer` is trying to read the registers of IMU. To be aligned with the case in Linux, the pinmux configuration is changed and the P TN5110 read function is added as follows.

```c
IOMUXC_SetPinMux(IOMUXC_PAD_GPIO_IO29__FLEXIO1_FLEXIO29, 1U);
IOMUXC_SetPinConfig(IOMUXC_PAD_GPIO_IO29__FLEXIO1_FLEXIO29, IOMUXC_PAD_DSE(15U)
| IOMUXC_PAD_FSEL1(2U) | IOMUXC_PAD_OD_MASK);
IOMUXC_SetPinMux(IOMUXC_PAD_GPIO_IO28__FLEXIO1_FLEXIO28, 1U);
IOMUXC_SetPinConfig(IOMUXC_PAD_GPIO_IO28__FLEXIO1_FLEXIO28, IOMUXC_PAD_DSE(15U)
| IOMUXC_PAD_FSEL1(2U) | IOMUXC_PAD_OD_MASK);

static bool I2C_example_read_PTN5110_VENDOR_ID(void) {
    uint16_t vendor_id  = 0x00;
    uint8_t i           = 0;
    uint32_t j          = 0;

    flexio_i2c_master_config_t masterConfig;

    FLEXIO_I2C_MasterGetDefaultConfig(&masterConfig);
    masterConfig.baudRate_Bps = I2C_BAUDRATE;

    if (FLEXIO_I2C_MasterInit(&i2cDev, &masterConfig, FLEXIO_CLOCK_FREQUENCY) != kStatus_Success) {
        PRINTF("FlexIO clock frequency exceeded upper range. \r\n");
    }
}
```
return false;
}

FLEXIO_I2C_MasterTransferCreateHandle(&i2cDev, &g_m_handle,
flexio_i2c_master_callback, NULL);

flexio_i2c_master_transfer_t masterXfer;
memset(&masterXfer, 0, sizeof(masterXfer));
masterXfer.slaveAddress = 0x51;
masterXfer.direction = kFLEXIO_I2C_Read;
masterXfer.subaddress = 0x00;
masterXfer.subaddressSize = 1;
masterXfer.data = (uint8_t *)&vendor_id;
masterXfer.dataSize = 2;

for (i = 0; i < 127; i++)
{
    completionFlag = false;
    FLEXIO_I2C_MasterTransferNonBlocking(&i2cDev, &g_m_handle, &masterXfer);
    /* wait for transfer completed. */
    while ((nakFlag == false) && (completionFlag == false))
    {
    }
    if (nakFlag == true)
    {
        nakFlag = false;
        for (j = 0; j < 0x1FFF; j++)
        {
            __NOP();
        }
    }
    if (completionFlag == true)
    {
        PRINTF("The Vendor ID is 0x%x\r\n", vendor_id);
    }
    else
    {
        PRINTF("Failed to Get the Vendor ID\r\n");
    }
    for (j = 0; j < 0xFFF; j++)
    {
        __NOP();
    }
    return 0;
}

### 3.4.3 Zephyr with A55

This section describes the software implementation in Zephyr OS running on A55. The driver can be divided into two parts—one is the FlexIO core driver and the other is the interface driver for specific cases. The FlexIO core driver and I2C drivers of Zephyr are not available in the current release. To add the support of FlexIO I2C
in Zephyr, see the patch file in Attachments. Zephyr has a Linux code style but sometimes works together with the SDK.

```c
## driver files
drivers/i2c/i2c_mcux_flexio.h
drivers/i2c/i2c_mcux_flexio.c
drivers/misc/mcux_flexio/mcux_flexio.h
drivers/misc/mcux_flexio/mcux_flexio.c

## dts:
flexio1: flexio@425c0000 {
    compatible = "nxp,imx-flexio";
    #address-cells = <1>;
    #size-cells = <0>;
    reg = <0x425c0000 0x10000>;
    interrupts = <GIC_SPI S3 IRQ_TYPE_LEVEL IRQ_DEFAULT_PRIORITY>;
    interrupt-parent = <&gic>;
    clocks = <&ccm IMX_CCM_FLEXIO1_CLK 0x70 12>;
    status = "disabled";
};

&pinctrl {
    pinmux_flexio1_i2c: pinmux_flexio1_i2c {
        group0 {
            pinmux =
                <&iomuxc1_gpio_io28_flexio_flexio_flexio1_flexio28>, /* SDA */
                <&iomuxc1_gpio_io29_flexio_flexio_flexio1_flexio29>; /* SCL */
            drive-open-drain;
            bias-pull-up;
            slew-rate = "fast";
            drive-strength = "x4";
        }
    }
};

&flexio1 {
    status = "okay";

    flexio1_i2c: flexio1_i2c {
        compatible = "nxp,imx-flexio-i2c-master";
        status = "okay";
        clock-frequency = <I2C_BITRATE_STANDARD>;
        #address-cells = <1>;
        #size-cells = <0>;
        pinctrl-0 = <&pinmux_flexio1_i2c>;
        pinctrl-names = "default";
        sda-pin = <28>;
        scl-pin = <29>;
        shifters = <0 1>;
        timers = <0 1 2>;
    }
};

The function \texttt{i2c_mcux_flexio_transfer} deals with the process of I2C scan, read, and write. Even if it runs in A55 cores, the drivers in the SDK that are named as hal are performing as the key parts.

```c
static int i2c_mcux_flexio_transfer(const struct device *dev, struct i2c_msg *msgs,
```
```c
uint8_t num_msgs, uint16_t addr) {
    ... 
    /* Iterate over all the messages */
    for (int i = 0; i < num_msgs; i++) {
        ...
        transfer.slaveAddress = addr;
        transfer.direction = (msgs->flags & I2C_MSG_READ)
            ? kFLEXIO_I2C_Read : kFLEXIO_I2C_Write;
        transfer.subaddress = 0;
        transfer.subaddressSize = 0;
        transfer.data = msgs->buf;
        transfer.dataSize = msgs->len;
        /* Start the transfer */
        status = FLEXIO_I2C_MasterTransferNonBlocking(config->flexio_i2c,
            &data->handle, &transfer);
        ...
        if (msgs->len == 0) {
            if (kFLEXIO_I2C_ReceiveNakFlag & FLEXIO_I2C_MasterGetStatusFlags(config->
                flexio_i2c)) {
                FLEXIO_I2C_MasterTransferAbort(config->flexio_i2c, &data->handle);
                ret = -EIO;
                break;
            }
        } /* Move to the next message */
        msgs++;
    }
    ...}
```

### 3.5 Running the test

Consider PTN5110 as an example, which is mounted on LPI2C3 by default. The same pins are configured to be FlexIO pins with no hardware rework. Table 5 describes the test that keeps reading the VENDOR_ID and should get the default value as “0x1FC9”.

<table>
<thead>
<tr>
<th>Group</th>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Default value</th>
<th>Bit field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Identification</td>
<td>00h</td>
<td>VENDOR_ID</td>
<td>read-only word</td>
<td>0x1FC9</td>
<td>15:0</td>
<td>Vendor ID A unique 16-bit unsigned integer. Assigned by the USB-IF to the vendor.</td>
</tr>
</tbody>
</table>
3.5.1 Linux with A55

Since the FlexIO I2C driver conforms to the I2C subsystem software framework, it can be tested as a common I2C master or slave device. To get the VENDOR_ID of PTN5110, use the `i2cdetect/i2ctransfer` command in Linux as shown in Figure 4.

![Figure 4. VENDOR_ID of PTN5110 in Linux with A55](image)

It can be found that the register VENDOR_ID is already received. However, if the command is called frequently, communication failures may occasionally occur. This issue is caused by untimely interrupt response and handling. The same case is also tested in a Linux-RT environment, but gets a little better result. The error rate increases significantly with the increase of CPU loading.

3.5.2 BareMetal on M33

FlexIO has been widely used in MCU before, and its real time and emulation stability are reliable. The test in this section runs on the M33 core of i.MX 93.
3.5.3 Zephyr on A55

Similar to Linux, Zephyr can use commands such as `i2c scan/read/write` to operate I2C devices conveniently. No errors are found during the test process.
4 Conclusion

FlexIO can be emulated as the I2C master in different operating systems. However, it is not recommended to use FlexIO I2C in a Linux environment directly. Some check mechanisms should be applied to make sure the read or write operation is executed correctly in the Linux environment. Linux is not an RTOS, which means it cannot guarantee the interrupt latency or interrupt responding time. Linux may generate big interrupt latency while FlexIO IP can only tolerate small interrupt latency.

In a BareMetal or RTOS environment, such as Zephyr, FlexIO can work normally as expected. Another optional plan is planned in the future. A core could request M core to perform FlexIO I2C communication through RPMsg, making full use of the real-time capabilities of M core.

5 References

Table 6 lists the resources that can be referred for more information.

<table>
<thead>
<tr>
<th>Resource</th>
<th>Link/how to access</th>
</tr>
</thead>
<tbody>
<tr>
<td>i.MX 93 Applications Processor Reference Manual</td>
<td>IMX93RM</td>
</tr>
<tr>
<td>Emulating I2C Bus Master by using FlexIO Application Note</td>
<td>AN5133</td>
</tr>
</tbody>
</table>

6 Acronym

Table 7 lists and defines the acronyms used in this document.

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>FlexIO</td>
<td>Flexible input/output</td>
</tr>
<tr>
<td>I2C</td>
<td>Inter-integrated circuit</td>
</tr>
<tr>
<td>I2S</td>
<td>Inter-IC sound</td>
</tr>
<tr>
<td>OSI</td>
<td>Open systems interconnection</td>
</tr>
<tr>
<td>PHY</td>
<td>Physical interface of the OSI model</td>
</tr>
<tr>
<td>PWM</td>
<td>Pulse width modulation</td>
</tr>
<tr>
<td>RTOS</td>
<td>Real-time operating system</td>
</tr>
</tbody>
</table>
Table 7. Acronyms...continued

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>SDK</td>
<td>Software development kit</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial peripheral interface</td>
</tr>
<tr>
<td>UART</td>
<td>Universal asynchronous receiver transmitter</td>
</tr>
</tbody>
</table>

7 Note about the source code in the document

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8 Revision history

Table 8 summariz...
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