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Current Sensing Techniques in Motor Control Applications

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Document information

Information	Content
Keywords	Current sensing, sensing techniques, motor control
Abstract	There are many ways of current measurement in motor control or power electronics applications. Moreover, electrical current can be measured with different sensor types. The selection of appropriate current sensors together with appropriate current sensing strategy is therefore a complex issue. System requirements need to be analyzed and appropriate current sensor and sensing technique need to be selected. This document focuses on current sensors based on Ohm's law and low-side or DC Bus current sensing approach.

1 Introduction

Measurement of current is an essential process in every power electronics system. Measured current signals can be processed for monitoring purposes in less complex systems or can be processed to suit control purposes in complex and more sophisticated systems.

There are many ways of current measurement in power electronics applications. Moreover, electrical current can be measured with different sensor types. The selection of appropriate current sensors together with the appropriate current sensing strategy is therefore a complex issue. System requirements need to be analyzed and appropriate current sensor and sensing techniques need to be selected.

2 Current sensors

Electric current represents one of the most important and high dynamic feedback signals in motor control applications. Current feedback accuracy is crucial for current control loop and observers. Current sensors work based on specific physical laws and can be categorized as follows:

- Current sensors based on Ohm’s law.
- Current sensors based on Faraday’s law.
- Current sensors based on electromagnetic field laws.
- Current sensors based on the Faraday effect.

The current sensing technique in the power electronic systems can be categorized according to the placement of the current sensor in the power path:

- High-side current sensing approach.
- Low-side current sensing approach.
- Phase current sensing approach.
- DC bus current sensing approach.

This document focuses on current sensors based on Ohm’s law and low-side or DC bus current sensing approach.

3 Current sensing techniques based on Ohm’s law

Current sensors based on Ohm’s law are called shunt resistors. These sensors are widely used in many application domains, especially in automotive, due to their cost and simplicity benefits. They allow to sense DC and AC current, sense current bidirectionally and cope well with high dynamic currents.

Shunt resistors are connected to power circuitry in series. Their nominal resistance is relatively small, typically around several milliohms. Higher resistance is not recommended due to additional power losses. The low nominal resistance of the shunt resistor brings challenges with the signal/noise ratio. Therefore, there is always a trade-off between power loss reduction and the signal/noise ratio. The voltage drop over the shunt resistor is low and usually does not have a noticeable impact on the performance of the connected motor. In applications comprising an analog-to-digital converter (ADC), the current signal (shunt resistor voltage drop) must be further processed by the conditioning circuitry. This voltage drop is amplified to the range of ADC. The current signal in the form of voltage drop is linear dependent on the current flowing through the shunt resistor.

Benefits of such sensors are low cost, simplicity, stability, and linearity.

4 Low-side current sensing

In the case of low-side current sensing, shunt resistors are connected between low-side transistors and a negative DC bus terminal.

There are two low-side current sensing techniques available:

- Triple-shunt
- Dual-shunt

4.1 Triple-shunt

Triple-shunt current sensing technique employs a current sensing resistor in each phase leg of a power inverter.

Figure 1 depicts schematic of power inverter using low-side triple-shunt current sensing approach and waveforms of duty cycles, phase currents, and currents flowing through shunt resistors. Shunt resistors R_A, R_B, R_C are inserted between the respective low-side transistor (T_2, T_4, T_6) and the negative DC link terminal. The current flowing through the motor windings and subsequently through the low-side transistors and shunt resistors creates a voltage drop across these shunt resistors. The voltage drop is proportional to the current according to:

$$V_{A,B,C} = R_{A,B,C} i_{RA,RB,RC} \quad (1)$$

The voltage drop across the shunt resistors is further processed by differential operational amplifiers (OP amps) and amplified to exploit the range of the ADC best. The current flowing through the shunt resistor is then calculated in the software (SW) based on Equation 1.

ON/OFF states of the transistors, motor phase currents, and shunt resistor currents are illustrated in Figure 1. It is obvious that the shunt resistor current is equal to the motor phase current only if the respective low-side transistor is switched on, that is: current $i_{RA,RB,RC}$ readings are valid only if low-side transistors $T_{2,4,6}$ are switched on. Therefore, the current measurement (ADC conversion) and pulse-width modulation (PWM) switching algorithm need to be synchronized.

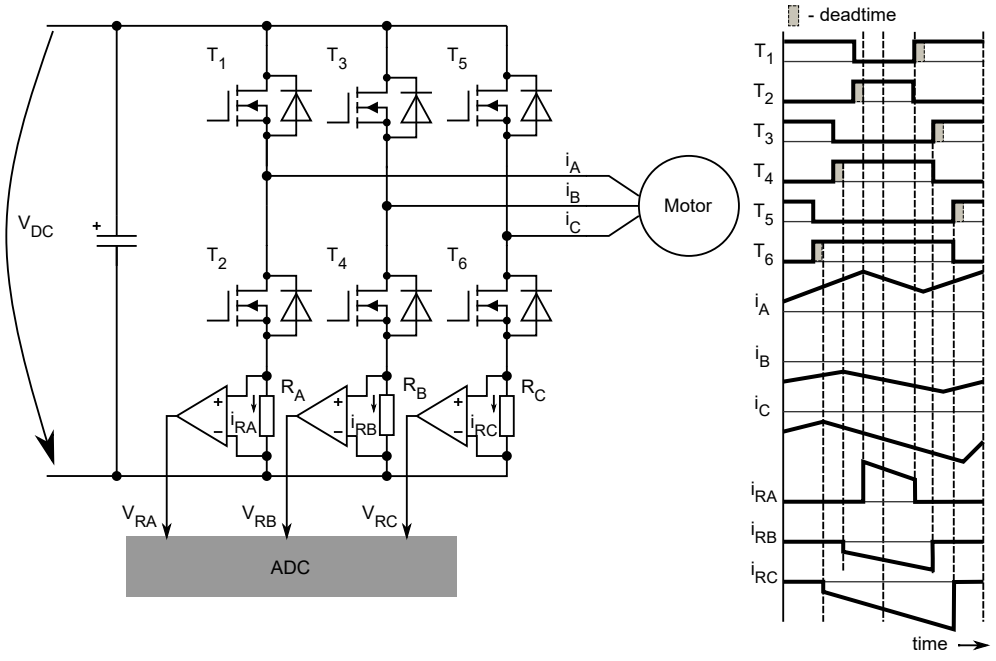

Figure 1. Low-side triple-shunt current sensing technique – principal topology, switching states and current waveforms during one PWM period

The synchronization not only needs to consider the switching states of the transistors, but also the conversion time of the ADC needs to be considered. If the low-side transistor is opened for a time period shorter than the ADC conversion time, the current reading will be inaccurate. Moreover, the current reading needs to be done in steady state to avoid transients and disturbances caused by transistor switching.

The ADC conversion events, PWM algorithm and their synchronization are explained in Figure 2, where duty cycle waveforms and switching patterns of space vector modulation (SVM) technique are shown. SVM is commonly used in modern electric drives. It is based on center-aligned PWM patterns, which allow to measure average motor currents (per PWM cycle) easily.

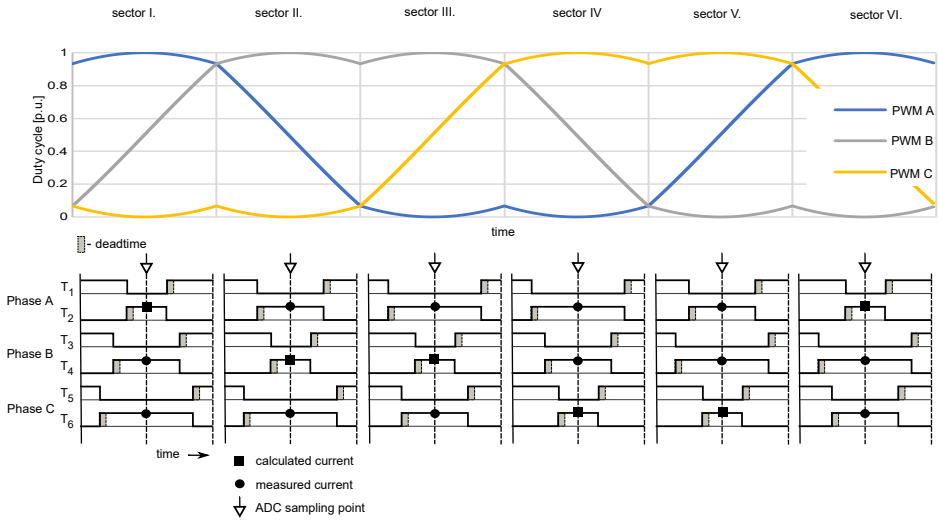

Figure 2. Triple-shunt - SVM duty cycle waveforms and switching states examples

The inverter topology shown in Figure 1 is assumed. Current samples are taken in the middle of the PWM period. The average PWM period current value can be measured in this manner. The currents are obtained simultaneously in all 3 phases, that assures the current feedback to the motor controller is in accordance with real-time motor behavior. (As Park, Clarke transformations, observers/estimators, and current controllers need simultaneous phase current readings in order to produce accurate results).

Observe that in the middle of each sector the duty cycle of one of the phases reaches 100% (provided there is max. DC Bus voltage utilization). In such a case it is impossible to measure the phase current as the low-side transistor will be open (and the high-side transistor closed) throughout the whole PWM period. Therefore, valid current measurements of the corresponding phase cannot be obtained during certain periods of the respective sector duration. Due to this reason, two of the phase currents are measured and the remaining current (which reaches 100% duty cycle) is calculated based on the assumption of symmetrical inverter load (which is fulfilled by a 3-phase motor under normal operating conditions):

$$i_a + i_b + i_c = 0 \tag{2}$$

The calculated and measured current values are acquired in the corresponding SVM sectors according to Table 1. In each sector two phase currents are measured and the remaining current is calculated.

Table 1. Phase currents acquisition vs SVM sector

SVM sector	1	2	3	4	5	6
Phase A current	$i_a = -i_b - i_c$	measured	measured	measured	measured	$i_a = -i_b - i_c$
Phase B current	measured	$i_b = -i_a - i_c$	$i_b = -i_a - i_c$	measured	measured	measured
Phase C current	measured	measured	measured	$i_c = -i_a - i_b$	$i_c = -i_a - i_b$	measured

This approach does allow full DC Bus voltage utilization and requires only 2 ADC modules to obtain motor currents simultaneously. Since in each sector 2 currents are measured (the third one is calculated), one ADC module per measured current is necessary for their simultaneous A/D conversion. It is also possible to achieve redundancy for current measurement. In that case, the full utilization of DC Bus needs to be sacrificed in exchange for having the current sensing circuit in one phase available as a backup if one of the remaining

current sensing circuits should fail. In that case, the setup is operated as a dual-shunt and if a failure occurs then the current reading is taken from the backup current sensing circuitry.

The disadvantage of the triple-shunt method is its higher cost because the shunt resistor and the OP amp conditioning circuitry in each phase is necessary.

4.2 Dual-shunt

The higher cost disadvantage of the triple-shunt method can be dealt with by using Equation 2. If two-phase currents are measured (for example, i_a and i_b) throughout all SVM sectors and the remaining current (i_c) is calculated, then only 2 shunt resistors and 2 OP amp circuits are necessary. The resulting topology is illustrated in Figure 3.

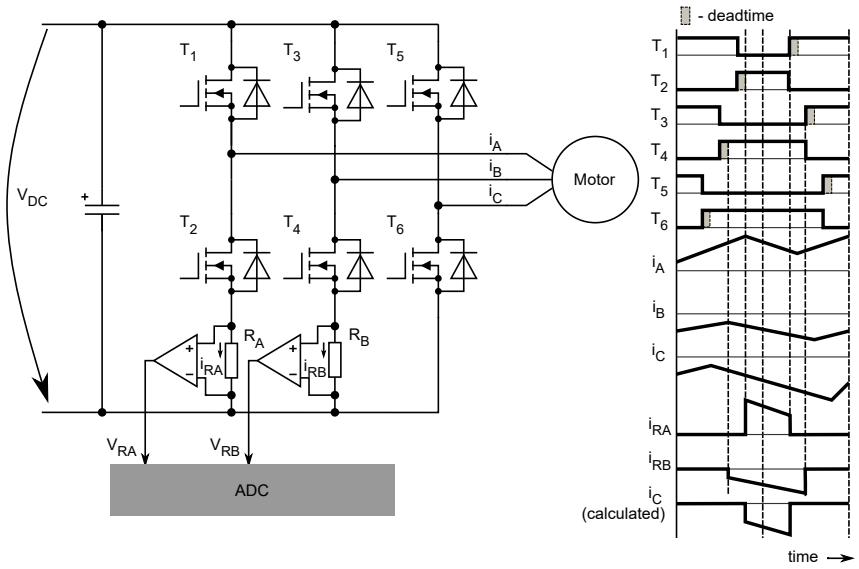

Figure 3. Low-side dual-shunt current sensing technique – principal topology, switching states and current waveforms during one PWM period

As explained in the chapter 4.1 and Figure 2 , in case of full DC Bus voltage utilization (operation with 100% peak duty cycle) there is always one phase per sector, where current cannot be measured. As there is now no option to select in which two phases the current is to be measured (dual-shunt configuration), the required output voltage amplitude (that is, duty cycle) has to be limited. The duty cycle limit needs to be set in a way that the low-side transistor minimum ON time is longer than ADC conversion time. Since we consider symmetrical PWM pattern and measurement in the middle of the PWM period, the minimum low-side transistor ON time needs to be equal or larger than 2*ADC conversion time (in a real system also transient settling and deadtime need to be considered). The situation is depicted in Figure 4.

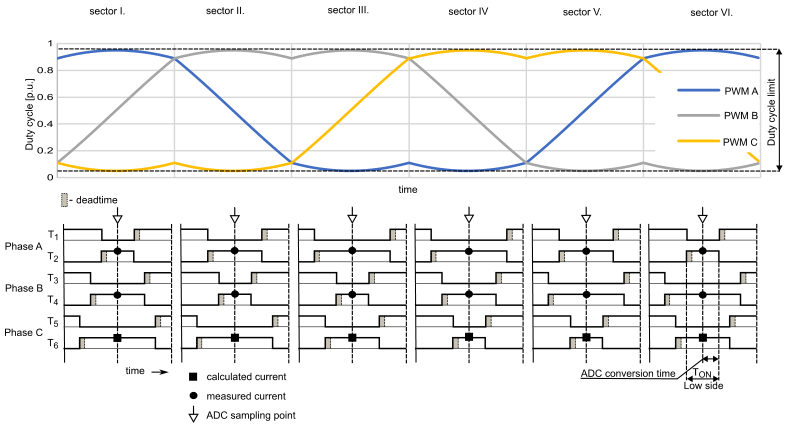

Figure 4. Dual-shunt - SVM duty cycle waveforms and switching states examples

As mentioned earlier, the advantage of this method compared to triple-shunt is the bill of material reduction but at the cost of DC Bus voltage not being fully utilized.

5 DC Bus current sensing – single shunt

5.1 DC bus current sensing – phase current reconstruction

If measuring the DC Bus current, the shunt resistor needs to be placed in series with the negative pole of the DC Bus. The method is shown in Figure 5.

This method is called single-shunt and relies upon the fact that while there is a switching combination in the inverter corresponding to an active vector, the DC Bus current is equal to one of the motor phase currents or its inverted value (depending on the active vector).

This statement is explained in Figure 6. In the middle of the picture there are the active voltage vectors available (each vector is pointing at its physical representation in the inverter - schematic with corresponding switching combination). For each switching combination there is a DC Bus current either flowing to one motor phase and flowing out of the remaining two phases or vice versa. By applying 1st Kirchhoff's law, the DC Bus current is equal to the current of the phase, which has an opposite direction than the currents of the remaining phases. If the current of this phase flows to the motor, then it is equal to the DC Bus current, if it flows from the motor then its inverted value is equal to the DC Bus current.

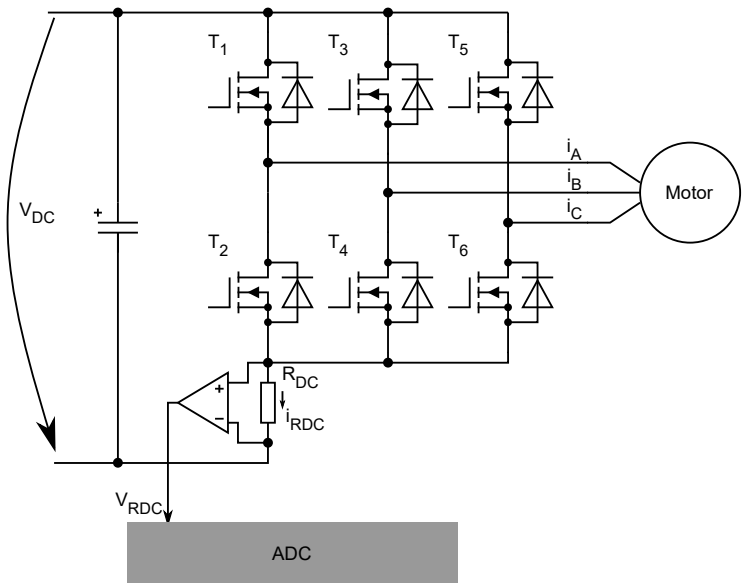

Figure 5. Single-shunt current sensing (DC Bus current sensing) principal topology

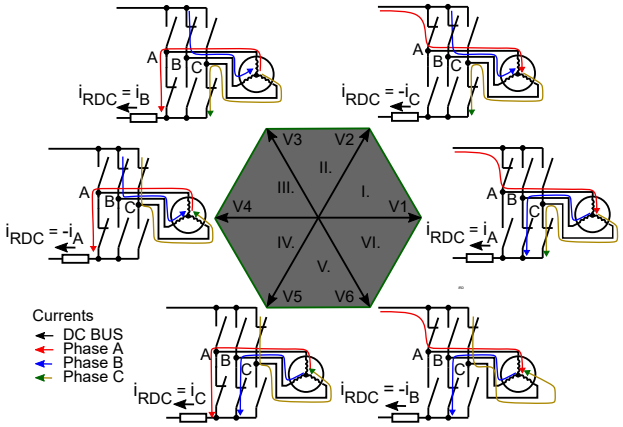

Figure 6. SVM active vectors, switching states and current flow

As shown in Figure 6, during each inverter switching state (applies to active voltage vector only!), only one phase current can be measured. However, all three phase currents need to be known to the control system to control the motor properly. As obvious from Equation 2 at least two currents need to be measured and the remaining one can be calculated. Ideally, the two currents are measured simultaneously. Since this cannot be achieved during one switching state in the case of single-shunt configuration, two phase current readings need to be acquired from two different consecutive active voltage vectors, preferably within one PWM period.

Figure 7 depicts typical SVM switching patterns for corresponding sectors. For each sector, an example of one PWM cycle is shown.

The creation of the demanded voltage vector and switching patterns for sector I are displayed in Figure 8. The rotation of the demanded vector *V* creates a rotational magnetic field in the motor. One rotation of the vector represents one electrical rotation of the motor. As per the picture, the demanded vector *V* can be created by vector combination of the inverter vectors, which create boundaries of the actual sector in which vector *V* is located (that is, vectors *V1* and *V2* for sector I.).

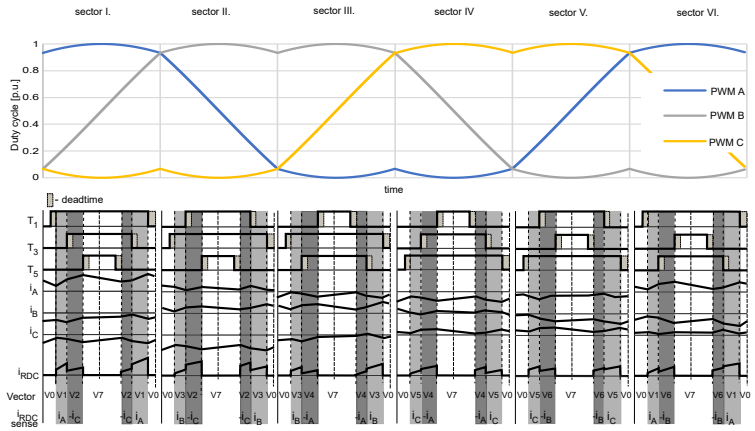

Figure 7. SVM switching patterns, phase, and DC Bus current waveforms for corresponding SVM sectors

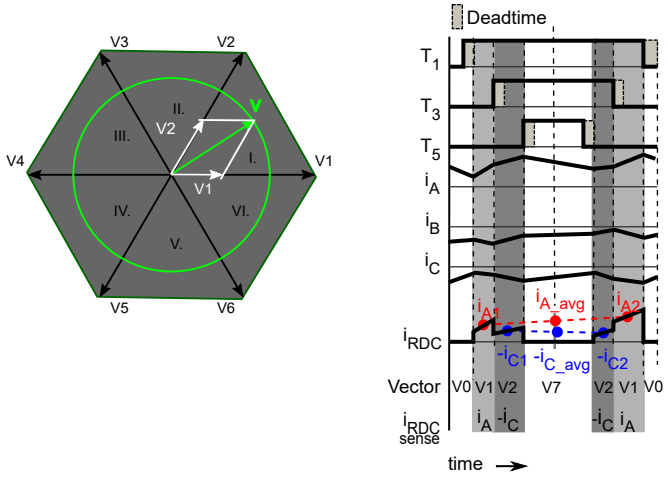

Figure 8. SVM – decomposition of demanded voltage vector, resulting center-aligned switching pattern and current measurement opportunities

The demanded angle and amplitude of *V* is obtained by the corresponding mutual ratio of switch-on intervals of *V1* and *V2* and by the insertion of zero vectors *V0* (all low-side transistors ON) or *V7* (all high-side transistors ON). The resulting center-aligned switching pattern allows for measurement of two motor phase currents in each PWM period half. Since the current varies throughout the PWM period, better measurement accuracy and motor control performance can be achieved by measuring the respective current in both of the PWM period halves and then calculating the average current value. The average values of the two currents are then also closer to each other timeline-wise compared to the consecutive readings acquired in the first and second half of the PWM period.

To be able to take valid current readings, the switch-on interval of either of the vectors needs to be equal to or greater than the ADC conversion time. This cannot be fulfilled close to the sector boundaries and at low amplitudes of the demanded voltage vector *V*. As seen in Figure 9 (dead times are neglected for the sake of picture clarity), while operating close to sector border, one of the active vectors is switched on for times shorter than ADC sample time (and ultimately it is not switched on at all at the sector border). During the operation with low voltage amplitude neither of the active vectors is switched on long enough to enable valid current readings. This results into a “critical zone” where no reliable current measurements can be taken as per Figure 10. The workaround for being able to take current readings while operating in the critical zone is to deform the standard SVM pattern in a way that there will be sufficient measurement windows and the average voltage

vector produced during the PWM period will be identical to that produced by the standard SVM. This document introduces the following techniques:

- Phase-shifted PWM
- Double switching

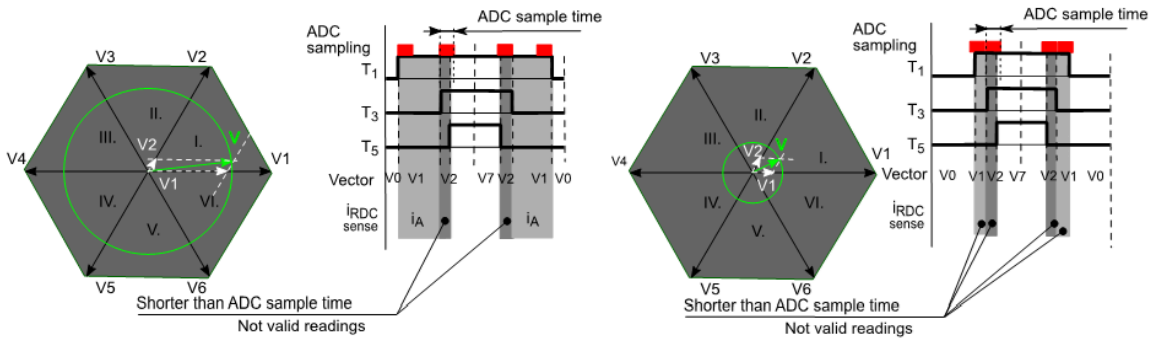

Figure 9. Operation close to the sector border (left) and operation with low voltage amplitude (right)

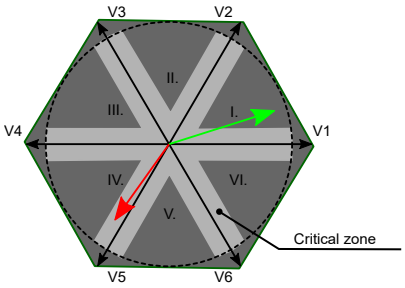

Figure 10. Demanded vector with valid current readings (green) and demanded vector in critical zone (red)

5.2 Phase-shifted PWM

The principle of phase-shifted PWM is the creation of an appropriate sampling window by shifting one of the phase patterns, which form an insufficient sampling window. In the case of standard SVM the duty cycles of the three phases for the particular sector are defined as per Table 2. The phase with the longest duty cycle duration is shifted to the left. The phase with the shortest duty cycle duration is shifted to the right and the phase with the duty cycle of mid-length is kept unshifted.

Table 2. Phase duty cycle comparison vs sector

Sector	I.	II.	III.	IV.	V.	VI.
Phase duty cycle comparison	A > B > C	B > A > C	B > C > A	C > B > A	C > A > B	A > C > B

The resulting voltage vector of the original SVM pattern and the resulting voltage vector of the phase-shifted pattern are the same. The situation is illustrated in Figure 11 and Figure 12. If the current sampling windows are sufficient, the SVM pattern is kept “as is”. In the case of a too narrow sampling window the phase shift is employed. If the insufficient sampling window occurs between the longest and mid-length phase duty cycles, then the longest duty cycle phase is shifted to the left. If the insufficient sampling window occurs between the mid-length and the shortest phase duty cycles, then the shortest duty cycle phase is shifted to the right. In the case of low demanded voltage both of the shifts (to the left and to the right) may occur.

As shown in Figure 11 and Figure 12, phase-shifted PWM does not allow symmetrical current readings. Therefore, the average current values cannot be calculated. The measured phase currents can be far from each other timeline-wise what may cause inaccuracies in the case of motors with low electrical time constants at high speeds, especially in sensorless motor control systems where the motor speed is calculated based on measured motor currents. As with such motors the current varies rapidly and only a couple of current samples per electrical revolution can be acquired at high speeds.

The advantage of phase-shifted PWM is the unchanged amount of switching operations, therefore unchanged switching losses compared to the standard SVM. The method (and the necessary deformation of the switching patterns) is only applied in the critical zone, otherwise the switching patterns are unchanged.

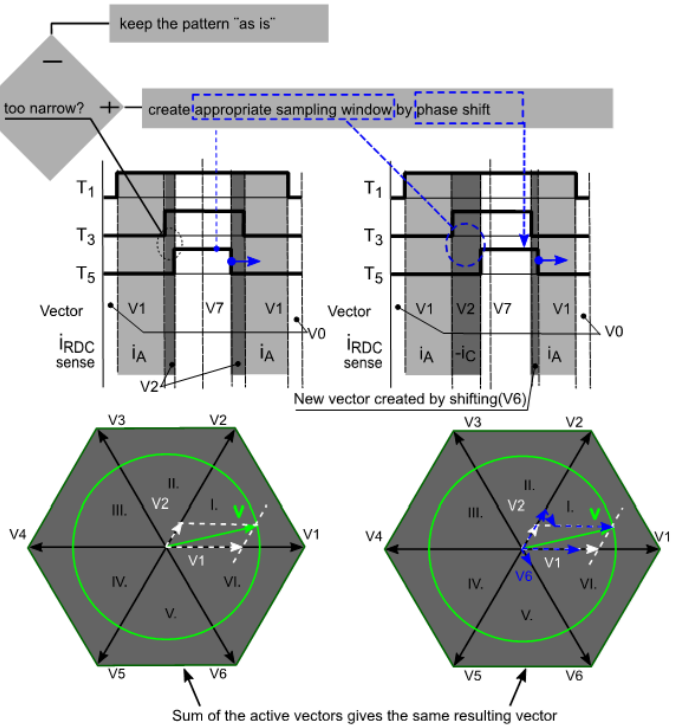

Figure 11. Phase-shifted PWM – shifting the phase with the shortest duty cycle duration to the right

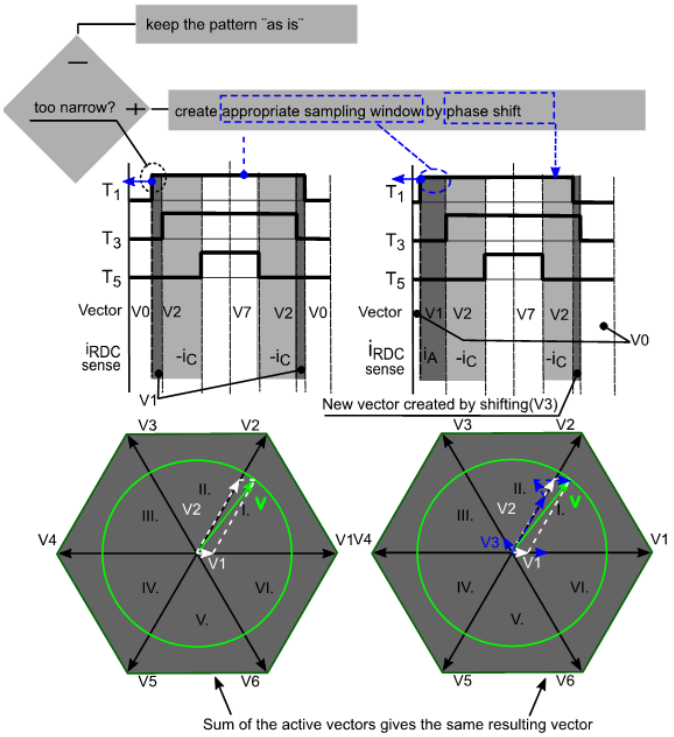

Figure 12. Phase-shifted PWM – shifting the phase with the longest duty cycle duration to the left

5.3 Double switching

5.3.1 The basics of double switching method

The principle of the double switching method is the creation of an appropriate sampling window in two stages:

1. Insertion of zero pulse to the middle of the PWM pattern. This divides the PWM period into two halves and creates two symmetrical half-pulses per phase per PWM period. The sum of the two half-pulse lengths needs to be the same as the length of the original pulse. The width of the zero pulse needs to be stipulated so that the inverter transistors are reliably switched on and off.
2. Shifting the halves of one of the phase patterns (which form an insufficient sampling window) to the sides. In the case of standard SVM, the duty cycles of the three phases for the particular sector are defined as per Table 2. The phase with the duty cycle of the shortest length is kept as is and either the halves of the phase with the longest or mid-length duty cycle are shifted to the sides.

The resulting voltage vector of the original SVM pattern and the resulting voltage vector of the double-switched pattern are the same. The situation is illustrated in Figure 13 and Figure 14. If the current sampling windows are sufficient, the SVM pattern is kept only with the zero pulse inserted and no additional shifting occurs. If there is a too narrow sampling window the phase shift of the half-pulses to the sides occurs. In the case of low demanded voltage both of the shifts (of the phase with longest and mid-length duty cycle) may be necessary. Due to the insertion of the zero pulse and moving of the patterns to the sides, the limitation of the output voltage is necessary. The limit is approximately 93% of the full duty cycle.

The double switching algorithm evaluates the width of the sampling window and calculates the necessary shifts in multiple stages as per Figure 15, to consider newly shifted mid-length pulse halves when checking the available sampling window between the longest and mid-length pulse.

As shown in Figure 13 and Figure 14, double-switched PWM allows symmetrical current readings. Therefore, the average current values can be calculated. This gives better performance, especially at high speeds in the case of motors with low electrical time constants as opposed to phase-shifted PWM.

The disadvantage of the method is double the switching frequency compared to the standard SVM, resulting into higher switching losses. The impact of higher switching losses can be reduced by modifications of the double switching method:

- Adaptive double switching
- Adaptive double switching in one phase only

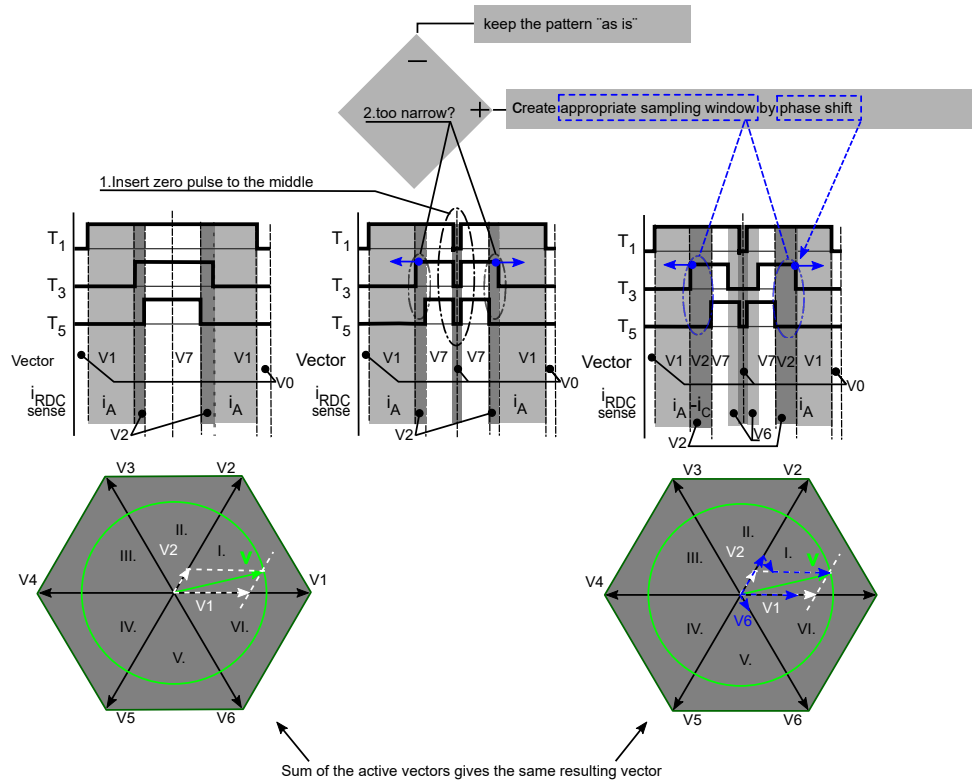

Figure 13. Double switching – shifting the phase with the mid-length duty cycle duration to the sides

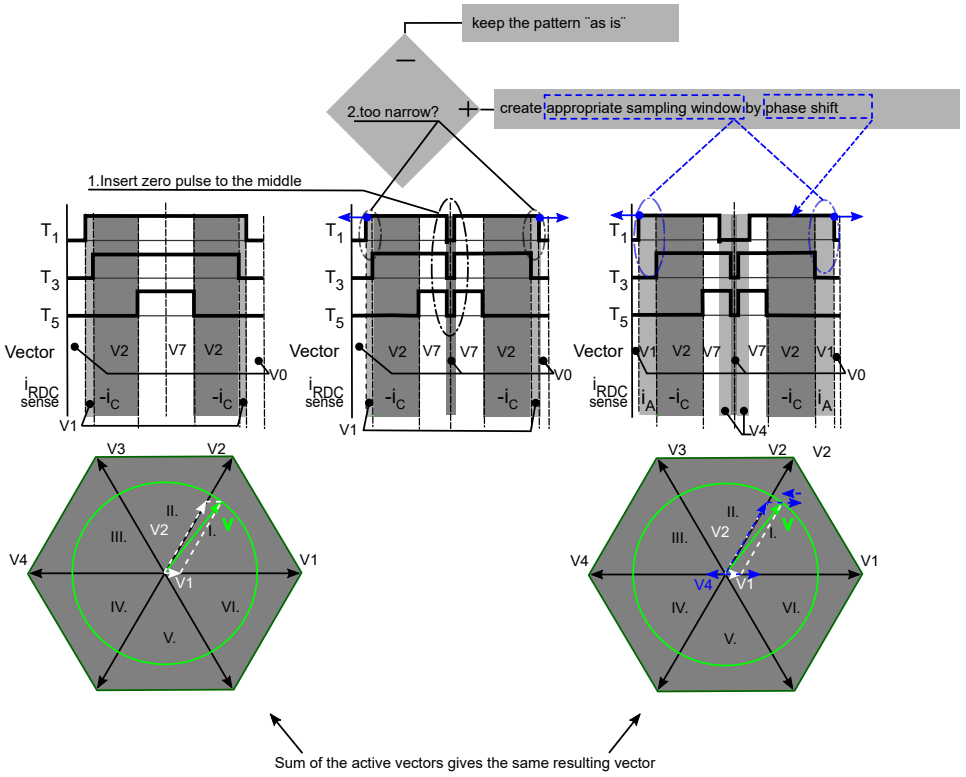

Figure 14. Double switching – shifting the phase with the longest duty cycle duration to the sides

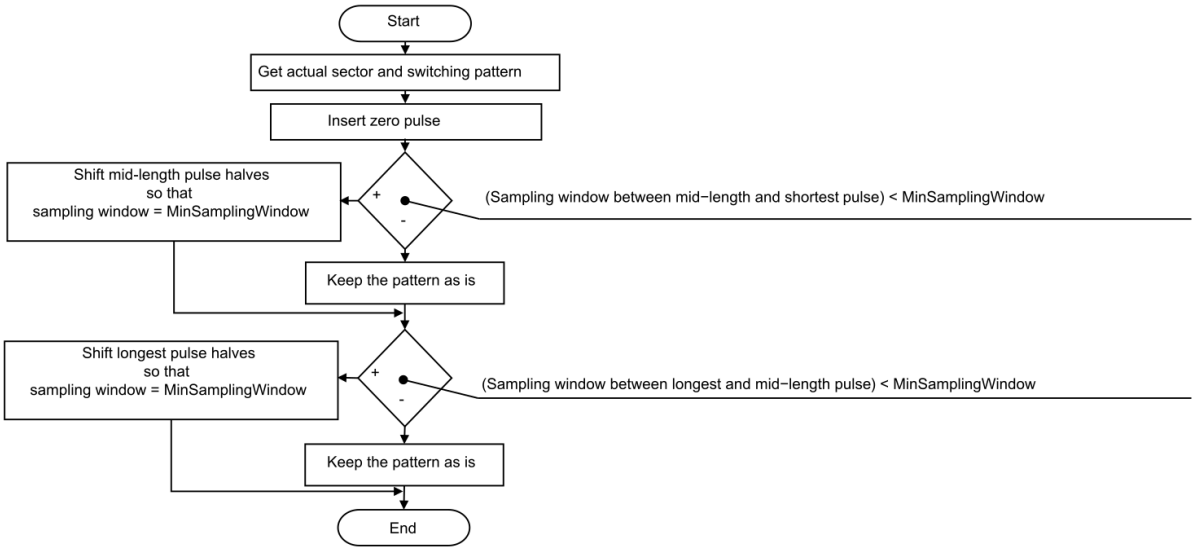

Figure 15. Double switching flowchart

5.3.2 Adaptive double switching

Adaptive double switching is based on applying the double switching method only when the desired voltage vector is located in the critical zone as explained in the chapter Section 5.1 and in Figure 10. If the desired voltage vector lies in the zone with valid current readings, then standard SVM PWM patterns are used. Double

switching is activated only in the critical zone. The flowchart and switching pattern example are displayed in Figure 16 and Figure 17.

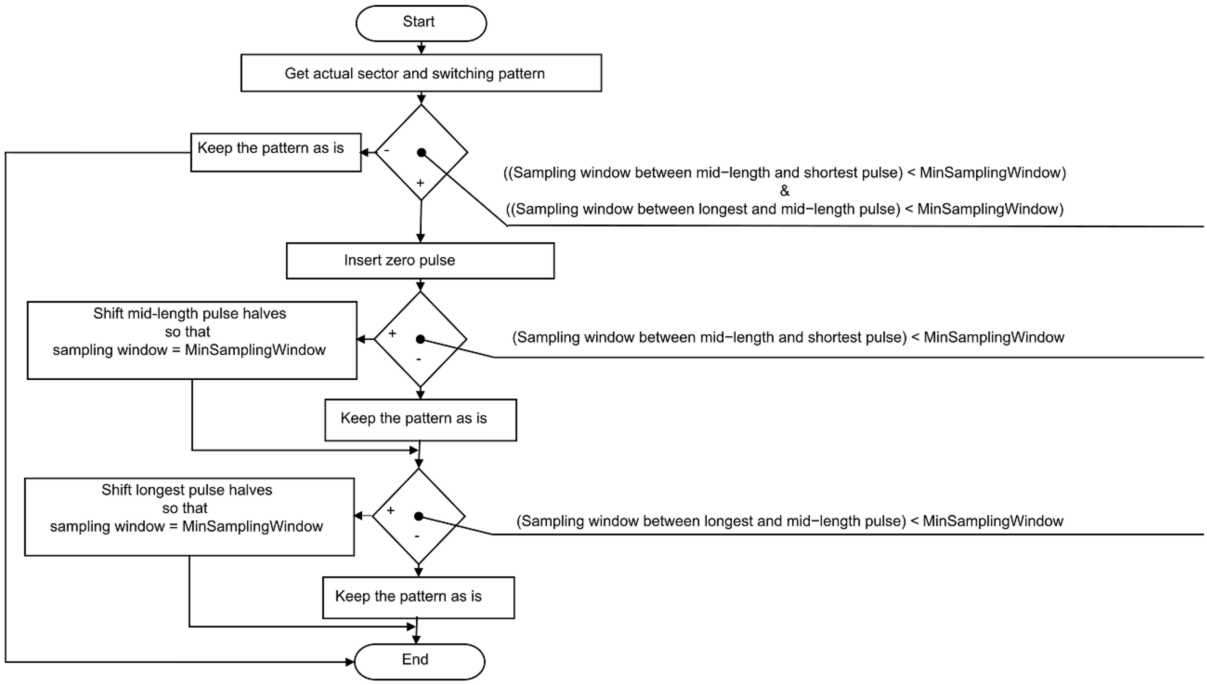

Figure 16. Adaptive double switching flowchart

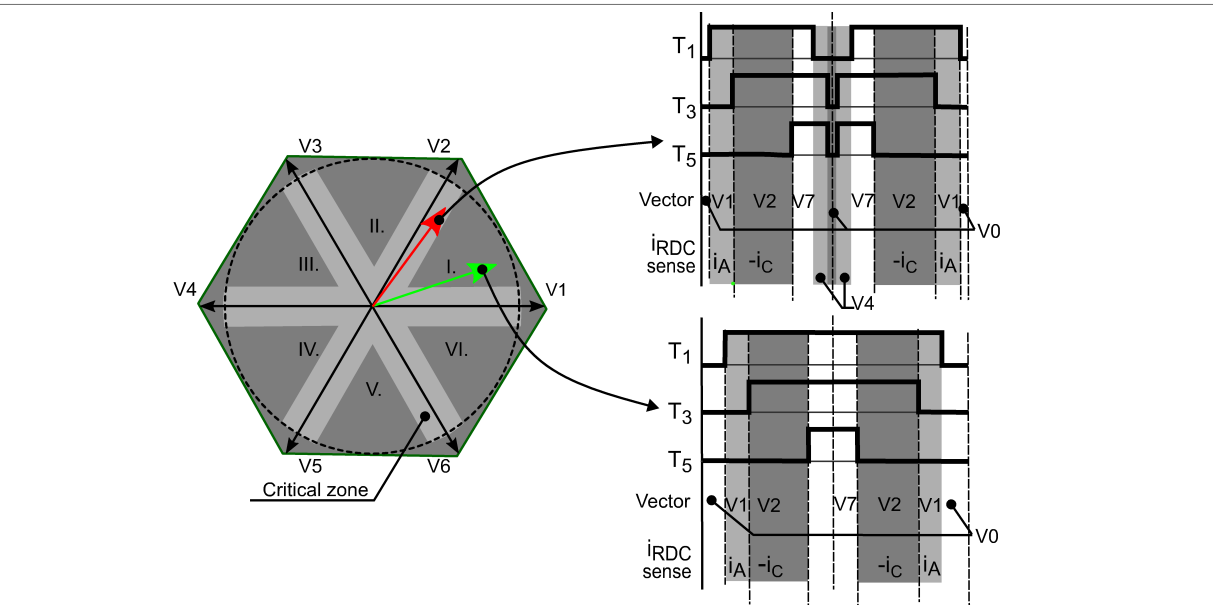

Figure 17. Adaptive double switching – voltage vector position vs switching pattern

This approach results into lower switching losses. The dependence between the critical zone (as a percentage of electrical rotation) and the ratio of demanded vs maximum achievable output voltage (at a given minimum sampling window) can be derived for sector I as:

- Critical zone time interval at the sector beginning:

$$t \in \left\langle 0 \; ; \frac{\text{asin}\frac{2*W}{V}}{\omega} \right\rangle \tag{3}$$

- Critical zone time interval at the sector end:

$$t \in \left\langle \frac{\text{acos}\frac{2*W}{V} - \frac{\pi}{6}}{\omega} ; \; \frac{T}{6} \right\rangle \tag{4}$$

Where:

- t is the time interval of the critical zone
- W is the minimum width of the current sampling window [p.u. of el. period]
- ω is electrical angular speed
- T is the electrical period
- V is the amplitude of the desired output voltage [p.u.]
- Assumption: $2*W < V$; $V \neq 0$

Based on Equation 3 and Equation 4 the dependence between the critical zone duration (area where double switching is active as a percentage of electrical rotation) and the ratio of demanded vs maximum achievable output voltage (as a percentage of DC bus voltage) can be shown as per Figure 18. It needs to be noted that in a real system there would be a zone of "uncertainty" due to the alignment of sampling events of the system vs real time quantities(voltages, currents) which cannot be calculated exactly.

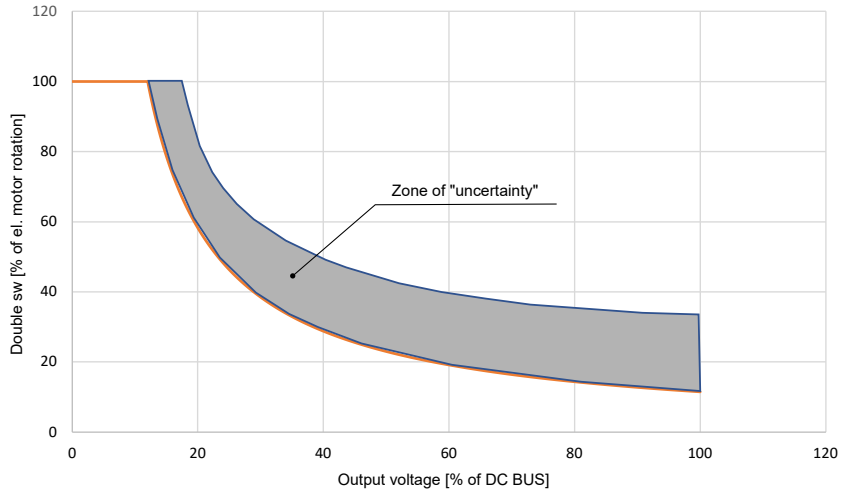

Figure 18. Double switching area vs output voltage (example at a constant minimum sampling window)

5.3.3 Adaptive double switching in one phase only

The approach introduced in the chapter 5.3.2. *Adaptive double switching* can be further modified by performing the double switching only in the phase where the sampling window needs to be widened. This approach is depicted in Figure 19 and Figure 20.

Switching in one phase only results into lower switching losses compared to Adaptive double switching (chapter Section 5.3.2.) However, with certain motors this method can produce slightly more noise compared to Adaptive double switching(depending on motor construction and quality. The appropriate method needs to be chosen for the particular motor.

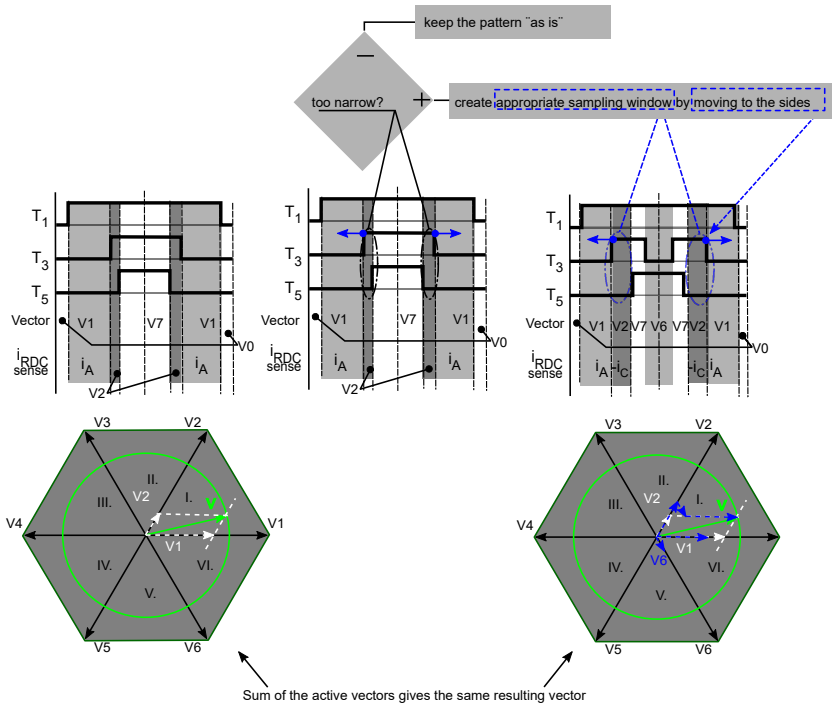

Figure 19. Adaptive double switching in one phase only - moving the phase with the mid-length duty cycle

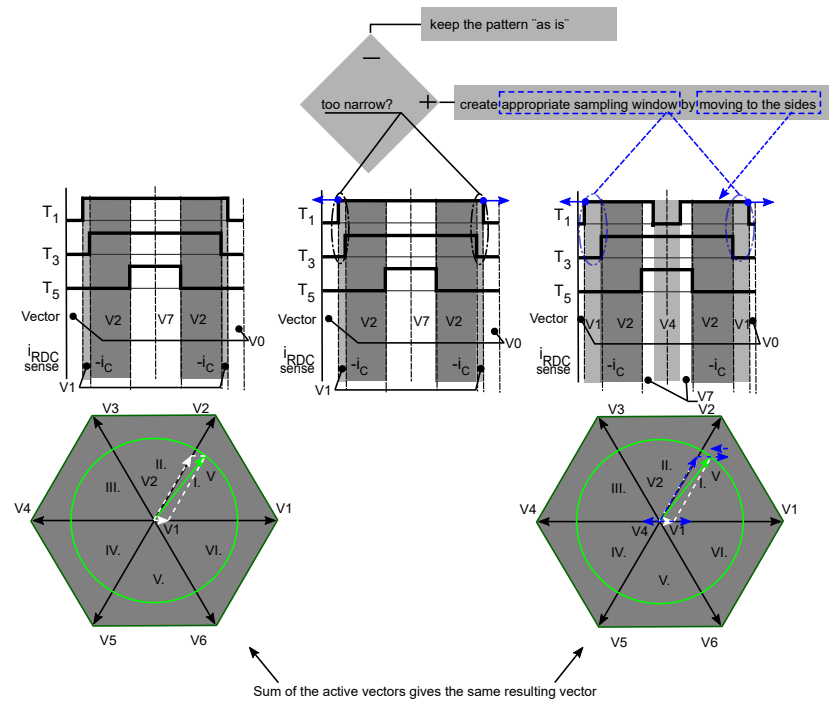

Figure 20. Adaptive double switching in one phase only - moving the phase with the longest duty cycle

6 Summary

Various methods of current sensing have been introduced. Each of the methods is suitable for a different type of application. The main differences among the methods are in the following areas:

- DC Bus utilization
- Bill of material (BOM)
- Redundancy (possible operation with current circuit measurement broken in one phase)
- Switching losses
- Conductive losses
- Control performance with high-speed motors with low electrical time constant
- Algorithm complexity
- Acoustic noise
- Current THD
- EMC

The comparison of the methods is shown in Table 3. However, in the case of acoustic noise and EMC it is not straightforward to pick a method with better performance as the performance is highly dependent on the hardware design of the motor and the power stage.

Generally speaking, dual and triple-shunt methods have better acoustic noise performance but a comparable performance with the single-shunt method is achievable with a properly designed and constructed motor. There can also be differences in acoustic performance among the different single-shunt methods (generally, double and adaptive double switching in all phases perform best) but it highly depends on motor construction and quality.

Also dual, triple-shunt, and phase-shifted PWM techniques have better performance than double switching in case of EMC (less switching operation). But by choosing adaptive double switching (in all or one phase) and by adjusting the HW (power transistors switching performance, PCB design,…) a satisfactory level of EMC can be achieved.

In the end it is up to the user to consider all the trade-offs and pick the right method fit for the purpose.

Table 3. Current sensing method comparison

	Method					
	Triple-shunt	Dual-Shunt	Single-shunt			
			Phase shift	Double switching		
				Non-adaptive (see chapter 5.3.1)	Adaptive	In one phase only
DC Bus utilization	100%	Limited (low-side transistors to be switched on for at least ADC sample time)	Depending on the min. sampling window is possible to reach 100%	Limited to approx. 93%	Limited to approx. 93%	Limited to approx. 93%
BOM [1 – smallest 3 – largest]	3	2	1	1	1	1
Redundancy	yes	no	no	no	no	no

Table 3. Current sensing method comparison*...continued*

	Method					
	Triple-shunt	Dual-Shunt	Single-shunt			
			Phase shift	Double switching		
				Non-adaptive (see chapter 5.3.1)	Adaptive	In one phase only
Switching losses [1 – lowest 4 – highest]	1	1	1	4	3	2
Conductive losses [1 – lowest 3 – highest]	3	2	1	1	1	1
Control performance - high speed, low el. time constant motors [1 – best 3 – worst]	1	1	3	2	2	2
Algorithm complexity [1 - simple 4 - complex]	1 (2 for full DC Bus utilization)	1	3	4	4	4
Current THD	best	best	Higher but comparable	Higher but comparable	Higher but comparable	Higher but comparable

7 Revision history

Table 4. Revision history

Document ID	Release date	Description
AN14164 v. 1.0	21 February 2024	Initial release

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Contents

1 Introduction 2
2 Current sensors 2
3 Current sensing techniques based on Ohm's law 2
4 Low-side current sensing 2
4.1 Triple-shunt 3
4.2 Dual-shunt 5
5 DC Bus current sensing – single shunt 6
5.1 DC bus current sensing – phase current reconstruction 6
5.2 Phase-shifted PWM 9
5.3 Double switching 11
5.3.1 The basics of double switching method 11
5.3.2 Adaptive double switching 13
5.3.3 Adaptive double switching in one phase only 15
6 Summary 17
7 Revision history 18
8 Legal information 19

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