AN14760

PCIe Enablement and Benchmarking Guidelines for i.MX 95

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Document information

Information	Content
Keywords	AN14760, i.MX 95, PCIe, IMX95LPD5EVK-19, enabling, benchmarking, root complex, endpoint, MSI/ MSI-X, max payload size (MPS), pci_endpoint_test
Abstract	This application note provides the comprehensive guidelines for enabling and benchmarking the peripheral component interconnect express (PCIe) on i.MX 95.

1 Introduction

This application note provides the comprehensive guidelines for enabling and benchmarking the peripheral component interconnect express (PCIe) on i.MX 95. The board used in the test is IMX95LPD5EVK-19.

1.1 PCIe overview

The PCIe is a high-speed serial communication protocol widely used for connecting processors to peripherals such as network cards, storage devices, and accelerators. PCIe performance and reliability are essential in system design with the increasing demand for high-throughput, and low-latency data transfer in applications such as:

- AI
- Machine learning
- Multimedia processing

PCIe offers scalable bandwidth through multiple lanes and supports both Root complex (RC) and Endpoint (EP) modes.

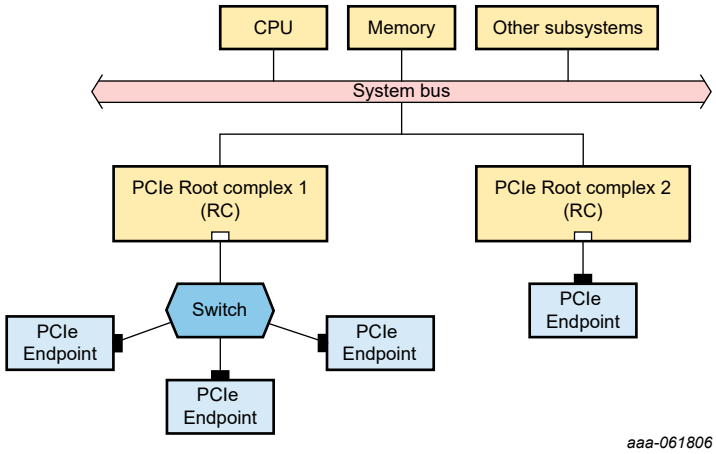

Figure 1. PCIe architecture overview

The support for advanced features like direct memory access (DMA) for efficient memory access, message signaled interrupts (MSI)/MSI-X for scalable interrupt handling and power management are critical for performance-sensitive applications.

To ensure the stable operation and achieve the expected performance levels, enabling the PCIe correctly is essential. Benchmarking plays a vital role in identifying bottlenecks or misconfigurations and comparing performance across different setups.

1.2 i.MX 95 overview

The i.MX 95 is a high-performance applications processor designed for next-generation edge computing applications across automotive, industrial, medical, and Internet of Things (IoT) domains. For more details, see i.MX 95 Applications Processor Family: High-Performance, Safety Enabled Platform with eIQ Neutron NPU. It has:

- Six Arm Cortex-A55 application cores (up to 2.0 GHz)
- High-performance Arm Cortex-M7 and low-power Arm Cortex-M33 for real-time and safety-critical tasks
- PCIe capabilities:
  - 2x PCIe Gen 3.0 interfaces, each supporting x1 lane

– Operable in RC and EP mode

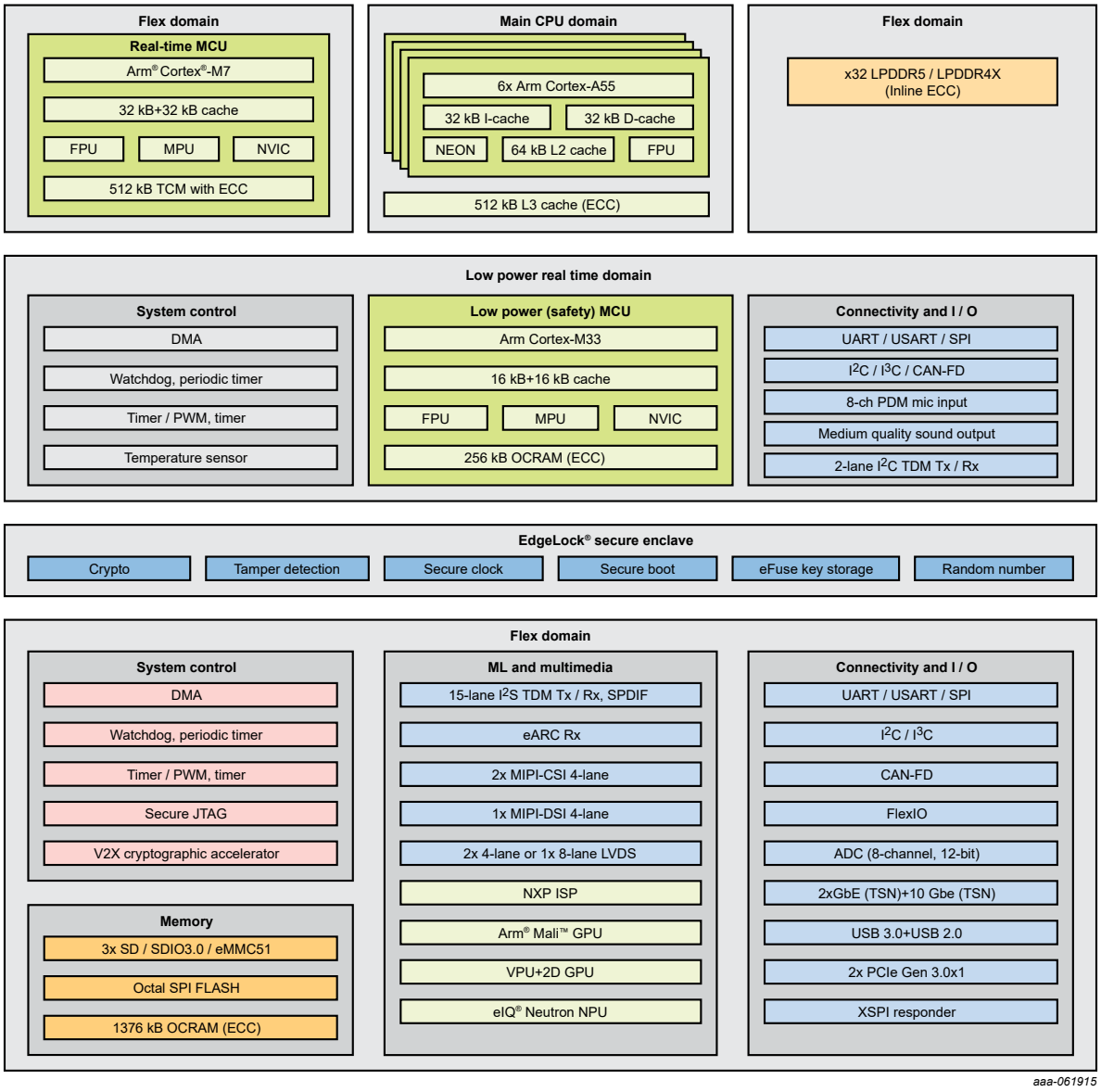

Figure 2. i.MX 95 applications processor block diagram

2 i.MX 95 PCIe enablement

This section provides the software and hardware setup details and PCIe enablement.

2.1 Software setup

The PCIe setup is performed on the 6.6.52 Linux BSP version, see the imx-manifest. The following section describes the software setup, where one board with the PCIe driver is configured for RC and the second board is configured for EP. The PCIe driver configuration in each mode is achieved with different Linux DTB configurations. Figure 3 shows the overview of the software setup.

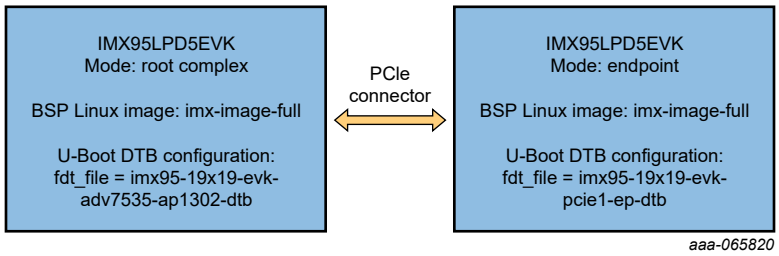

Figure 3. Overview of the software setup

1. Obtain the NXP Linux BSP sources:
   The following commands show how to download the i.MX Yocto Project BSP recipe layers. For this example, a directory called “imx-yocto-bsp” is created for the project. User can use any name as required. For more details on building an image for a specific release, see the “Embedded Linux for i.MX Applications Processors” in the *i.MX Yocto Project User's Guide* (UG10164).

```
$ mkdir imx-yocto-bsp
$ cp imx-yocto-bsp
# Initialize the Yocto Project from manifest
$ repo init -u https://github.com/nxp-imx/imx-manifest -b imx-linux-scarthgap
 -m imx-6.6.52-2.2.0.xml
$ repo sync
```

2. Set up the build configuration:
   i.MX 95 provides a script “imx-setup-release.sh” that simplifies the setup for i.MX 95 machines. To use the script, provide the names of the specific machine to be built and the desired graphical backend. The script sets up a directory and the configuration files for the specified machine and backend.

```
$ MACHINE=imx95-19x19-lpddr5-evk DISTRO=fsl-imx-xwayland source ./imx-setup-
release.sh -b bld-xwayland
```

3. Configure RC and EP in the kernel:
   Kernel config for the RC:
   - CONFIG_PCI_IMX6 = y
   - CONFIG_PCI_IMX6_HOST = y

   Kernel Config for the EP:
   - CONFIG_PCI_IMX6 = y
   - CONFIG_PCI_IMX6_EP = y

   Kernel Config for the EPF test driver support for EP:
   - CONFIG_PCI_ENDPOINT = y
   - CONFIG_PCI_ENDPOINT_CONFIGFS = y
   - CONFIG_PCI_ENDPOINT_TEST = y
   - CONFIG_PCI_EPF_TEST = y
4. Apply kernel patches to support the PCIe benchmark test:
   An additional patch is required to enable the PCIe EPF test for i.MX 95 device and to report the read/write speed.

```
diff --git
a/drivers/misc/pci_endpoint_test.c
b/drivers/misc/pci_endpoint_test.c
index 780b80790436..4d5979e2617f 100644
--- a/drivers/misc/pci_endpoint_test.c
+++ b/drivers/misc/pci_endpoint_test.c
```

```
@@ -1006,6 +1006,9 @@ static const struct pci_device_id
 pci_endpoint_test_tbl[] = {
        { PCI_DEVICE(PCI_VENDOR_ID_FREESCALE, PCI_DEVICE_ID_IMX8),
          .driver_data = (kernel_ulong_t)&default_data,
        },
+       { PCI_DEVICE(PCI_VENDOR_ID_NXP2, PCI_DEVICE_ID_NXP2),
+         .driver_data = (kernel_ulong_t)&default_data,
+        },
        { PCI_DEVICE(PCI_VENDOR_ID_FREESCALE, PCI_DEVICE_ID_IMX6),
          .driver_data = (kernel_ulong_t)&imx6q_data
        },
diff --git a/include/linux/pci_ids.h b/include/linux/pci_ids.h
index fe153f399337..eaec4e499841 100644
--- a/include/linux/pci_ids.h
+++ b/include/linux/pci_ids.h
@@ -1551,8 +1551,10 @@
 #define PCI_DEVICE_ID_FORE_PCA200E     0x0300

 #define PCI_VENDOR_ID_PHILIPS          0x1131
+#define PCI_VENDOR_ID_PHILIPS           0x0000
 /* NXP has two vendor IDs, the other one is 0x1957 */
 #define PCI_VENDOR_ID_NXP2             PCI_VENDOR_ID_PHILIPS
+#define PCI_DEVICE_ID_NXP2              PCI_DEVICE_ID_PHILIPS
 #define PCI_DEVICE_ID_PHILIPS_SAA7146  0x7146
 #define PCI_DEVICE_ID_PHILIPS_SAA9730  0x9730
 #define PCI_DEVICE_ID_NXP2_NETC_RCEC   0xe001
```

To apply the patches, run the following commands:

```
$ bitbake -c devshell linux-imx
# in the new shell, git commands can be used
$ git apply --check <patch_file>
$ git apply <patch_file>
```

5. Build the Image:
   To build the SD card image, run the following commands:

```
$ bitbake -f -c compile linux-imx
$ bitbake -f -c deploy linux-imx
```

6. Deployment on board:
   The image is available at `<build_dir>/tmp/deploy/images/imx95-19x19-lpddr5-evk`.
   Image can be deployed on the board in the following ways:
   a. Using the UUU tool:
      Connect the USB cable with the USB1 connector (J29) on board.

```
$ uuu -lsusb
$ uuu -b emmc_all imx-image-core-imx95-19x19-lpddr5-
evk.rootfs-20250319110032.wic
```

   b. Write the image on an SD card for each board:

The image is available at `<build_dir>/tmp/deploy/images/imx95-19x19-lpddr5-evk`. It is necessary to write the image on an SD card for each board. The `lsblk` command can be used to find the SD card drive. To write the image, use the following command:

```
$ bzcat imx-image-core-imx95-19x19-lpddr5-evk.rootfs-20250319110032.wic |
 sudo dd of=/dev/sd<drive> bs=1M && sync
```

c. Replace the kernel image on the board:
Replace the image in bootpartition.

```
$ root@imx95evk# cd /run/media/boot-mmcblk0p1
$ root@imx95evk# scp <user>@<ip>:<dir>/linux-imx/linux imx/arch/arm64/
boot/Image run/media/boot-mmcblk0p1/
```

2.2 Hardware setup

PCIe benchmarks can only be performed if two boards are interconnected using the same type of PCIe connection. The boards used are IMX95LPD5EVK-19.

Figure 4 shows the signals for the PCIe CEM connector:

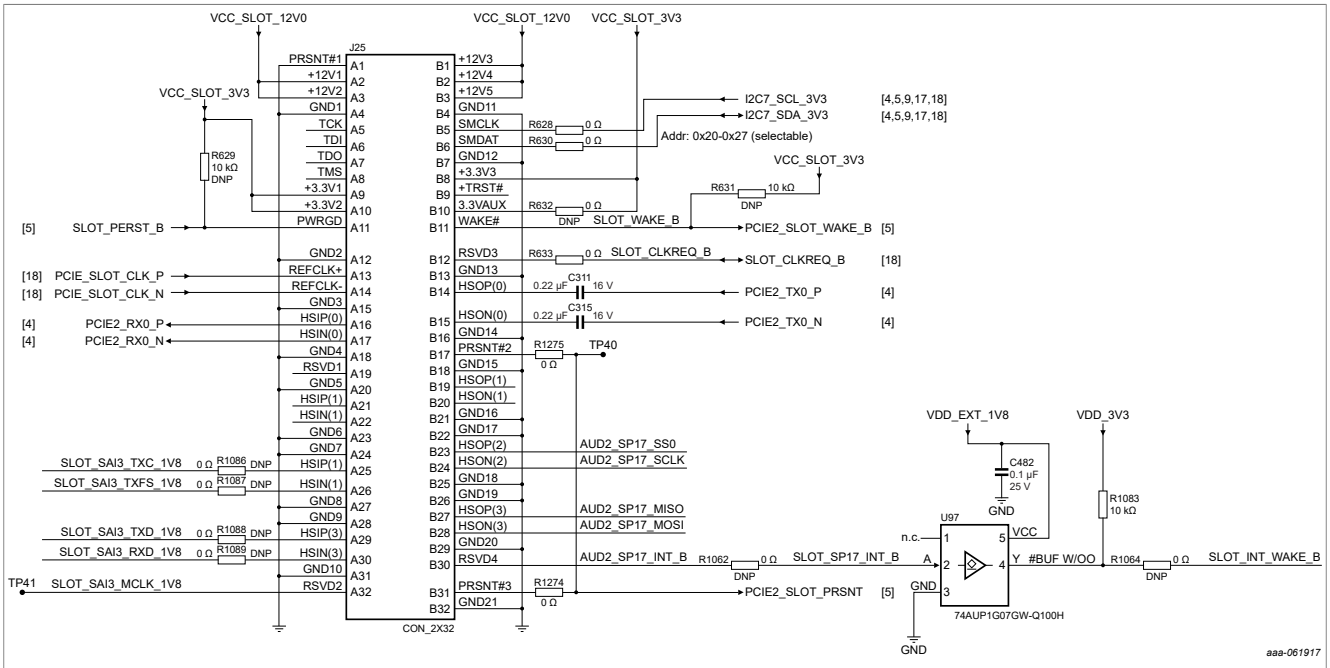

Figure 4. PCIe connection schematics

Note: *The Figure 4 represents the electrical connections used for benchmarking. For more details on comprehensive layout guidelines, see the i.MX 95 Hardware Design Guide (UG10210) and the PCIe Specifications.*

For creating the setup, use the following:

- NXP proprietary M4-PCIE-SGMII connector with Samtec type 3 cable assembly (ECUE-08-030-T2-FF-02-1-D1).
- Any high-quality PCIe Gen3/Gen4-compliant CEM-to-CEM connector cable to interconnect both the IMX95LPD5EVK-19 boards. For example: PCI Express Jumper Cable Assemblies, PCI Express 4.0 Cable Assembly.

Setup the PCIe with the IMX95LPD5EVK-19 boards as follows:

1. Connect the M4-PCIE-SGMII connector with the IMX95LPD5EVK-19 board CEM connector. For details, see Figure 5.

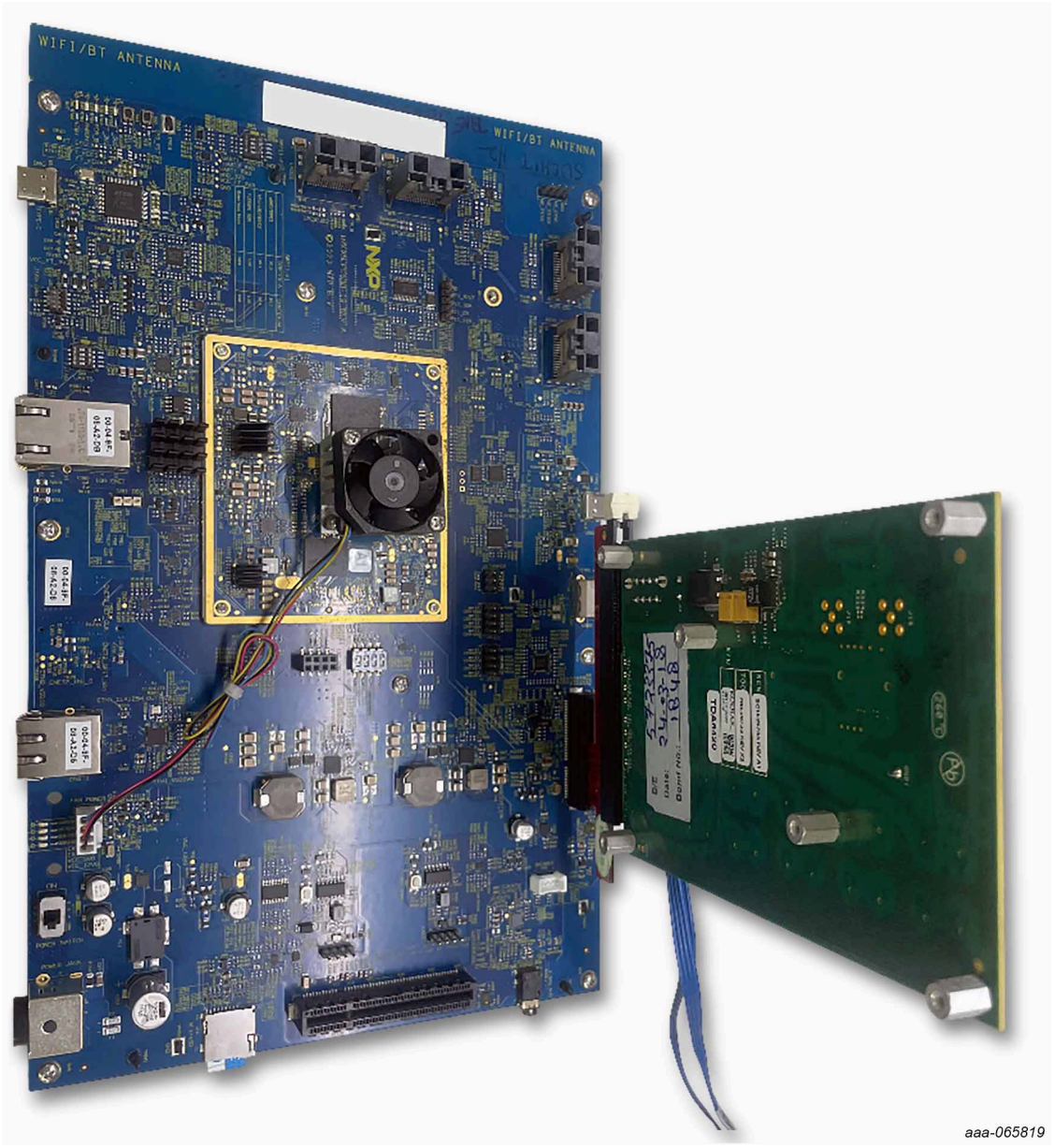

Figure 5. Insert the M4-PCIE-SGMII connector into the board CEM connector

2. Connect the second IMX95LPD5EVK-19 board as shown in Figure 6.

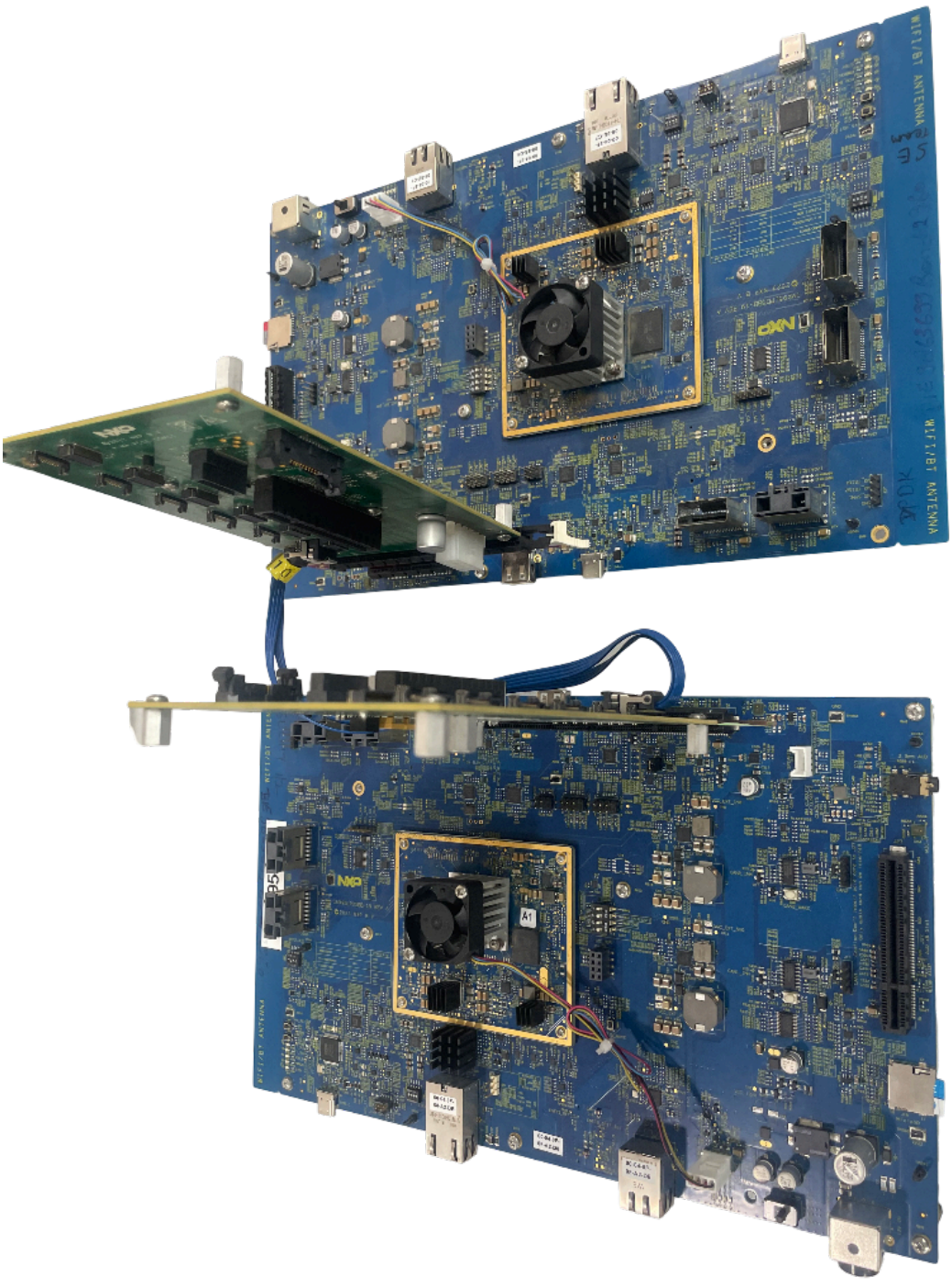

Figure 6. Connect the second board

3. Connect the SD card, Ethernet cable, debug cable, and power cord as shown in Figure 7.

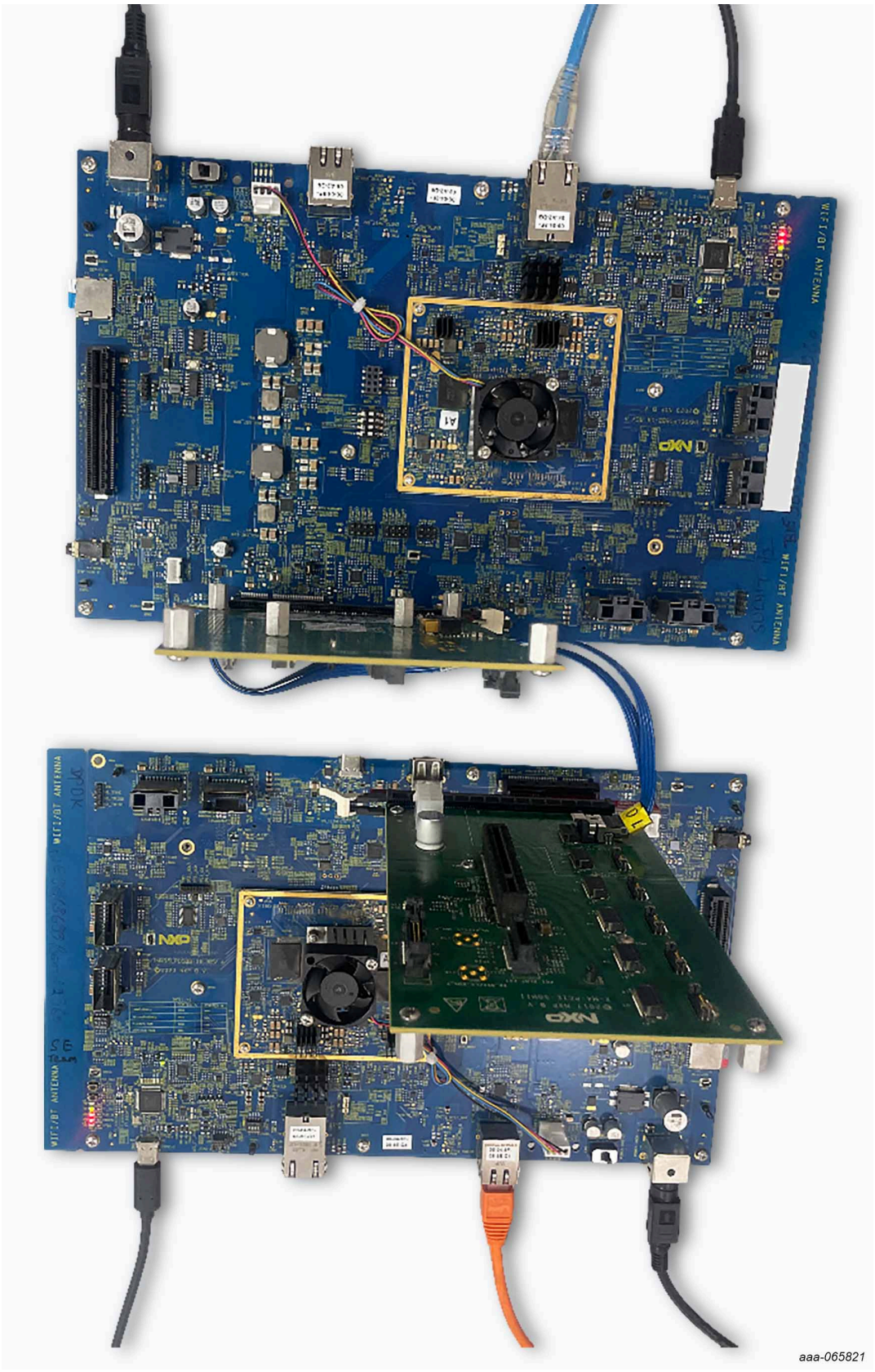

Figure 7. Final setup (SD card, Ethernet cable, debug cable, and power cord connected)

2.3 Methodology

The test procedure is based on the standard PCI Test User Guide. The PCIe DMA benchmarking procedure uses the new EP framework introduced starting with the 5.4.y release line. One board must be configured in RC mode, while the second board must be configured in EP mode. To achieve this configuration, change the `.dtb` files used in each case from the U-Boot command line. Each board presents four COM ports. Open the third port for the debug console.

For RC, ensure that the `imx95-19x19-evk-adv7535-ap1302.dtb` is used:

```
=> print fdt_file
fdt_file= imx95-19x19-evk-adv7535-ap1302.dtb
```

For EP, ensure that the `imx95-19x19-evk-pcie1-ep.dtb` is used:

```
=> print fdt_file
fdt_file= imx95-19x19-evk-pcie1-ep.dtb
=> setenv fdt_file imx95-19x19-evk-pcie1-ep.dtb
=> saveenv
Saving Environment to MMC... Writing to MMC(1)... OK
```

The following are the `lspci` logs on the RC:

```
$lspci -vvxxx
0001:00:00.0 PCI bridge: Philips Semiconductors Device 0000 (prog-if 00 [Normal
 decode])
Control: I/O+ Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping-
 SERR+ FastB2B- DisINTx+
Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort-
 >SERR- <PERR- INTx-
Latency: 0
Interrupt: pin A routed to IRQ 239
IOMMU group: 2
Region 0: Memory at a10000000 (32-bit, non-prefetchable) [size=1M]
Bus: primary=00, secondary=01, subordinate=01, sec-latency=0
I/O behind bridge: [disabled] [16-bit]
Memory behind bridge: 10100000-102fffff [size=2M] [32-bit]
Prefetchable memory behind bridge: [disabled] [64-bit]
Secondary status: 66MHz- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort-
 <SERR- <PERR-
Expansion ROM at a10300000 [virtual] [disabled] [size=64K]
BridgeCtl: Parity- SERR+ NoISA- VGA- VGA16- MAbort- >Reset- FastB2B-
PriDiscTmr- SecDiscTmr- DiscTmrStat- DiscTmrSERREn-
Capabilities: [40] Power Management version 3
Flags: PMEClk- DSI- D1+ D2+ AuxCurrent=375mA PME(D0+,D1+,D2-,D3hot+,D3cold-)
Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-
Capabilities: [50] MSI: Enable+ Count=1/32 Maskable+ 64bit+
Address: 0000000094040000 Data: 0000
Masking: fffffffe Pending: 00000000
Capabilities: [70] Express (v2) Root Port (Slot-), IntMsgNum 0
DevCap: MaxPayload 256 bytes, PhantFunc 0
ExtTag- RBE+
DevCtl: CorrErr- NonFatalErr- FatalErr- UnsupReq-
RlxdOrd+ ExtTag- PhantFunc- AuxPwr- NoSnoop-
MaxPayload 128 bytes, MaxReadReq 512 bytes
DevSta: CorrErr- NonFatalErr- FatalErr- UnsupReq- AuxPwr- TransPend-
LnkCap: Port #0, Speed 8GT/s, Width x1, ASPM L1, Exit Latency L1 <16us
ClockPM- Surprise- LLActRep+ BwNot- ASPMOptComp+
LnkCtl: ASPM Disabled; RCB 128 bytes, LnkDisable- CommClk+
```

```
ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-
LnkSta: Speed 8GT/s, Width x1
TrErr- Train- SlotClk+ DLActive+ BWMgmt- ABWMgmt-
RootCap: CRSVisible-
RootCtl: ErrCorrectable- ErrNon-Fatal- ErrFatal- PMEIntEna+ CRSVisible-
RootSta: PME ReqID 0000, PMEStatus- PMEPending-
DevCap2: Completion Timeout: Range ABCD, TimeoutDis+ NROPrPrP+ LTR+
10BitTagComp- 10BitTagReq- OBFF Not Supported, ExtFmt- EETLPPrefix-
EmergencyPowerReduction Not Supported, EmergencyPowerReductionInit-
FRS- LN System CLS Not Supported, TPHComp- ExtTPHComp- ARIFwd+
AtomicOpsCap: Routing- 32bit- 64bit- 128bitCAS-
DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis- ARIFwd-
AtomicOpsCtl: ReqEn- EgressBlck-
IDOReq- IDOCompl- LTR+ EmergencyPowerReductionReq-
10BitTagReq- OBFF Disabled, EETLPPrefixBlk-
LnkCap2: Supported Link Speeds: 2.5-8GT/s, Crosslink- Retimer- 2Retimers- DRS-
LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-
Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-
Compliance Preset/De-emphasis: -6dB de-emphasis, 0dB preshoot
LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+
 EqualizationPhase1+
EqualizationPhase2+ EqualizationPhase3+ LinkEqualizationRequest-
Retimer- 2Retimers- CrosslinkRes: unsupported
Capabilities: [100 v2] Advanced Error Reporting
UESta: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC-
 UnsupReq- ACSViol-
UEMsk: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC-
 UnsupReq- ACSViol-
UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO- CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+ ECRC-
 UnsupReq- ACSViol-
CESta: RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr-
CEMsk: RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr+
AERCap: First Error Pointer: 00, ECRCGenCap+ ECRCGenEn- ECRCChkCap+ ECRCChkEn-
MultHdrRecCap- MultHdrRecEn- TLPPfxPres- HdrLogCap-
HeaderLog: 00000000 00000000 00000000 00000000
RootCmd: CERptEn- NFERptEn- FERptEn-
RootSta: CERcvd- MultCERcvd- UERcvd- MultUERcvd-
FirstFatal- NonFatalMsg- FatalMsg- IntMsgNum 0
ErrorSrc: ERR_COR: 0000 ERR_FATAL/NONFATAL: 0000
Capabilities: [148 v1] Secondary PCI Express
LnkCtl3: LnkEquIntrruptEn- PerformEqu-
LaneErrStat: 0
Capabilities: [160 v1] L1 PM Substates
L1SubCap: PCI-PM_L1.2+ PCI-PM_L1.1+ ASPM_L1.2+ ASPM_L1.1+ L1_PM_Substates+
PortCommonModeRestoreTime=10us PortTPowerOnTime=10us
L1SubCtl1: PCI-PM_L1.2- PCI-PM_L1.1+ ASPM_L1.2- ASPM_L1.1-
T_CommonMode=10us LTR1.2_Threshold=26016ns
L1SubCtl2: T_PwrOn=10us
Capabilities: [170 v1] Vendor Specific Information: ID=0006 Rev=0 Len=018 <?>
Kernel driver in use: pcieport
Kernel modules: pci_endpoint_test
00: 31 11 00 00 07 05 10 00 00 00 04 06 00 00 01 00
10: 00 00 00 10 00 00 00 00 00 01 01 00 f0 00 00 00
20: 10 10 20 10 f1 ff 01 00 00 00 00 00 00 00 00 00
30: 00 00 00 00 40 00 00 00 00 00 00 00 ee 01 02 00
40: 01 50 c3 5f 08 00 00 00 00 00 00 00 00 00 00 00
50: 05 70 8b 01 00 00 04 94 00 00 00 00 00 00 00 00
60: fe ff ff ff 00 00 00 00 00 00 00 00 00 00 00 00
70: 10 00 42 00 01 80 00 00 10 20 00 00 13 68 52 00
80: 48 00 13 30 20 00 00 00 c0 03 40 00 08 00 00 00
```

```
90: 00 00 00 00 3f 0c 00 00 00 04 00 00 0e 00 00 00
a0: 03 00 1e 00 00 00 00 00 00 00 00 00 00 00 00 00
b0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
c0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
d0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
e0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
f0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
0001:01:00.0 Non-VGA unclassified device: Philips Semiconductors Device 0000
Control: I/O- Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping-
 SERR- FastB2B- DisINTx+
Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort-
 >SERR- <PERR- INTx-
Latency: 0
Interrupt: pin A routed to IRQ 250
IOMMU group: 2
Region 0: Memory at a10244000 (32-bit, non-prefetchable) [size=4K]
Region 1: Memory at a10220000 (32-bit, non-prefetchable) [size=64K]
Region 2: Memory at a10245000 (32-bit, non-prefetchable) [size=4K]
Region 3: Memory at a10240000 (32-bit, non-prefetchable) [size=16K]
Region 4: Memory at a10200000 (32-bit, non-prefetchable) [size=128K]
Region 5: Memory at a10100000 (32-bit, non-prefetchable) [size=1M]
Expansion ROM at a10230000 [virtual] [disabled] [size=64K]
Capabilities: [40] Power Management version 3
Flags: PMEClk- DSI- D1+ D2+ AuxCurrent=375mA PME(D0+,D1+,D2-,D3hot+,D3cold-)
Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-
Capabilities: [50] MSI: Enable+ Count=16/16 Maskable+ 64bit+
Address: 0000000094040000 Data: 0010
Masking: 00000000 Pending: 00000000
Capabilities: [70] Express (v2) Endpoint, IntMsgNum 0
DevCap: MaxPayload 256 bytes, PhantFunc 0, Latency L0s unlimited, L1 unlimited
ExtTag- AttnBtn- AttnInd- PwrInd- RBE+ FLReset+ SlotPowerLimit 0W
DevCtl: CorrErr- NonFatalErr- FatalErr- UnsupReq-
RlxdOrd+ ExtTag- PhantFunc- AuxPwr- NoSnoop- FLReset-
MaxPayload 128 bytes, MaxReadReq 512 bytes
DevSta: CorrErr- NonFatalErr- FatalErr- UnsupReq- AuxPwr- TransPend-
LnkCap: Port #0, Speed 8GT/s, Width x1, ASPM L1, Exit Latency L1 <16us
ClockPM+ Surprise- LLActRep- BwNot- ASPMOptComp+
LnkCtl: ASPM Disabled; RCB 64 bytes, LnkDisable- CommClk+
ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-
LnkSta: Speed 8GT/s, Width x1
TrErr- Train- SlotClk+ DLActive- BWMgmt- ABWMgmt-
DevCap2: Completion Timeout: Range ABCD, TimeoutDis+ NROPrPrP- LTR+
10BitTagComp- 10BitTagReq- OBFF Not Supported, ExtFmt- EETLPPrefix-
EmergencyPowerReduction Not Supported, EmergencyPowerReductionInit-
FRS- TPHComp- ExtTPHComp-
AtomicOpsCap: 32bit- 64bit- 128bitCAS-
DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis-
AtomicOpsCtl: ReqEn-
IDOReq- IDOCompl- LTR+ EmergencyPowerReductionReq-
10BitTagReq- OBFF Disabled, EETLPPrefixBlk-
LnkCap2: Supported Link Speeds: 2.5-8GT/s, Crosslink- Retimer- 2Retimers- DRS-
LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-
Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-
Compliance Preset/De-emphasis: -6dB de-emphasis, 0dB preshoot
LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+
 EqualizationPhase1+
EqualizationPhase2+ EqualizationPhase3+ LinkEqualizationRequest-
Retimer- 2Retimers- CrosslinkRes: unsupported
Capabilities: [100 v2] Advanced Error Reporting
```

```
UESta: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC-
 UnsupReq- ACSViol-
UEMsk: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP- ECRC-
 UnsupReq- ACSViol-
UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO- CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+ ECRC-
 UnsupReq- ACSViol-
CESta: RxErr+ BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr-
CEMsk: RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr+
AERCap: First Error Pointer: 00, ECRCGenCap+ ECRCGenEn- ECRCChkCap+ ECRCChkEn-
MultHdrRecCap- MultHdrRecEn- TLPPfxPres- HdrLogCap-
HeaderLog: 00000000 00000000 00000000 00000000
Capabilities: [148 v1] Secondary PCI Express
LnkCtl3: LnkEquIntrruptEn- PerformEqu-
LaneErrStat: LaneErr at lane: 0
Capabilities: [158 v1] Latency Tolerance Reporting
Max snoop latency: 0ns
Max no snoop latency: 0ns
Capabilities: [160 v1] L1 PM Substates
L1SubCap: PCI-PM_L1.2+ PCI-PM_L1.1+ ASPM_L1.2+ ASPM_L1.1+ L1_PM_Substates+
PortCommonModeRestoreTime=10us PortTPowerOnTime=10us
L1SubCtl1: PCI-PM_L1.2- PCI-PM_L1.1- ASPM_L1.2- ASPM_L1.1-
T_CommonMode=0us LTR1.2_Threshold=26016ns
L1SubCtl2: T_PwrOn=10us
Capabilities: [170 v1] Vendor Specific Information: ID=0006 Rev=0 Len=018 <?>
Kernel driver in use: pci-endpoint-test
Kernel modules: pci_endpoint_test
00: 31 11 00 00 06 04 10 00 00 00 00 ff 00 00 00 00
10: 00 40 24 10 00 00 22 10 00 50 24 10 00 00 24 10
20: 00 00 20 10 00 00 10 10 00 00 00 00 00 00 00 00
30: 00 00 00 00 40 00 00 00 00 00 00 00 ee 01 00 00
40: 01 50 c3 5f 08 00 00 00 00 00 00 00 00 00 00 00
50: 05 70 c9 01 00 00 04 94 00 00 00 00 10 00 00 00
60: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
70: 10 00 02 00 c1 8f 00 10 10 20 00 00 13 68 46 00
80: 40 00 13 10 00 00 00 00 00 00 00 00 00 00 00 00
90: 00 00 00 00 1f 08 00 00 00 04 00 00 0e 00 00 00
a0: 03 00 1e 00 00 00 00 00 00 00 00 00 00 00 00 00
b0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
c0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
d0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
e0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
f0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
```

Note: *See ERR051382 "Limit on Max_Read_Request_Size". The read requests of more than 256 B can result in delays on the system bus, and impact the performance of other applications running on the SoC.*

First, boot the board in EP mode. To configure the board, run the following commands in the Linux terminal:

```
$ cd /sys/kernel/config/pci_ep/
$ mkdir functions/pci_epf_test/func1
$ cat functions/pci_epf_test/func1/deviceid
0xffff
$ cat functions/pci_epf_test/func1/vendorid
0xffff
$ echo 0x1131 > functions/pci_epf_test/func1/vendorid
$ echo 0x0000 > functions/pci_epf_test/func1/deviceid
$ echo 16 > functions/pci_epf_test/func1/msi_interrupts
$ ln -s functions/pci_epf_test/func1 controllers/4c380000.pcie-ep/
```

Boot the board in RC mode. Run the following commands in the RC Linux terminal:

```
$ pcitest -i <IRQ enable> -d <DMA enable> -w <write> -r <read> -s <size>
$ pcitest -i 1
$ pcitest -i 1 -d 1 -w -s 4096000
$ pcitest -i 1 -d 1 -r -s 4096000
```

The following are the logs on the RC side:

```
$ root@imx95-19x19-lpddr5-evk:~# pcitest -i 1 -d 1 -w -s 4096000
SET IRQ TYPE TO MSI:        OKAY
WRITE (4096000 bytes):      OKAY
$ root@imx95-19x19-lpddr5-evk:~# pcitest -i 1 -d 1 -r -s 4096000
SET IRQ TYPE TO MSI:        OKAY
READ (4096000 bytes):      OKAY
```

The following are the logs on the EP side:

```
[ 2337.573952] pci_epf_test pci_epf_test.0: READ => Size: 4096000 B, DMA: YES,
 Time: 0.005177833 s, Rate: 791064 KB/s
[ 2699.414678] pci_epf_test pci_epf_test.0: WRITE => Size: 4096000 B, DMA: YES,
 Time: 0.005310875 s, Rate: 820926 KB/s
```

2.4 Results

Figure 8 and Table 1 show the performance results.

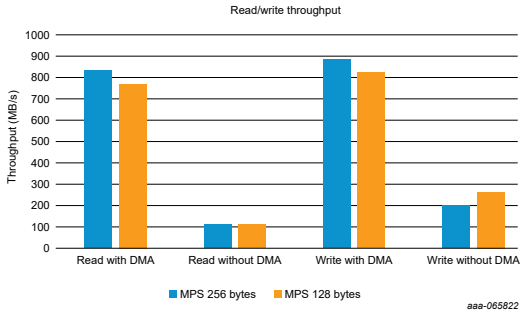

Figure 8. Read/write throughput

Table 1. Performance results

Case	EP (PCIe transfer initiator)	Data transfer type related to i.MX 95	RC	Transfer size	Average throughput (MB/s)
With DMA max payload size (MPS): 256 bytes	i.MX 95	Read from (i.MX 95 EP Outbound MRd)	i.MX 95	4 MB	834.2
	i.MX 95	Write to (i.MX 95 EP Outbound MWr)	i.MX 95	4 MB	885.6
Without DMA MPS: 256 bytes	i.MX 95	Read from (i.MX 95 EP Outbound MRd)	i.MX 95	4 MB	112
	i.MX 95	Write to (i.MX 95 EP Outbound MWr)	i.MX 95	4 MB	200.2
With DMA MPS: 128 bytes	i.MX 95	Read from (i.MX 95 EP Outbound MRd)	i.MX 95	4 MB	774

Table 1. Performance results*...continued*

Case	EP (PCIe transfer initiator)	Data transfer type related to i.MX 95	RC	Transfer size	Average throughput (MB/s)
	i.MX 95	Write to (i.MX 95 EP Outbound MWr)	i.MX 95	4 MB	826.2
Without DMA MPS: 128 bytes	i.MX 95	Read from (i.MX 95 EP Outbound MRd)	i.MX 95	4 MB	112.4
	i.MX 95	Write to (i.MX 95 EP Outbound MWr)	i.MX 95	4 MB	262.6

Note: *The non-DMA transactions are executed through the system bus.*

2.5 Analysis

The throughput performance of the PCIe EP is evaluated under different configurations using two MPS: 256 bytes and 128 bytes. The results are categorized based on whether the DMA is present or not and whether the operation is a read or write.

1. Impact of DMA on throughput:
   - Read with DMA achieves higher throughput ~(800 MB/s to 850 MB/s) compared to read without DMA (~110 MB/s), irrespective of the MPS.
   - Similarly, write with DMA shows a marked improvement ~(832 MB/s to 885 MB/s) over write without DMA (~200 MB/s to 263 MB/s).
2. Influence of MPS:
   - In all cases, increasing the MPS from 128 bytes to 256 bytes provides a modest performance improvement.
   - For DMA cases, throughput increases by approximately 5 % to 7 %.
   - For non-DMA cases, the improvement is present but less impactful and indicates MPS optimization yields the best results when used with DMA.
   - The smaller the payload, the more packets are needed for the same data transfer, increasing overhead and lowering throughput.

2.6 Change MPS

The MPS can be changed in U-Boot or in Linux. Perform the following steps for changing the MPS to 256 B.

1. U-Boot

```
u-boot=> edit mmcargs
edit: setenv bootargs ${cpuidle} ${mcore_args} console=${console} root=
${mmcroot} pci=pcie_bus_perf
```

Boot the board until Linux prompt. The following are the `lspci` logs:

```
0001:00:00.0 0604: 1131:0000 (prog-if 00 [Normal decode])
Control: I/O+ Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping-
 SERR+ FastB2B- DisINTx+
Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort-
 >SERR- <PERR- INTx-
Latency: 0
Interrupt: pin A routed to IRQ 253
Region 0: Memory at a10000000 (32-bit, non-prefetchable) [size=1M]
Bus: primary=00, secondary=01, subordinate=ff, sec-latency=0
```

```
I/O behind bridge: [disabled] [16-bit]
Memory behind bridge: 10100000-102fffff [size=2M] [32-bit]
Prefetchable memory behind bridge: [disabled] [64-bit]
Secondary status: 66MHz- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort-
 <SERR- <PERR-
Expansion ROM at a10300000 [virtual] [disabled] [size=64K]
BridgeCtl: Parity- SERR+ NoISA- VGA- VGA16- MAbort- >Reset- FastB2B-
PriDiscTmr- SecDiscTmr- DiscTmrStat- DiscTmrSERREn-
Capabilities: [40] Power Management version 3
Flags: PMEClk- DSI- D1+ D2+ AuxCurrent=375mA PME(D0+,D1+,D2-,D3hot+,D3cold-)
Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-
Capabilities: [50] MSI: Enable+ Count=1/32 Maskable+ 64bit+
Address: 0000000048050040 Data: 0000
Masking: fffffffe Pending: 00000000
Capabilities: [70] Express (v2) Root Port (Slot-), IntMsgNum 0
DevCap: MaxPayload 256 bytes, PhantFunc 0
ExtTag- RBE+ TEE-IO-
DevCtl: CorrErr- NonFatalErr- FatalErr- UnsupReq-
RlxdOrd+ ExtTag- PhantFunc- AuxPwr- NoSnoop-
MaxPayload 256 bytes, MaxReadReq 256 bytes
DevSta: CorrErr- NonFatalErr- FatalErr- UnsupReq- AuxPwr- TransPend-
LnkCap: Port #0, Speed 8GT/s, Width x1, ASPM L1, Exit Latency L1 <16us
ClockPM- Surprise- LLActRep+ BwNot- ASPMOptComp+
LnkCtl: ASPM Disabled; RCB 128 bytes, LnkDisable- CommClk+
ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-
LnkSta: Speed 8GT/s, Width x1
TrErr- Train- SlotClk+ DLActive+ BWMgmt- ABWMgmt-
RootCap: CRSVisible-
RootCtl: ErrCorrectable- ErrNon-Fatal- ErrFatal- PMEIntEna+ CRSVisible-
RootSta: PME ReqID 0000, PMEStatus- PMEPending-
DevCap2: Completion Timeout: Range ABCD, TimeoutDis+ NROPrPrP+ LTR+
10BitTagComp- 10BitTagReq- OBFF Not Supported, ExtFmt- EETLPPrefix-
EmergencyPowerReduction Not Supported, EmergencyPowerReductionInit-
FRS- LN System CLS Not Supported, TPHComp- ExtTPHComp- ARIFwd+
AtomicOpsCap: Routing- 32bit- 64bit- 128bitCAS-
DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis- ARIFwd-
AtomicOpsCtl: ReqEn- EgressBlck-
IDOReq- IDOCompl- LTR+ EmergencyPowerReductionReq-
10BitTagReq- OBFF Disabled, EETLPPrefixBlk-
LnkCap2: Supported Link Speeds: 2.5-8GT/s, Crosslink- Retimer- 2Retimers- DRS-
LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-
Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-
Compliance Preset/De-emphasis: -6dB de-emphasis, 0dB preshoot
LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+
 EqualizationPhase1+
EqualizationPhase2+ EqualizationPhase3+ LinkEqualizationRequest-
Retimer- 2Retimers- CrosslinkRes: unsupported
Capabilities: [100 v2] Advanced Error Reporting
UESta: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP-
ECRC- UnsupReq- ACSViol- UncorrIntErr- BlockedTLP- AtomicOpBlocked-
 TLPBlockedErr-
PoisonTLPBlocked- DMWrReqBlocked- IDECheck- MisIDETLP- PCRC_CHECK-
 TLPXlatBlocked-
UEMsk: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP-
ECRC- UnsupReq- ACSViol- UncorrIntErr+ BlockedTLP- AtomicOpBlocked-
 TLPBlockedErr-
PoisonTLPBlocked- DMWrReqBlocked- IDECheck- MisIDETLP- PCRC_CHECK-
 TLPXlatBlocked-
UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO- CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+
```

```
ECRC- UnsupReq- ACSViol- UncorrIntErr+ BlockedTLP- AtomicOpBlocked-
 TLPBlockedErr-
PoisonTLPBlocked- DMWrReqBlocked- IDECheck- MisIDETLP- PCRC_CHECK-
 TLPXlatBlocked-
CESta: RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr- CorrIntErr-
 HeaderOF-
CEMsk: RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr+ CorrIntErr+
 HeaderOF+
AERCap: First Error Pointer: 00, ECRCGenCap+ ECRCGenEn- ECRCChkCap+ ECRCChkEn-
MultHdrRecCap- MultHdrRecEn- TLPPfxPres- HdrLogCap-
HeaderLog: 00000000 00000000 00000000 00000000
RootCmd: CERptEn- NFERptEn- FERptEn-
RootSta: CERcvd- MultCERcvd- UERcvd- MultUERcvd-
FirstFatal- NonFatalMsg- FatalMsg- IntMsgNum 0
ErrorSrc: ERR_COR: 0000 ERR_FATAL/NONFATAL: 0000
Capabilities: [148 v1] Secondary PCI Express
LnkCtl3: LnkEquIntrruptEn- PerformEqu-
LaneErrStat: 0
Capabilities: [160 v1] L1 PM Substates
L1SubCap: PCI-PM_L1.2+ PCI-PM_L1.1+ ASPM_L1.2+ ASPM_L1.1+ L1_PM_Substates+
PortCommonModeRestoreTime=10us PortTPowerOnTime=10us
L1SubCtl1: PCI-PM_L1.2- PCI-PM_L1.1+ ASPM_L1.2- ASPM_L1.1-
T_CommonMode=10us LTR1.2_Threshold=26016ns
L1SubCtl2: T_PwrOn=10us
Capabilities: [170 v1] Vendor Specific Information: ID=0006 Rev=0 Len=018 <?>
Kernel driver in use: pcieport
0001:01:00.0 ff00: 1131:0000
Control: I/O- Mem- BusMaster- SpecCycle- MemWINV- VGASnoop- ParErr- Stepping-
 SERR- FastB2B- DisINTx-
Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort-
 >SERR- <PERR- INTx-
Interrupt: pin A routed to IRQ 252
Region 0: Memory at a10244000 (32-bit, non-prefetchable) [disabled] [size=4K]
Region 1: Memory at a10220000 (32-bit, non-prefetchable) [disabled] [size=64K]
Region 2: Memory at a10245000 (32-bit, non-prefetchable) [disabled] [size=4K]
Region 3: Memory at a10240000 (32-bit, non-prefetchable) [disabled] [size=16K]
Region 4: Memory at a10200000 (32-bit, non-prefetchable) [disabled] [size=128K]
Region 5: Memory at a10100000 (32-bit, non-prefetchable) [disabled] [size=1M]
Expansion ROM at a10230000 [virtual] [disabled] [size=64K]
Capabilities: [40] Power Management version 3
Flags: PMEClk- DSI- D1+ D2+ AuxCurrent=375mA PME(D0+,D1+,D2-,D3hot+,D3cold-)
Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-
Capabilities: [50] MSI: Enable- Count=1/16 Maskable+ 64bit+
Address: 0000000000000000 Data: 0000
Masking: 00000000 Pending: 00000000
Capabilities: [70] Express (v2) Endpoint, IntMsgNum 0
DevCap: MaxPayload 256 bytes, PhantFunc 0, Latency L0s unlimited, L1 unlimited
ExtTag- AttnBtn- AttnInd- PwrInd- RBE+ FLReset+ SlotPowerLimit 0W TEE-IO-
DevCtl: CorrErr- NonFatalErr- FatalErr- UnsupReq-
RlxdOrd+ ExtTag- PhantFunc- AuxPwr- NoSnoop- FLReset-
 MaxPayload 256 bytes, MaxReadReq 256 bytes
DevSta: CorrErr- NonFatalErr- FatalErr- UnsupReq- AuxPwr- TransPend-
LnkCap: Port #0, Speed 8GT/s, Width x1, ASPM L1, Exit Latency L1 <16us
ClockPM+ Surprise- LLActRep- BwNot- ASPMOptComp+
LnkCtl: ASPM Disabled; RCB 64 bytes, LnkDisable- CommClk+
ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-
LnkSta: Speed 8GT/s, Width x1
TrErr- Train- SlotClk+ DLActive- BWMgmt- ABWMgmt-
DevCap2: Completion Timeout: Range ABCD, TimeoutDis+ NROPrPrP- LTR+
10BitTagComp- 10BitTagReq- OBFF Not Supported, ExtFmt- EETLPPrefix-
```

```
EmergencyPowerReduction Not Supported, EmergencyPowerReductionInit-
FRS- TPHComp- ExtTPHComp-
AtomicOpsCap: 32bit- 64bit- 128bitCAS-
DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis-
AtomicOpsCtl: ReqEn-
IDOReq- IDOCompl- LTR+ EmergencyPowerReductionReq-
10BitTagReq- OBFF Disabled, EETLPPrefixBlk-
LnkCap2: Supported Link Speeds: 2.5-8GT/s, Crosslink- Retimer- 2Retimers- DRS-
LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-
Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-
Compliance Preset/De-emphasis: -6dB de-emphasis, 0dB preshoot
LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+
 EqualizationPhase1+
EqualizationPhase2+ EqualizationPhase3+ LinkEqualizationRequest-
Retimer- 2Retimers- CrosslinkRes: unsupported
Capabilities: [100 v2] Advanced Error Reporting
UESta: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP-
ECRC- UnsupReq- ACSViol- UncorrIntErr- BlockedTLP- AtomicOpBlocked-
 TLPBlockedErr-
PoisonTLPBlocked- DMWrReqBlocked- IDECheck- MisIDETLP- PCRC_CHECK-
 TLPXlatBlocked-
UEMsk: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP-
ECRC- UnsupReq- ACSViol- UncorrIntErr+ BlockedTLP- AtomicOpBlocked-
 TLPBlockedErr-
PoisonTLPBlocked- DMWrReqBlocked- IDECheck- MisIDETLP- PCRC_CHECK-
 TLPXlatBlocked-
UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO- CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+
ECRC- UnsupReq- ACSViol- UncorrIntErr+ BlockedTLP- AtomicOpBlocked-
 TLPBlockedErr-
PoisonTLPBlocked- DMWrReqBlocked- IDECheck- MisIDETLP- PCRC_CHECK-
 TLPXlatBlocked-
CESta: RxErr+ BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr- CorrIntErr-
 HeaderOF-
CEMsk: RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr+ CorrIntErr+
 HeaderOF+
AERCap: First Error Pointer: 00, ECRCGenCap+ ECRCGenEn- ECRCChkCap+ ECRCChkEn-
MultHdrRecCap- MultHdrRecEn- TLPPfxPres- HdrLogCap-
HeaderLog: 00000000 00000000 00000000 00000000
Capabilities: [148 v1] Secondary PCI Express
LnkCtl3: LnkEquIntrruptEn- PerformEqu-
LaneErrStat: 0
Capabilities: [158 v1] Latency Tolerance Reporting
Max snoop latency: 0ns
Max no snoop latency: 0ns
Capabilities: [160 v1] L1 PM Substates
L1SubCap: PCI-PM_L1.2+ PCI-PM_L1.1+ ASPM_L1.2+ ASPM_L1.1+ L1_PM_Substates+
PortCommonModeRestoreTime=10us PortTPowerOnTime=10us
L1SubCtl1: PCI-PM_L1.2- PCI-PM_L1.1- ASPM_L1.2- ASPM_L1.1-
T_CommonMode=0us LTR1.2_Threshold=26016ns
L1SubCtl2: T_PwrOn=10us
Capabilities: [170 v1] Vendor Specific Information: ID=0006 Rev=0 Len=018 <?>
```

2. Set DEVICE_CONTROL_DEVICE_STATUS[MPS] = 1 on RC and EP in Linux.

```
root@imx95evk:~# setpci -s 0001:00:00.0 CAP_EXP+8.L
00002010
root@imx95evk:~# setpci -s 0001:00:00.0 CAP_EXP+8.L=00002030
root@imx95evk:~# setpci -s 0001:01:00.0 CAP_EXP+8.L
00002010
root@imx95evk:~# setpci -s 0001:01:00.0 CAP_EXP+8.L=00002030
```

```
root@imx95evk:~# lspci -vvn
0001:00:00.0 0604: 1131:0000 (prog-if 00 [Normal decode])
Control: I/O+ Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping-
 SERR+ FastB2B- DisINTx+
Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort-
 >SERR- <PERR- INTx-
Latency: 0
Interrupt: pin A routed to IRQ 253
Region 0: Memory at a10000000 (32-bit, non-prefetchable) [size=1M]
Bus: primary=00, secondary=01, subordinate=ff, sec-latency=0
I/O behind bridge: [disabled] [16-bit]
Memory behind bridge: 10100000-102fffff [size=2M] [32-bit]
Prefetchable memory behind bridge: [disabled] [64-bit]
Secondary status: 66MHz- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort-
 <SERR- <PERR-
Expansion ROM at a10300000 [virtual] [disabled] [size=64K]
BridgeCtl: Parity- SERR+ NoISA- VGA- VGA16- MAbort- >Reset- FastB2B-
PriDiscTmr- SecDiscTmr- DiscTmrStat- DiscTmrSERREn-
Capabilities: [40] Power Management version 3
Flags: PMEClk- DSI- D1+ D2+ AuxCurrent=375mA PME(D0+,D1+,D2-,D3hot+,D3cold-)
Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-
Capabilities: [50] MSI: Enable+ Count=1/32 Maskable+ 64bit+
Address: 0000000048050040 Data: 0000
Masking: fffffffe Pending: 00000000
Capabilities: [70] Express (v2) Root Port (Slot-), IntMsgNum 0
DevCap: MaxPayload 256 bytes, PhantFunc 0
ExtTag- RBE+ TEE-IO-
DevCtl: CorrErr- NonFatalErr- FatalErr- UnsupReq-
RlxdOrd+ ExtTag- PhantFunc- AuxPwr- NoSnoop-
MaxPayload 256 bytes, MaxReadReq 512 bytes
DevSta: CorrErr- NonFatalErr- FatalErr- UnsupReq- AuxPwr- TransPend-
LnkCap: Port #0, Speed 8GT/s, Width x1, ASPM L1, Exit Latency L1 <16us
ClockPM- Surprise+ LLActRep+ BwNot+ ASPMOptComp+
LnkCtl: ASPM Disabled; RCB 128 bytes, LnkDisable- CommClk+
ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-
LnkSta: Speed 8GT/s, Width x1
TrErr- Train- SlotClk+ DLActive+ BWMgmt- ABWMgmt+
RootCap: CRSVisible+
RootCtl: ErrCorrectable- ErrNon-Fatal- ErrFatal- PMEIntEna+ CRSVisible+
RootSta: PME ReqID 0000, PMEStatus- PMEPending-
DevCap2: Completion Timeout: Range ABCD, TimeoutDis+ NROPrPrP+ LTR+
10BitTagComp- 10BitTagReq- OBFF Not Supported, ExtFmt- EETLPPrefix-
EmergencyPowerReduction Not Supported, EmergencyPowerReductionInit-
FRS- LN System CLS Not Supported, TPHComp- ExtTPHComp- ARIFwd+
AtomicOpsCap: Routing- 32bit- 64bit- 128bitCAS-
DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis- ARIFwd-
AtomicOpsCtl: ReqEn- EgressBlck-
IDOReq- IDOCompl- LTR+ EmergencyPowerReductionReq-
10BitTagReq- OBFF Disabled, EETLPPrefixBlk-
LnkCap2: Supported Link Speeds: 2.5-8GT/s, Crosslink- Retimer- 2Retimers- DRS-
LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-
Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-
Compliance Preset/De-emphasis: -6dB de-emphasis, 0dB preshoot
LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+
 EqualizationPhase1+
EqualizationPhase2+ EqualizationPhase3+ LinkEqualizationRequest-
Retimer- 2Retimers- CrosslinkRes: unsupported
Capabilities: [100 v2] Advanced Error Reporting
UESta: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP-
```

```
ECRC- UnsupReq- ACSViol- UncorrIntErr- BlockedTLP- AtomicOpBlocked-
 TLPBlockedErr-
PoisonTLPBlocked- DMWrReqBlocked- IDECheck- MisIDETLP- PCRC_CHECK-
 TLPXlatBlocked-
UEMsk: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP-
ECRC- UnsupReq- ACSViol- UncorrIntErr+ BlockedTLP- AtomicOpBlocked-
 TLPBlockedErr-
PoisonTLPBlocked- DMWrReqBlocked- IDECheck- MisIDETLP- PCRC_CHECK-
 TLPXlatBlocked-
UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO- CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+
ECRC- UnsupReq- ACSViol- UncorrIntErr+ BlockedTLP- AtomicOpBlocked-
 TLPBlockedErr-
PoisonTLPBlocked- DMWrReqBlocked- IDECheck- MisIDETLP- PCRC_CHECK-
 TLPXlatBlocked-
CESta: RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr- CorrIntErr-
 HeaderOF-
CEMsk: RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr+ CorrIntErr+
 HeaderOF+
AERCap: First Error Pointer: 00, ECRCGenCap+ ECRCGenEn- ECRCChkCap+ ECRCChkEn-
MultHdrRecCap- MultHdrRecEn- TLPPfxPres- HdrLogCap-
HeaderLog: 00000000 00000000 00000000 00000000
RootCmd: CERptEn- NFERptEn- FERptEn-
RootSta: CERcvd- MultCERcvd- UERcvd- MultUERcvd-
FirstFatal- NonFatalMsg- FatalMsg- IntMsgNum 0
ErrorSrc: ERR_COR: 0000 ERR_FATAL/NONFATAL: 0000
Capabilities: [148 v1] Secondary PCI Express
LnkCtl3: LnkEquIntrruptEn- PerformEqu-
LaneErrStat: 0
Capabilities: [160 v1] L1 PM Substates
L1SubCap: PCI-PM_L1.2+ PCI-PM_L1.1+ ASPM_L1.2+ ASPM_L1.1+ L1_PM_Substates+
PortCommonModeRestoreTime=10us PortTPowerOnTime=10us
L1SubCtl1: PCI-PM_L1.2- PCI-PM_L1.1+ ASPM_L1.2- ASPM_L1.1-
T_CommonMode=10us LTR1.2_Threshold=26016ns
L1SubCtl2: T_PwrOn=10us
Capabilities: [170 v1] Vendor Specific Information: ID=0006 Rev=0 Len=018 <?>
Kernel driver in use: pcieport
0001:01:00.0 ff00: 1131:0000
Control: I/O- Mem+ BusMaster+ SpecCycle- MemWINV- VGASnoop- ParErr- Stepping-
 SERR- FastB2B- DisINTx+
Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEVSEL=fast >TAbort- <TAbort- <MAbort-
 >SERR- <PERR- INTx-
Latency: 0
Interrupt: pin A routed to IRQ 273
Region 0: Memory at a10244000 (32-bit, non-prefetchable) [size=4K]
Region 1: Memory at a10220000 (32-bit, non-prefetchable) [size=64K]
Region 2: Memory at a10245000 (32-bit, non-prefetchable) [size=4K]
Region 3: Memory at a10240000 (32-bit, non-prefetchable) [size=16K]
Region 4: Memory at a10200000 (32-bit, non-prefetchable) [size=128K]
Region 5: Memory at a10100000 (32-bit, non-prefetchable) [size=1M]
Expansion ROM at a10230000 [virtual] [disabled] [size=64K]
Capabilities: [40] Power Management version 3
Flags: PMEClk- DSI- D1+ D2+ AuxCurrent=375mA PME(D0+,D1+,D2-,D3hot+,D3cold-)
Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-
Capabilities: [50] MSI: Enable+ Count=16/16 Maskable+ 64bit+
Address: 0000000048050040 Data: 0000
Masking: 00000000 Pending: 00000000
Capabilities: [70] Express (v2) Endpoint, IntMsgNum 0
DevCap: MaxPayload 256 bytes, PhantFunc 0, Latency L0s unlimited, L1 unlimited
ExtTag- AttnBtn- AttnInd- PwrInd- RBE+ FLReset+ SlotPowerLimit 0W TEE-IO-
DevCtl: CorrErr- NonFatalErr- FatalErr- UnsupReq-
```

```
RlxdOrd+ ExtTag- PhantFunc- AuxPwr- NoSnoop- FLReset-
MaxPayload 256 bytes, MaxReadReq 512 bytes
DevSta: CorrErr- NonFatalErr- FatalErr- UnsupReq- AuxPwr- TransPend-
LnkCap: Port #0, Speed 8GT/s, Width x1, ASPM L1, Exit Latency L1 <16us
ClockPM+ Surprise- LLActRep- BwNot- ASPMOptComp+
LnkCtl: ASPM Disabled; RCB 64 bytes, LnkDisable- CommClk+
ExtSynch- ClockPM- AutWidDis- BWInt- AutBWInt-
LnkSta: Speed 8GT/s, Width x1
TrErr- Train- SlotClk+ DLActive- BWMgmt- ABWMgmt-
DevCap2: Completion Timeout: Range ABCD, TimeoutDis+ NROPrPrP- LTR+
10BitTagComp- 10BitTagReq- OBFF Not Supported, ExtFmt- EETLPPrefix-
EmergencyPowerReduction Not Supported, EmergencyPowerReductionInit-
FRS- TPHComp- ExtTPHComp-
AtomicOpsCap: 32bit- 64bit- 128bitCAS-
DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis-
AtomicOpsCtl: ReqEn-
IDOReq- IDOCompl- LTR+ EmergencyPowerReductionReq-
10BitTagReq- OBFF Disabled, EETLPPrefixBlk-
LnkCap2: Supported Link Speeds: 2.5-8GT/s, Crosslink- Retimer- 2Retimers- DRS-
LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-
Transmit Margin: Normal Operating Range, EnterModifiedCompliance- ComplianceSOS-
Compliance Preset/De-emphasis: -6dB de-emphasis, 0dB preshoot
LnkSta2: Current De-emphasis Level: -6dB, EqualizationComplete+
 EqualizationPhase1+
EqualizationPhase2+ EqualizationPhase3+ LinkEqualizationRequest-
Retimer- 2Retimers- CrosslinkRes: unsupported
Capabilities: [100 v2] Advanced Error Reporting
UESta: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP-
ECRC- UnsupReq- ACSViol- UncorrIntErr- BlockedTLP- AtomicOpBlocked-
 TLPBlockedErr-
PoisonTLPBlocked- DMWrReqBlocked- IDECheck- MisIDETLP- PCRC_CHECK-
 TLPXlatBlocked-
UEMsk: DLP- SDES- TLP- FCP- CmpltTO- CmpltAbrt- UnxCmplt- RxOF- MalfTLP-
ECRC- UnsupReq- ACSViol- UncorrIntErr+ BlockedTLP- AtomicOpBlocked-
 TLPBlockedErr-
PoisonTLPBlocked- DMWrReqBlocked- IDECheck- MisIDETLP- PCRC_CHECK-
 TLPXlatBlocked-
UESvrt: DLP+ SDES+ TLP- FCP+ CmpltTO- CmpltAbrt- UnxCmplt- RxOF+ MalfTLP+
ECRC- UnsupReq- ACSViol- UncorrIntErr+ BlockedTLP- AtomicOpBlocked-
 TLPBlockedErr-
PoisonTLPBlocked- DMWrReqBlocked- IDECheck- MisIDETLP- PCRC_CHECK-
 TLPXlatBlocked-
CESta: RxErr+ BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr- CorrIntErr-
 HeaderOF-
CEMsk: RxErr- BadTLP- BadDLLP- Rollover- Timeout- AdvNonFatalErr+ CorrIntErr+
 HeaderOF+
AERCap: First Error Pointer: 00, ECRCGenCap+ ECRCGenEn- ECRCChkCap+ ECRCChkEn-
MultHdrRecCap- MultHdrRecEn- TLPPfxPres- HdrLogCap-
HeaderLog: 00000000 00000000 00000000 00000000
Capabilities: [148 v1] Secondary PCI Express
LnkCtl3: LnkEquIntrruptEn- PerformEqu-
LaneErrStat: 0
Capabilities: [158 v1] Latency Tolerance Reporting
Max snoop latency: 0ns
Max no snoop latency: 0ns
Capabilities: [160 v1] L1 PM Substates
L1SubCap: PCI-PM_L1.2+ PCI-PM_L1.1+ ASPM_L1.2+ ASPM_L1.1+ L1_PM_Substates+
PortCommonModeRestoreTime=10us PortTPowerOnTime=10us
L1SubCtl1: PCI-PM_L1.2- PCI-PM_L1.1- ASPM_L1.2- ASPM_L1.1-
T_CommonMode=0us LTR1.2_Threshold=26016ns
```

```
L1SubCtl2: T_PwrOn=10us
Capabilities: [170 v1] Vendor Specific Information: ID=0006 Rev=0 Len=018 <?>
Kernel driver in use: pci-endpoint-test
```

3 Acronyms

Table 2 lists the acronyms used in this document.

Table 2. Acronyms

Acronym	Description
DMA	Direct memory access
EP	Endpoint
IoT	Internet of Things
MPS	Max payload size
MSI	Message signaled interrupts
PCIe	Peripheral component interconnect express
RC	Root complex

4 References

Table 3 lists the references used to supplement this document.

Table 3. Related documentation/resources

Document	Link/how to access
i.MX 95 Hardware Design Guide	UG10210
i.MX Yocto Project User's Guide	UG10164
i.MX Linux User's Guide	IMXLUG_6.6.23_2.0.0
imx-manifest	imx-manifest
PCIe Specification	PCIe Specifications
PCI Express Jumper Cable Assemblies	PCI Express Jumper Cable Assemblies
PCI Express 4.0 Cable Assembly	PCI Express 4.0 Cable Assembly
PCI Test User Guide	PCI Test User Guide

5 Revision history

Table 4 summarizes the revisions to this document.

Table 4. Revision history

Revision number	Release date	Description
AN14760 v.2.0	21 April 2026	Initial public release
AN14760 v.1.1	11 September 2025	Updated Section 2.3
AN14760 v.1.0	12 August 2025	Initial NDA release

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