

# AN15043

## Power Architecture and Power Supply Schemes on the MIMXRT700-EVK

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Application note

### Document information

Information	Content
Keywords	AN15043, i.MX RT700, MIMXRT700-EVK, power architecture, power supply schemes
Abstract	This application note introduces the i.MX RT700 power architecture with a focus on the different power rails, and their roles within the system. It presents four EVK power supply schemes, explains their implementation and design characteristics, and provides guidance for understanding and selecting suitable power configurations.



## 1 Introduction

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The i.MX RT700 features a flexible power management architecture. It supports multiple power supply configurations and enables different system design approaches depending on an integration level and power supply resources.

On the MIMXRT700-EVK, four representative supply configurations are implemented to demonstrate typical design options. These included solutions based on an external PMIC (such as PCA9422), and configurations that use the on-chip DC-DC converter and LDO regulators.

This application note introduces the i.MX RT700 power architecture with a focus on the different power rails, and their roles within the system. It presents four EVK power supply schemes, explains their implementation and design characteristics, and provides guidance for understanding and selecting suitable power configurations.

## 2 i.MX RT700 power architecture overview

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The i.MX RT700 integrates a flexible power architecture that consists of multiple power domains and power rails, enables fine-grained power control across different functional blocks. This architecture allows each domain to be independently powered on, powered down, or placed into low-power states according to system performance requirements that improve overall power efficiency and system flexibility.

As shown in [Figure 1](#), the functional blocks are organized into multiple power domains, each associated with a specific power rail. Each domain groups related modules that enable independent control and optimized power management.

Key processing domains, such as the compute domain (VDD2\_COMP) and the sense domain (VDD1\_SENSE), are separated to allow independent control. For example, the compute domain includes CPU0, NPU, and related processing modules, while the sense domain contains CPU1 and peripheral modules for always-on or low-power operation.

Power Architecture and Power Supply Schemes on the MIMXRT700-EVK

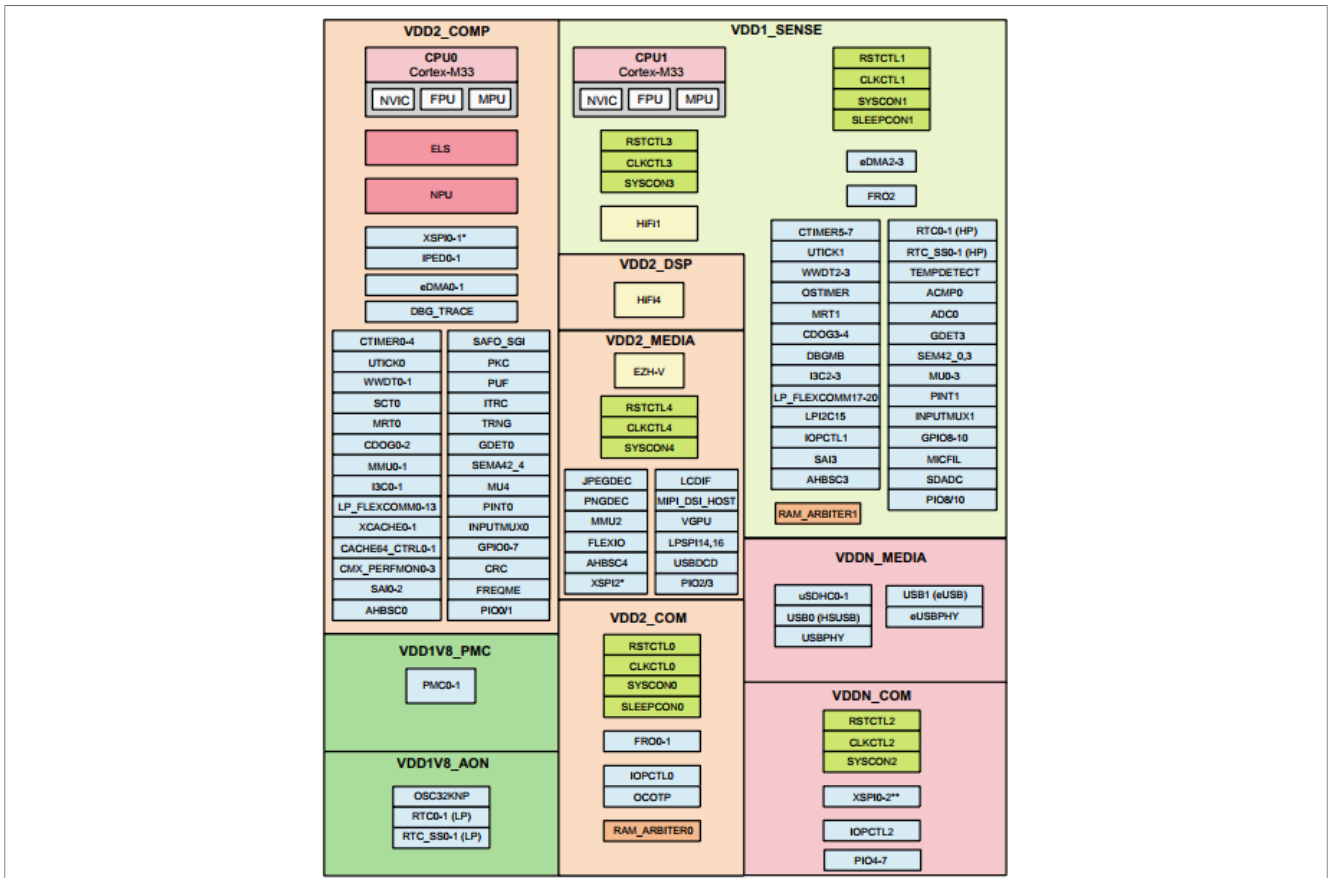


Figure 1. Power architecture block diagram

In addition to compute and sensing domains, the i.MX RT700 defines dedicated domains for DSP (VDD2\_DSP), media processing (VDD2\_MEDIA, VDDN\_MEDIA), and common system functions (VDD2\_COM, and VDDN\_COM). These domains are mapped to different power rails including VDD1, VDD2, VDDN, and 1.8 V rails according to their performance and voltage requirements. These power rails enable the independent control and optimized power management across different functional blocks.

To supply these power rails, the i.MX RT700 supports the following two main approaches, using the:

- On-chip Power Management Controller (PMC)
- An external Power Management Integrated Circuit (PMIC)

The PMC integrates an on-chip DC-DC converter with on-chip LDO regulators to generate and regulate the required voltages internally. In contrast, an external PMIC can supply the main power rails directly.

As shown in [Figure 2](#) and [Figure 3](#), these two approaches define different power supply paths to the core rails (VDD1, VDD2, and VDDN). This approach enables flexible system-level power design that depends on the integration, cost, and system requirements.

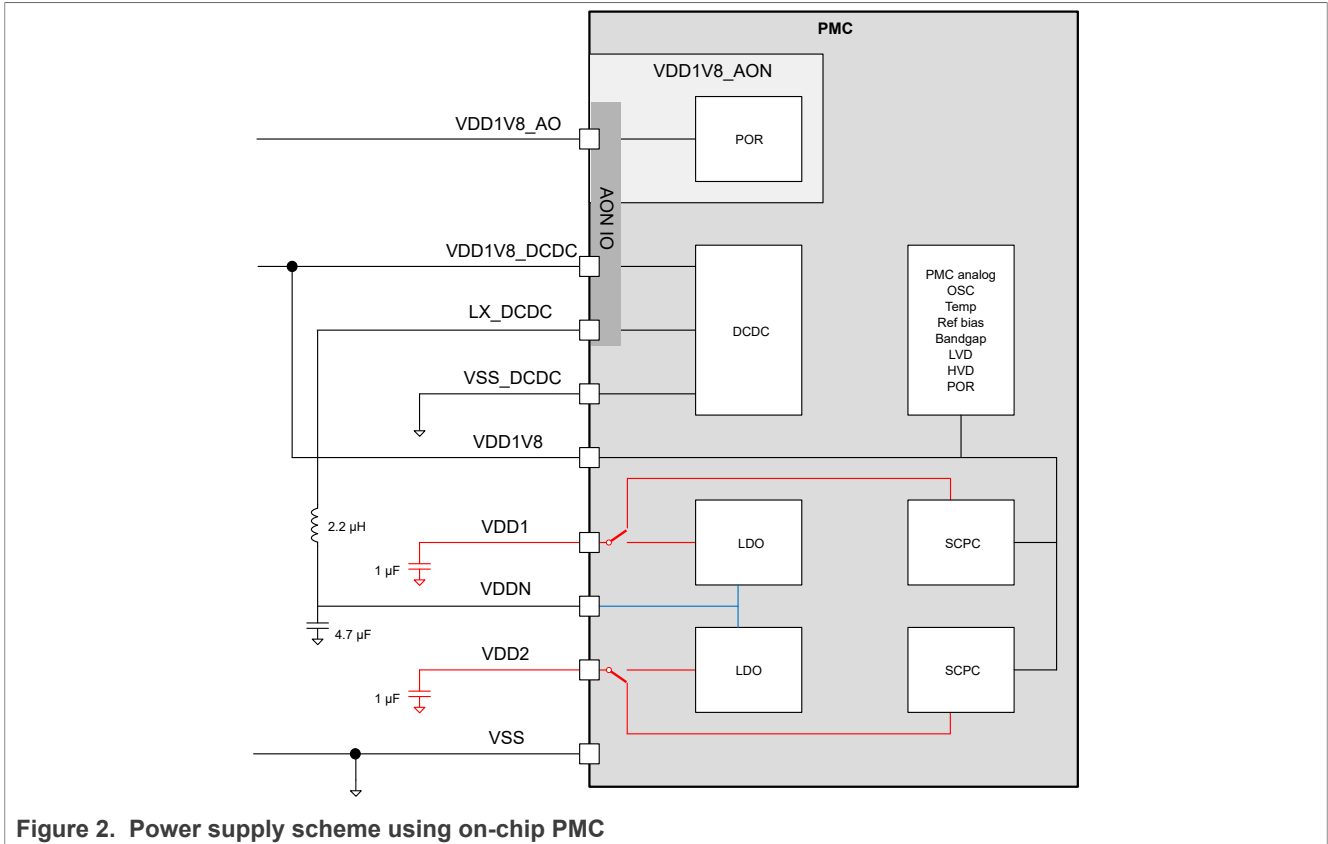


Figure 2. Power supply scheme using on-chip PMC

Figure 2 shows the power supply scheme based on the on-chip PMC. In this configuration, a 1.8 V supply is used as the input to the on-chip DC-DC converter. This converter generates the VDDN rail as the primary internal supply. During normal operation, the VDD1 and VDD2 rails are derived from VDDN through on-chip LDO regulators.

In low-power retention modes, the on-chip Switched-Capacitor Power Converters (SCPC) can optionally supply VDD1 and VDD2 directly from the 1.8 V rail. This supply from the rail allows the on-chip LDOs to be powered down. This architecture enables flexible power control by combining on-chip DC-DC, on-chip LDO, and on-chip SCPC. This combination reduces the complexity of the external power design and supports low-power system operation.

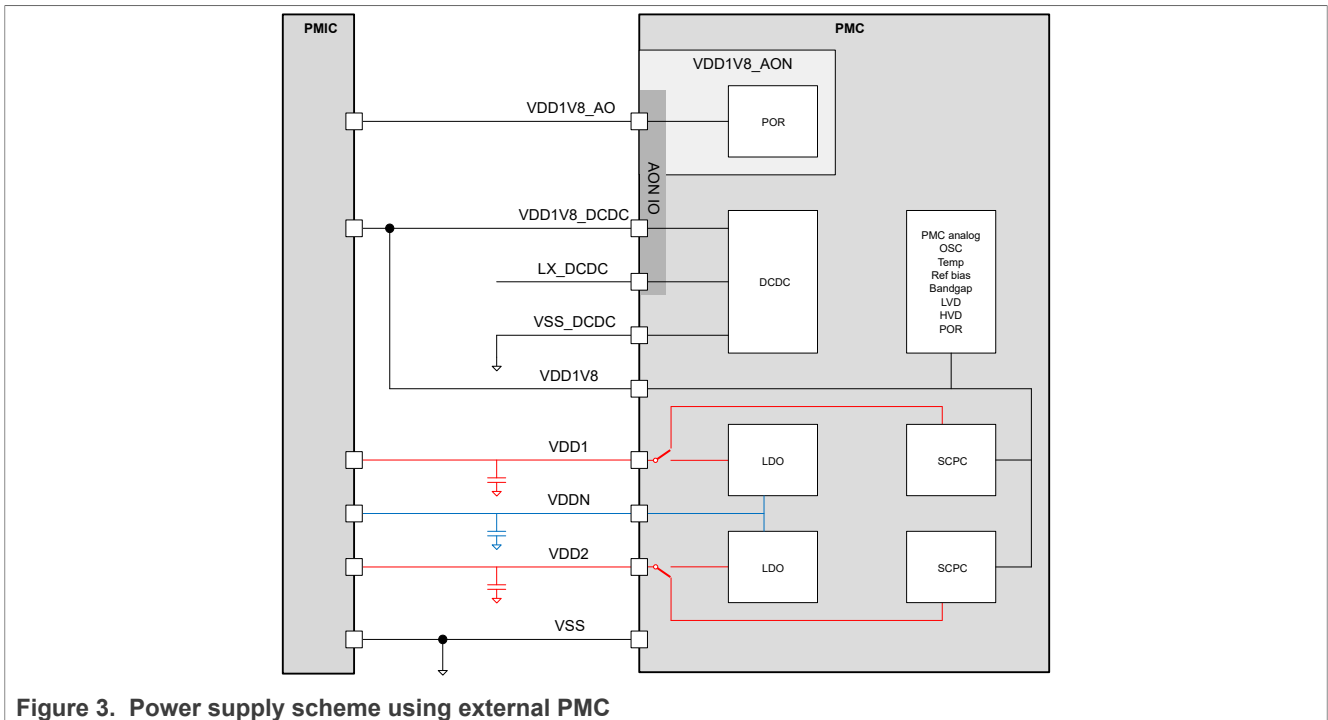


Figure 3. Power supply scheme using external PMC

Figure 3 shows the power supply scheme using an external PMIC, such as PCA9422. In this configuration, the PMIC directly provides multiple regulated power rails, including VDD1, VDD2, and VDDN. With PCA9422, a single PMIC device is sufficient to supply all the required power rails for the i.MX RT700. It enables a highly integrated and simplified power solution.

Compared to the on-chip PMC approach, this scheme offers greater flexibility in power rail control and allows independent optimization of each rail. In addition, by reducing internal conversion stages, higher overall power efficiency can be achieved.

### 3 i.MX RT700 power rails description

The i.MX RT700 uses multiple power rails to supply different functional domains that enable optimized power distribution across the system. These power rails include core supply rails, 1.8 V supply rails, I/O supply rails, and other dedicated rails for specific functions. The main power rails are described as follows:

- VDD1V8: 1.8 V supply for the PMC. This rail provides the base supply for internal power management functions.
- VDD1V8\_AO: 1.8 V supply for always-on logic (VDD1V8\_AON) that supports system functions that remain powered in Low-power modes.
- VDD1V8\_DCDC: 1.8 V input supply for the on-chip DC-DC converter.
- VDDA\_1V8: 1.8 V supply for analog modules.
- VDDN: supply for the VDDN\_COM domain, including clock sources, and high-speed logic in the VDDN\_MEDIA domain. The on-chip DC-DC can generate the VDDN rail or an external supply can provide it.
- VDD1: supply for the VDD1\_SENSE domain.
- VDD2: supply for high-performance domains, including VDD2\_COMP, VDD2\_DSP, VDD2\_MEDIA, and VDD2\_COM.
- VDDIO\_x: I/O supply rails that provide appropriate voltage levels for GPIO interfaces.

Among the power rails, VDD1, VDD2, and VDDN are the primary core supply rails and are critical for system operation. The achievable maximum performance of the system depends on how VDD1 and VDD2 are supplied.

When VDD1 and VDD2 are supplied from an external source, the i.MX RT700 can achieve its maximum supported performance. With a supply voltage of 1.1 V or higher, CPU0 can reach up to 325 MHz, and CPU1 can operate up to 250 MHz.

In contrast, when VDD1 and VDD2 are generated using the on-chip LDO regulators, the maximum achievable frequency is reduced. Under this configuration, CPU0 operation is limited to 250 MHz, and CPU1 is limited to 205 MHz. This configuration provides a more integrated solution, while operating at a lower maximum performance compared to external supply.

Therefore, an external supply allows the i.MX RT700 to operate at its full performance capability, while an on-chip LDO-based supply results in reduced maximum operating frequency compared to external supply. This difference highlights the impact of the selected power supply scheme on system performance.

## 4 Power supply schemes on the MIMXRT700-EVK

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The following are the power supply schemes on the MIMXRT700-EVK.

### 4.1 Overview of MIMXRT700-EVK power configurations

The MIMXRT700-EVK provides a highly flexible power solution that supports multiple power supply configurations through configurable jumper settings. As shown in [Figure 4](#), the MIMXRT700-EVK integrates an external PMIC (PCA9422) with discrete DC-DC converters and LDO regulators. This combination allows different system-level power architectures to be evaluated on a single platform.

Power Architecture and Power Supply Schemes on the MIMXRT700-EVK

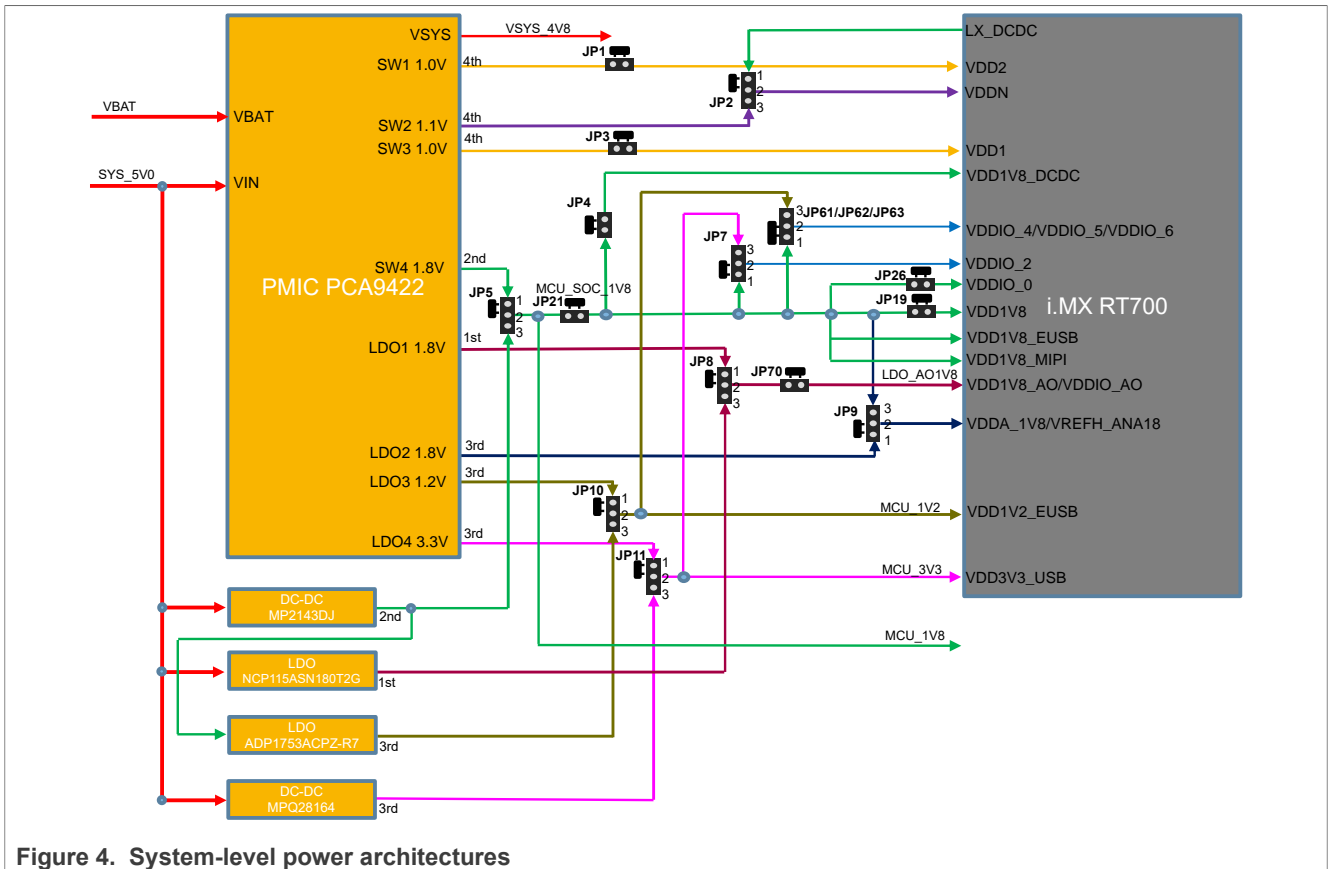


Figure 4. System-level power architectures

By configuring the onboard jumpers, different supply paths can be selected for the core power rails VDDN, VDD1, and VDD2. These rails can be supplied directly through the external PMIC, generated using the on-chip DC-DC converter and on-chip LDO regulators, or supplied through a hybrid combination of internal and external sources.

Although the MIMXRT700-EVK includes a PMIC for evaluation flexibility, the power supply schemes described in this section represent general system design approaches. In practical applications, the external supply rails can be generated using a PMIC or discrete DC-DC and LDO regulators.

Four representative power supply schemes are supported on the MIMXRT700-EVK, as described in the following sections.

### 4.2 Option 1 – fully external PMIC supply (default)

Option 1 uses the external PMIC (PCA9422) to supply all core power rails VDDN/VDD1/VDD2 directly, as shown in [Figure 5](#).

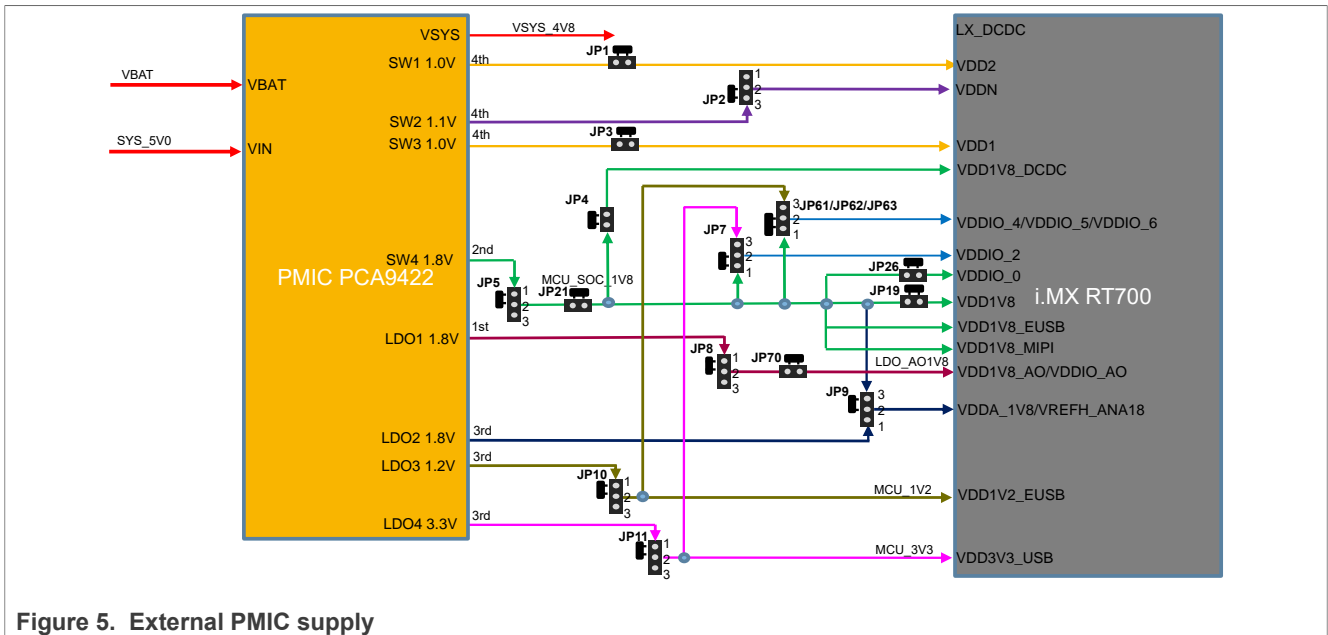


Figure 5. External PMIC supply

In this configuration:

- External PMIC supplies VDDN, VDD1, and VDD2.
- The on-chip DC-DC converter and on-chip LDO regulators are not used for generating these rails.

This configuration is the default configuration of the MIMXRT700-EVK and enables the i.MX RT700 to operate at its maximum supported performance.

This scheme represents a typical PMIC-based power architecture, where a single device generates the multiple regulated outputs, providing a compact and highly integrated power solution.

Jumper settings:

- JP1 (1-2), JP2 (2-3), JP3 (1-2), JP4 (1-2), JP5 (1-2)
- JP7 (1-2), JP8 (1-2), JP9 (2-3), JP10 (1-2), JP11 (1-2)
- JP19 (1-2), JP21 (1-2), JP26 (1-2), JP61 (1-2), JP62 (1-2), JP63 (1-2)

### 4.3 Option 2 – on-chip DC-DC and LDO supply

Option 2 uses the on-chip DC-DC converter with the on-chip LDO regulators to generate the core power rails, as shown in [Figure 6](#).

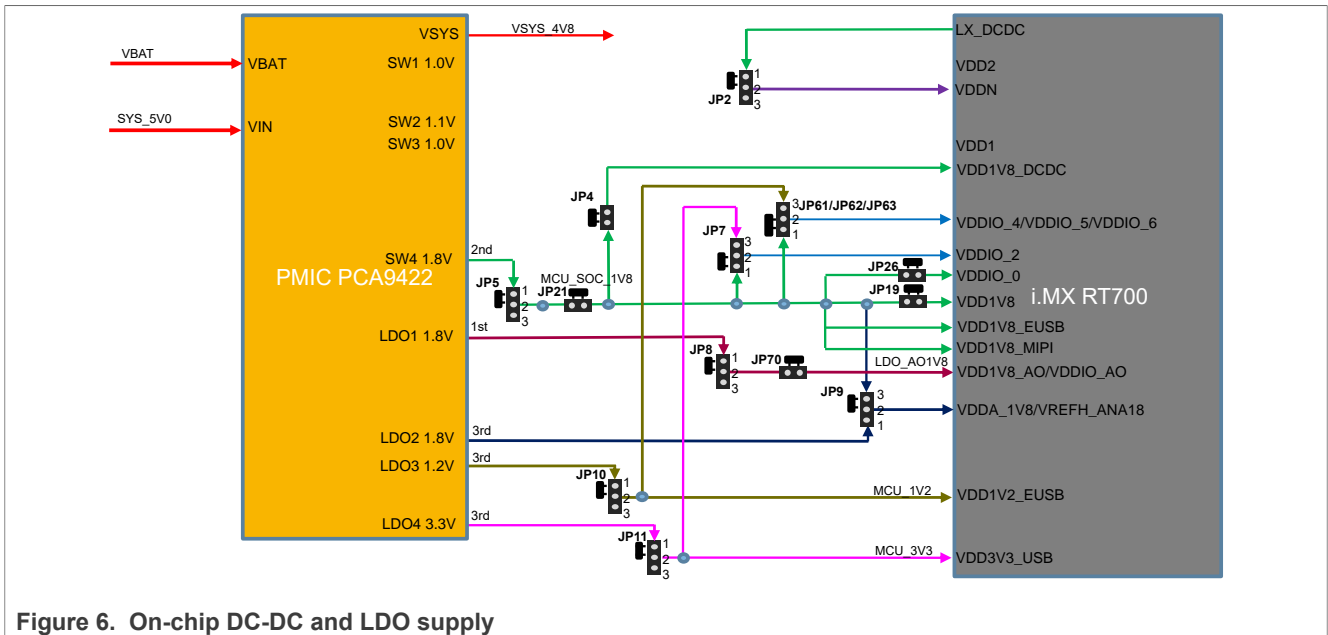


Figure 6. On-chip DC-DC and LDO supply

In this configuration:

- The on-chip DC-DC converter generates the VDDN.
- The on-chip LDO regulators supply the VDD1 and VDD2.

This scheme reduces the number of required external power rails, as the core voltages are generated internally. As a result, fewer external regulators or PMIC outputs are needed, simplifying the overall power tree design.

This approach provides a higher level of integration and is suitable for designs where minimizing external components and reducing system complexity are important considerations.

Jumper settings:

- JP1 (Open), JP2 (1-2), JP3 (Open), JP4 (1-2), JP5 (1-2)
- JP7 (1-2), JP8 (1-2), JP9 (2-3), JP10 (1-2), JP11 (1-2)
- JP19 (1-2), JP21 (1-2), JP26 (1-2), JP61 (1-2), JP62 (1-2), JP63 (1-2)

#### 4.4 Option 3 – hybrid supply

Option 3 implements a hybrid power architecture. It combines the on-chip power generation and external supply, as shown in [Figure 7](#).

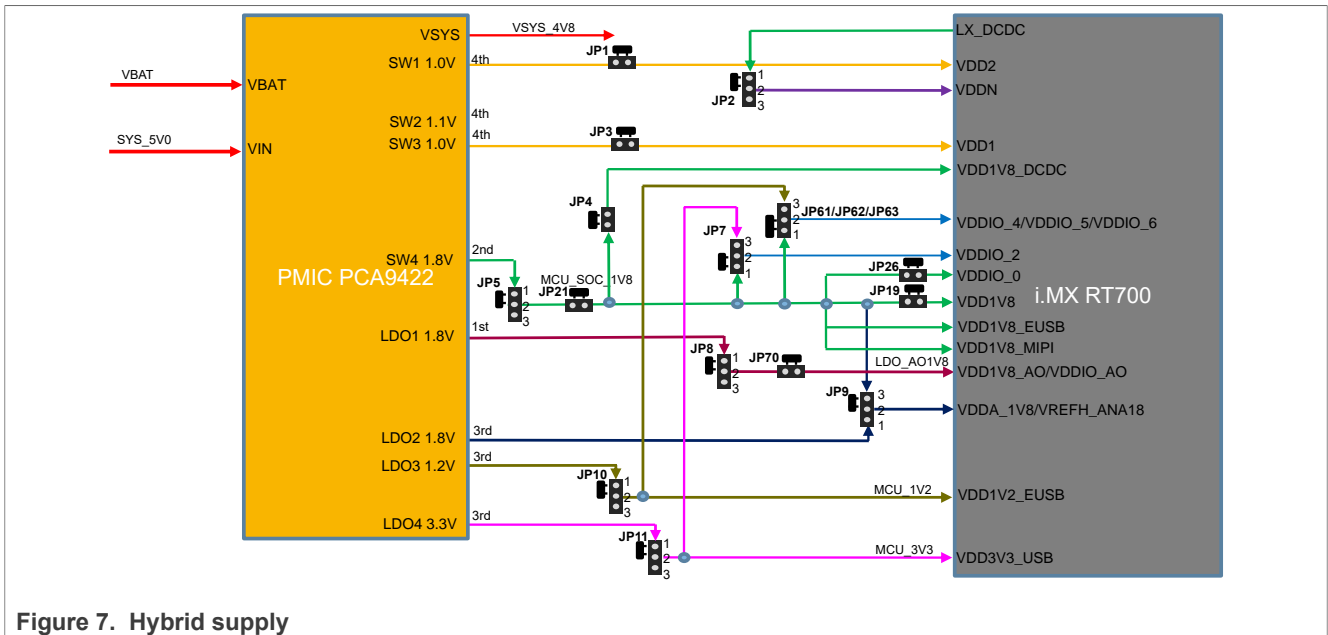


Figure 7. Hybrid supply

In this configuration:

- The on-chip DC-DC converter generates the VDDN.
- The external regulators from PMIC on the MIMXRT700-EVK supply the VDD1 and VDD2.

This scheme uses the internal DC-DC converter to generate the intermediate rail VDDN, while external regulators provide VDD1 and VDD2 to support higher performance operation.

Compared to [Section 4.3 "Option 2 – on-chip DC-DC and LDO supply"](#), this approach improves the achievable performance of the compute and sensing domains, while still reducing part of the external power design complexity.

This hybrid configuration is suitable for applications that require a balance between performance capability and system integration.

Jumper settings:

- JP1 (1-2), JP2 (1-2), JP3 (1-2), JP4 (1-2), JP5 (1-2)
- JP7 (1-2), JP8 (1-2), JP9 (2-3), JP10 (1-2), JP11 (1-2)
- JP19 (1-2), JP21 (1-2), JP26 (1-2), JP61 (1-2), JP62 (1-2), JP63 (1-2)

#### 4.5 Option 4 – on-chip DC-DC and LDO supply without PMIC

Option 4 uses the same on-chip power generation structure as [Section 4.3 "Option 2 – on-chip DC-DC and LDO supply"](#), but without using an external PMIC, as shown in [Figure 8](#). Unlike [Section 4.3 "Option 2 – on-chip DC-DC and LDO supply"](#) that still relies on a PMIC for input supply. This configuration completely removes the PMIC and uses discrete power components.

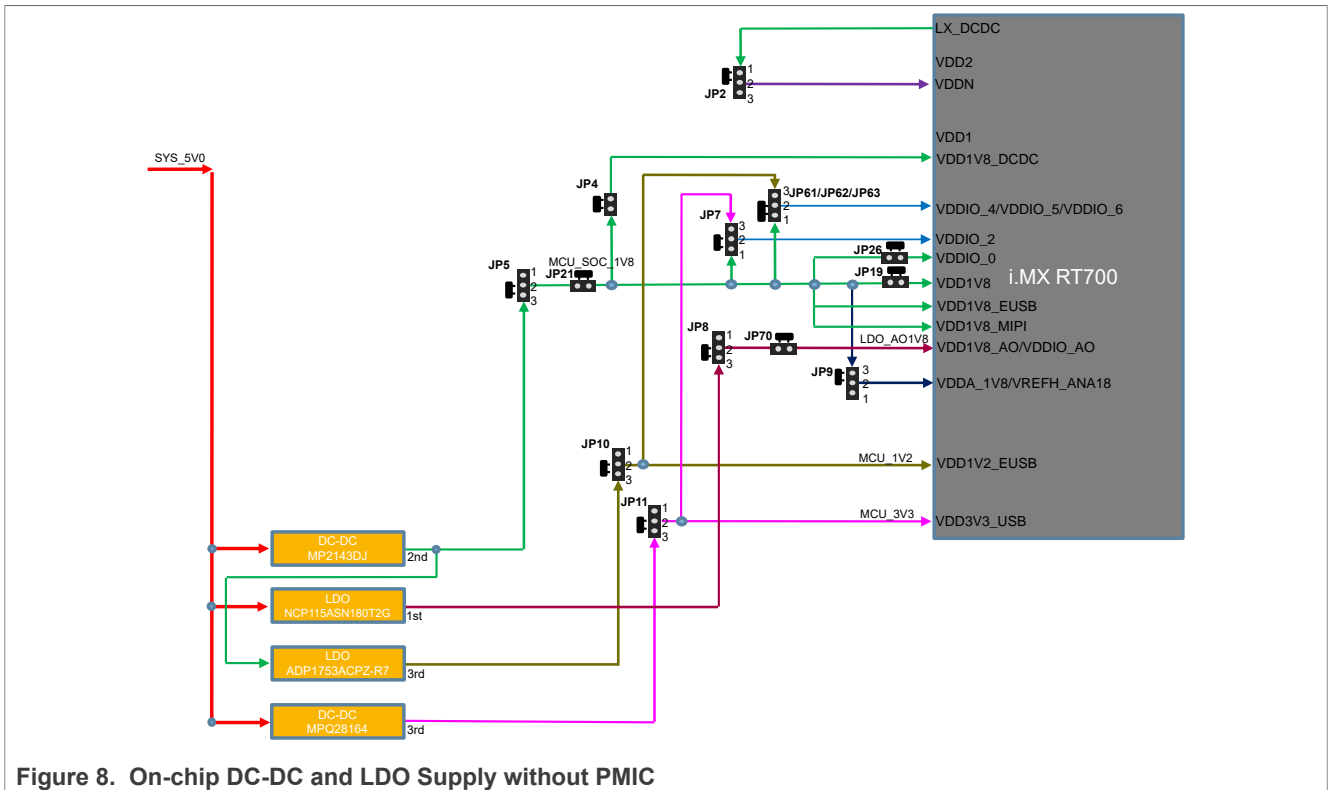


Figure 8. On-chip DC-DC and LDO Supply without PMIC

In this configuration:

- The on-chip DC-DC converter generates the VDDN.
- The on-chip LDO regulators supply the VDD1 and VDD2.
- All external supply rails are generated using discrete DC-DC converters and LDO regulators.

This scheme represents a fully discrete system-level power design without a PMIC. It provides maximum flexibility for system power design that allows designers to select external regulators optimized for specific application requirements.

Jumper settings:

- JP1 (Open), JP2 (1-2), JP3 (Open), JP4 (1-2), JP5 (2-3)
- JP7 (1-2), JP8 (2-3), JP9 (1-2), JP10 (2-3), JP11 (2-3)
- JP19 (1-2), JP21 (1-2), JP26 (1-2), JP61 (1-2), JP62 (1-2), JP63 (1-2)

## 5 Conclusion

The four power supply schemes supported on the MIMXRT700-EVK represent different approaches for generating the core rails VDDN, VDD1, and VDD2. Their characteristics can be compared as follows:

- [Section 4.2 "Option 1 – fully external PMIC supply \(default\)"](#): The external PMIC supplies the VDDN, VDD1, and VDD2. Provides full performance capability with a highly integrated PMIC-based power solution.
- [Section 4.3 "Option 2 – on-chip DC-DC and LDO supply"](#): The on-chip DC-DC converter generates the VDDN, while the on-chip LDO regulators supply the VDD1 and VDD2. Reduces the number of required external power rails and simplifies the power design, with reduced maximum performance.

- [Section 4.4 "Option 3 – hybrid supply"](#): The on-chip DC-DC converter generates the VDDN, while the external regulators supply the VDD1 and VDD2. Provides a balance between system integration and performance, enabling higher performance than fully on-chip supply.
- [Section 4.5 "Option 4 – on-chip DC-DC and LDO supply without PMIC"](#) The on-chip DC-DC converter and LDO regulators generate the core rails, while all external supplies are implemented using discrete power devices. Eliminates the need for a PMIC and offers maximum flexibility in system-level power design.

The four power supply schemes described above are representative examples that the MIMXRT700-EVK provides for evaluation purposes. They are not exhaustive, and more power supply architectures can be realized based on different combinations of on-chip regulators and external power components.

As an evaluation platform, the MIMXRT700-EVK is designed to support early-stage validation of different power architectures. In practical product designs, the final power solution is typically customized and optimized according to specific application requirements, such as:

- Performance targets
- Power efficiency
- Board space
- System cost

Among the available options, the fully external PMIC-based solution [Section 4.2 "Option 1 – fully external PMIC supply \(default\)"](#) is recommended for most applications. This configuration enables the i.MX RT700 to achieve its full performance capability and aligns with the official i.MX RT700 software ecosystem. The provided SDK and low-power demonstration examples are developed and validated based on this PMIC-based approach.

In addition, the power consumption data specified in the *i.MX RT700 Crossover Microcontroller Data Sheet (IMXRT700EC)* is characterized using this configuration with PCA9422. It ensures optimized power performance and accurate reference results.

The MIMXRT700-EVK configurations serve as reference implementations for evaluation. The PMIC-based solution offers the most mature and validated approach and is recommended as the baseline for system design. Alternative schemes can be further adopted and optimized depending on specific application requirements.

## 6 Acronyms

[Table 1](#) lists the acronyms used in this document.

Table 1. Acronyms

Acronym	Description
DSP	Digital Signal Processor
EVK	Evaluation Kit
I/O	Input/Output
LDO	Low-Dropout Regulator
PMC	Power Management Controller
PMIC	Power Management Integrated Circuit
SCPC	Switched Capacitor Power Converters

## 7 References

1. i.MX RT700 Crossover Microcontroller Data Sheet ([IMXRT700EC](#))

2. i.MX RT700 Crossover Microcontroller Reference Manual ([IMXRT700RM](#))
3. [MIMXRT700-EVK Schematic](#)

## 8 Revision history

[Table 2](#) summarizes revisions to this document.

**Table 2. Revision history**

Document ID	Release date	Description
AN15043 v.1.0	4 June 2026	Initial public release

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