AN15074

S32Z2/E2 Power Estimation Guide

Rev. 1.0 — 19 June 2026 **Application note**

Document information

Information	Content
Keywords	S32Z2, S32E2
Abstract	This application note supports Power Estimation for S32Z2/E2 devices. It describes the basic components and lists the steps to configure and estimate the power consumption of various cores and peripherals on S32Z2/E2.

1 Introduction

This application note supports Power Estimation for S32Z2/E2 devices. It describes the basic components and lists the steps to configure and estimate the power consumption of various cores and peripherals on S32Z2/E2.

This document helps enable embedded system designers to gain insights and design energy-efficient automotive applications. It helps the system developer to estimate and design an optimal power supply scheme for their application use case.

The document uses power consumption data from the device data sheet and additional real measurements or design estimates. The power consumption values provided in this document are estimates for reference only. Actual performance can vary depending on silicon process variations, system configuration, and operating conditions. The S32Z2/E2 Data Sheet defines the official electrical specifications. In the event of any discrepancy between this application note and the data sheet, the data sheet takes precedence.

2 Common terms used

Static consumption – This is the minimum consumption when the device is powered. It is always present irrespective of any activity.

Dynamic consumption – This depends on the activity of the module and must be added to the static consumption to derive total consumption.

I/O – Input-output pads of the S250 silicon, refer to the IOMUX sheet in S32Z2/E2 Reference Manual ref.[1], ref.[2].

3 Tools

S32Z2E2_Power_Estimator – Provides an estimation of power consumption by the chip when using various combinations of cores and peripherals at various usage rates. See details on its usage in Section 4.

S32Z2E2_IO_Power_Calculator – Configures I/O activity and estimates dynamic current for the I/O supply rails. See details on its usage in Section 5.

4 S32Z2/E2 Power Estimator Tool

The S32Z2E2 power estimator is an Excel tool that estimates the typical current consumption the device consumes based on peripheral and core activity. This calculator only calculates VDD (0.8V) currents. Use in combination with the I/O power calculator to give the full device power. These values are for reference only, for exact specifications refer to the S32ZE Data Sheet ref.[3], ref.[4].

The tool can be found here:

S32Z2E2_Power_Estimation.xlsx

4.1 Summary Sheet

The “Summary” sheet in Figure 1 shows the base, core, and peripheral power combined as measured on the 0.8V core rail, resulting in the total dynamic power consumption for a given device setup. This sheet is not modifiable by the user.

CORE & PERIPHERAL POWER	VDD (0.8V)
BASE POWER	490.555301
CORE POWER (mW)	-5.485465846
PERIPHERAL POWER (mW)	6.9589
TOTAL CORE AND PERIPHERAL POWER (mW)	492.0287351

Figure 1. Summary sheet of total core and peripheral power

Note, the values computed are dynamic power and are applicable regardless of operating temperature. A base dynamic power measurement on the 0.8V rail of the SMU running WFI (Wait for Interrupt) at various frequencies and cache states is computed in this tool for reference (the base dynamic power measurements were measured on S32E2 50913 Rev A EVB).

4.2 Core Activity Sheet

The “Core Activity” sheet includes options for selecting partition state and configuration, core state and configuration, and core cache on/off and utilization rate. The total core power consumption is computed based on factors such as core enablement, operating frequency, and activity factor.

User-configurable fields include CORE FREQ, PARTITION STATE, PARTITION CONFIG, CORE STATE, CORE CACHE STATE, and CORE ACTIVITY FACTOR. How to configure each field is described in the list below, and the number and color for each field described corresponds to the feature number and the box color the field is highlighted with in Figure 2.

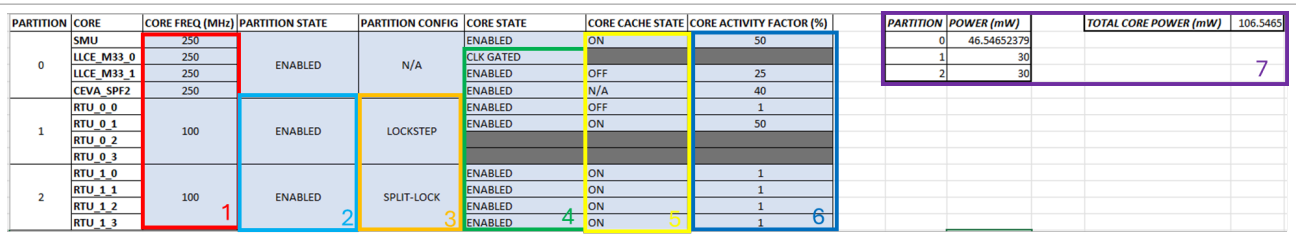

Figure 2. Core Activity Sheet with user-configurable fields highlighted

1. CORE FREQ (boxed in red), for the cores listed in Partition 0, the valid input frequencies are 1-400 MHz, and for cores in Partitions 1 and 2, the valid input frequencies are 1-1000 MHz. An error message appears if an invalid frequency is entered.
2. PARTITION STATE (boxed in light blue) is always enabled for Partition 0. However, for Partitions 1 and 2, the drop-down list in the cell can be used to select CLK GATED, CLK ENABLED & IN RST, or ENABLED.
3. PARTITION CONFIG (boxed in orange) is not selectable for Partition 0. However, for Partitions 1 and 2, the drop-down list in the cell can be used to select the LOCKSTEP or SPLIT-LOCK configuration for the cores.
4. CORE STATE (boxed in green) is always enabled for the SMU core in Partition 0. However, for the other Partition 0 cores and cores in Partitions 1 and 2, the drop-down list in the cell can be used to select the following options for each as shown in Figure 3.

SMU	ENABLED		
LLCE_M33_0	CLK GATED	ENABLED	
LLCE_M33_1	CLK GATED	ENABLED	
CEVA_SPF2	CLK GATED	CLK ENABLED & IN RST	ENABLED
RTU_0_0	CLK GATED	CLK ENABLED & IN RST	ENABLED
RTU_0_1	CLK GATED	CLK ENABLED & IN RST	ENABLED
RTU_0_2	CLK GATED	CLK ENABLED & IN RST	ENABLED
RTU_0_3	CLK GATED	CLK ENABLED & IN RST	ENABLED
RTU_1_0	CLK GATED	CLK ENABLED & IN RST	ENABLED
RTU_1_1	CLK GATED	CLK ENABLED & IN RST	ENABLED
RTU_1_2	CLK GATED	CLK ENABLED & IN RST	ENABLED
RTU_1_3	CLK GATED	CLK ENABLED & IN RST	ENABLED

Figure 3. CORE STATE options

5. CORE CACHE STATE (boxed in yellow) is not selectable for the CEVA_SPF2 core in Partition 0. However, for all other cores in Partitions 0, 1 and 2, the drop-down list in the cell can be used to select ON or OFF.
6. Cells in the CORE ACTIVITY FACTOR column (boxed in dark blue) accept an input of 1-100 for how often the peripheral is being used.
7. Each partition has its individual total power calculated, and the total core power is the sum of the individual partitions' power (boxed in purple).

Note, if PARTITION STATE is set to CLK GATED or CLK ENABLED & IN RST for Partitions 1 and/ or 2, the configurable cells for PARTITION CONFIG, CORE STATE, CORE CACHE STATE, and CORE ACTIVITY FACTOR for all the cores will be grayed out and unmodifiable. Similarly, if CORE STATE is set to CLK GATED or CLK ENABLED & IN RST, then the configurable cells for CORE CACHE STATE and CORE ACTIVITY FACTOR will be grayed out and unmodifiable for that core. These features are shown in Figure 4.

PARTITION	CORE	CORE FREQ (MHz)	PARTITION STATE	PARTITION CONFIG	CORE STATE	CORE CACHE STATE	CORE ACTIVITY FACTOR (%)
0	SMU	250	ENABLED	N/A	ENABLED	ON	50
	LLCE_M33_0	250			CLK GATED		
	LLCE_M33_1	250			ENABLED	OFF	25
	CEVA_SPF2	250			CLK ENABLED & IN RST		
1	RTU_0_0	100	CLK ENABLED & IN RST				
	RTU_0_1						
	RTU_0_2						
	RTU_0_3						
2	RTU_1_0	100	ENABLED	SPLIT-LOCK	ENABLED	ON	1
	RTU_1_1				ENABLED	ON	1
	RTU_1_2				ENABLED	ON	1
	RTU_1_3				ENABLED	ON	1

Figure 4. Partition 1 is clock-gated, core LLCE_M33_0 is clock-gated, and core CEVA_SPF2 is clock-enabled and in reset.

Note, only for Partitions 1 and 2, that if PARTITION CONFIG is selected as LOCKSTEP (assuming PARTITION STATE is ENABLED), then all the configurable cells after PARTITION CONFIG (CORE STATE, CORE CACHE STATE, and CORE ACTIVITY FACTOR) will be grayed out and unmodifiable for cores RTU_0_2 and RTU_0_3 (if Partition 1) or RTU_1_2 and RTU_1_3 (if Partition 2). This is because RTU_n_0 and RTU_n_2 are a lockstep pair, as are RTU_n_1 and RTU_n_3; so configuring RTU_n_0 will handle configuring RTU_n_2, and configuring RTU_n_1 will handle configuring RTU_n_3. See Figure 5.

PARTITION	CORE	CORE FREQ (MHz)	PARTITION STATE	PARTITION CONFIG	CORE STATE	CORE CACHE STATE	CORE ACTIVITY FACTOR (%)
0	SMU	250	ENABLED	N/A	ENABLED	ON	50
	LLCE_M33_0	250			ENABLED	OFF	25
	LLCE_M33_1	250			ENABLED	OFF	25
	CEVA_SPF2	250			ENABLED	N/A	40
1	RTU_0_0	100	ENABLED	LOCKSTEP	ENABLED	ON	1
	RTU_0_1				ENABLED	ON	50
	RTU_0_2						
	RTU_0_3						
2	RTU_1_0	100	ENABLED	LOCKSTEP	ENABLED	ON	1
	RTU_1_1				ENABLED	ON	1
	RTU_1_2						
	RTU_1_3						

Figure 5. Partition 1 is in lockstep, so RTU_0_2 and RTU_0_3 are disabled, and RTU_0_0 and RTU_0_1 are enabled. Partition 2 is in lockstep, so RTU_1_2 and RTU_1_3 are disabled, and RTU_1_0 and RTU_1_1 are enabled.

Note, when the RTU cores are in reset, they consume more dynamic power due to reduced clock gating compared to when running Dhrystone (or WFI, which has the lowest power consumption due to virtually no clocks being enabled). As a result, a negative value for the Partition 1 or 2 power, or a decline in Partition 1 or 2 power as more cores are enabled (rather than remaining in reset) is normal behavior for the RTU partitions.

4.3 Peripheral Activity Sheet

The “Peripheral Activity” sheet includes options for configuring the activity rates for QSPI, SDHC, DDR, FLEXCAN, SPI, and LIN. The peripheral power is computed based on the assumption that these modules are being run at max frequency, the activity factor, and the number of instances enabled per peripheral. User-configurable fields are PERIPHERAL STATE and PERIPHERAL ACTIVITY FACTOR. How to configure each field is described in the list below, and the number and color for each field described corresponds to the feature number and the box color the field is highlighted with in Figure 6.

1. PERIPHERAL STATE (boxed in red) can be set to ENABLED or DISABLED by using the drop-down list for the cells in this column.
2. Cells in the PERIPHERAL ACTIVITY FACTOR column (boxed in light blue) accept an input of 1-100 for how often the peripheral is being used. Note, if the module is set to DISABLED in the PERIPHERAL STATE cell, the activity factor cell will be grayed out instead of blue.
3. The power consumed for a given instance of a peripheral at a specified activity factor is computed in the “VDD Power” column, and the total peripheral power is the sum of all the cells in the “VDD Power” column and is shown in the “Total Peripheral Power” section (boxed in orange).

GROUP	PERIPHERAL	INSTANCE	PERIPHERAL FREQ	PERIPHERAL STATE	PERIPHERAL ACTIVITY FACTOR (%)	VDD POWER (mW)
MEMORIES	QSPI	0	133 MHz	ENABLED	100	4.8999
MEMORIES	QSPI	1	133 MHz	DISABLED		0
MEMORIES	SDHC	0	200 MHz	DISABLED		0
MEMORIES	DDR	0	800 MHz	DISABLED		0
COMMUNICATIONS	FLEXCAN	0	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	1	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	2	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	3	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	4	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	5	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	6	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	7	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	8	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	9	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	10	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	11	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	12	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	13	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	14	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	15	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	16	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	17	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	18	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	19	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	20	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	21	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	22	8 Mbps	DISABLED		0
COMMUNICATIONS	FLEXCAN	23	8 Mbps	DISABLED		0
COMMUNICATIONS	SPI	0	25 MHz	ENABLED	75	1.1576
COMMUNICATIONS	SPI	1	25 MHz	DISABLED		0
COMMUNICATIONS	SPI	2	25 MHz	DISABLED		0
COMMUNICATIONS	SPI	3	25 MHz	DISABLED		0
COMMUNICATIONS	SPI	4	25 MHz	DISABLED		0
COMMUNICATIONS	SPI	5	25 MHz	DISABLED		0
COMMUNICATIONS	SPI	6	25 MHz	DISABLED		0
COMMUNICATIONS	SPI	7	25 MHz	DISABLED		0
COMMUNICATIONS	SPI	8	25 MHz	DISABLED		0
COMMUNICATIONS	SPI	9	25 MHz	DISABLED		0
COMMUNICATIONS	LIN	0	19.98 Mbps	ENABLED	75	0.9014
COMMUNICATIONS	LIN	1	19.98 Mbps	DISABLED		0
COMMUNICATIONS	LIN	2	19.98 Mbps	DISABLED		0
COMMUNICATIONS	LIN	3	19.98 Mbps	DISABLED		0
COMMUNICATIONS	LIN	4	19.98 Mbps	DISABLED		0
COMMUNICATIONS	LIN	5	19.98 Mbps	DISABLED		0
COMMUNICATIONS	LIN	6	19.98 Mbps	DISABLED		0
COMMUNICATIONS	LIN	7	19.98 Mbps	DISABLED		0
COMMUNICATIONS	LIN	8	19.98 Mbps	DISABLED		0
COMMUNICATIONS	LIN	9	19.98 Mbps	DISABLED		0
COMMUNICATIONS	ETH	0	125 MHz	DISABLED		0
					TOTAL PERIPHERAL POWER (mW)	6.9589

Figure 6. Peripheral Activity Sheet with user-configurable fields highlighted

4.4 Test Descriptions for Core and Peripheral

Included below are summaries of how the cores and peripherals were stressed while taking power measurements.

4.4.1 Core Tests

4.4.1.1 SMU

The SMU alternates between running Dhrystone and executing the WFI instruction. The ratio between the 2 represents the activity factor. For example, at 30% activity factor, the SMU runs Dhrystone for 30% of the time and executes the WFI instruction for the remaining 70%. Note, SMU Power = Dhrystone Time Power + WFI Time Power.

4.4.1.2 RTU

The RTU alternates between running Dhrystone and executing the WFI instruction. The ratio between the 2 represents the activity factor. For example, at 30% activity factor, the RTU runs Dhrystone for 30% of the time and executes the WFI instruction for the remaining 70%. Although the SMU is running, it only executes the main test loop briefly, otherwise it is executing the WFI instruction. Note, RTU Power = Dhrystone Time Power + WFI Time Power. Since the RTU power is computed as a delta, the SMU power is not a significant factor in the total RTU power.

4.4.1.3 LLCE_M33

The LLCE_M33 alternates between running Dhrystone and executing the WFI instruction. The ratio between the 2 represents the activity factor. For example, at 30% activity factor, the LLCE_M33 runs Dhrystone for 30% of the time and executes the WFI instruction for the remaining 70%. Note, LLCE_M33 Power = Clock Enabled Power + Dhrystone Time Power + WFI Time Power.

4.4.1.4 CEVA SPF2

The SPF2 alternates between running matmul operations (directions issued by RTU) and executing the WFI instruction. The ratio between the 2 represents the activity factor. For example, at 30% activity factor, the SPF2 runs matmul operations for 30% of the time and executes the WFI instruction for the remaining 70%. Note, CEVA_SPF2 Power = Clock Enabled Power + Matmul Time Power + WFI Time Power.

4.4.2 Peripheral Tests

4.4.2.1 QSPI

The DMA periodically reads from QSPI memory at a predefined rate. The rate at which the DMA reads from the QSPI memory corresponds to the activity rate of the QSPI. For example, at 100% QSPI activity factor, the DMA is performing back-to-back reads at the QSPI's read limit and at 50% QSPI activity, the DMA is performing back-to-back reads at half the QSPI's read limit rate.

4.4.2.2 SDHC

The DMA periodically issues a read request to the SDHC module, which transfers a block of data back to a memory buffer. The rate at which the DMA reads from the SD card corresponds to the activity rate of the SD card. For example, at 100% SDHC activity factor, the DMA is performing back-to-back reads at the SD card's limit while adhering to the minimum spacing requirements for the SDHC v2.0 standard.

4.4.2.3 DDR

The DMA periodically reads from DDR memory at a predefined rate. The rate at which the DMA reads from the DDR memory corresponds to the activity rate of the DDR. For example, at 100% DDR activity factor, the DMA is performing back-to-back reads at the DDR's read limit while adhering to the minimum LPDDR4 spacing requirements for back-to-back reads and at 50% DDR activity, it is being done at half that.

4.4.2.4 FLEXCAN

DMA periodically reads 32-bit data from a predefined memory location and transfers the data to the FlexCAN instance's Message Buffer 0 (MB0) to trigger data transmission at a predefined rate. The 8 bytes of data being transmitted is pre-written into MB0, and the data is written to FlexCAN MB1. At 100% activity factor, FlexCAN is performing back-to-back transmits.

4.4.2.5 SPI

DMA periodically reads 2 bytes of data from a predefined memory location and transfers the data to the SPI instance's transmit buffer at a predefined rate. At 100% SPI activity factor, the SPI is performing back-to-back transmits at the SPI's limit.

4.4.2.6 LINFLEXD

DMA periodically reads 2 bytes of data from a predefined memory location and transfers the data to the LIN instance's LINCR2 register at a predefined rate to trigger a transmission of the data written in the LIN instance's BDRL and BDRH registers during initialization. At 100% activity factor, the LIN is performing back-to-back transmits at the LIN's limit. LINFLEX is operating in LIN mode.

4.4.2.7 ETHERNET

DMA periodically increments the source memory address to read 1-byte numbers from an array in a predefined memory location, then resets the source address to the start of the array and begins incrementing again. The DMA transfers this number to the TBPIR register and triggers the NETC to transmit the 64 bytes data stored by the Buffer Descriptor Entry corresponding to the number the DMA transferred at a predefined rate. At 100% NETC activity factor, the NETC is performing back-to-back transmits at the NETC's limit on each of the 4 data lines. NETC is in RGMII mode.

5 S32Z2/E2 IO Power Estimation

The S32Z2E2_IOpower_Calculator can be used to estimate dynamic I/O current for the I/O signals. This estimate can then be added to the static power specifications provided in the device data sheet to estimate total power on any of the I/O signals.

The tool can be found here:

S32Z2E2_IO_Power_Calculator.xlsx

The 'Overview' sheet provides a summary of the different specified or calculated current parameters and describes the I/O power estimator use case.

The '1.8 V (LVDS)', '1.8V (QSPI0)', and '3.3V (GPIO)' sheets include all available I/Os in their respective voltage domains. The green fields in these sheets are modifiable and require the user to fill in the inputs as per the expected output behavior on these I/Os. Enabling an I/O turns the row blue in the sheet.

One of the modifiable fields is activity. Activity refers to the percentage of time that a signal is "active" or emitting a pulse. For instance, a normal 1 MHz signal with no interruptions has a 100% activity rate. However, if the same 1 MHz (1us period) signal has a break of 1us between each period, then it has a 50% activity rate. The signal is active 50% of the time, during every other period. Dynamic current is determined by the amount of time an I/O signal is active. Therefore, a signal with <100% activity rate has the same dynamic current as a 100% active I/O signal, with frequency and duty cycle reduced by proportionate amounts.

For example, Figure 7 shows a 1MHz signal with 50% activity rate (1us break between 1us period) and 50% duty cycle. However, Figure 8 shows that this signal could also be evaluated in the dynamic current formula as a 500 kHz signal with 100% activity rate (2 us period) and 25% duty cycle and result in the same final dynamic current calculation. Both signals are active for a total of 0.5 us every 2 us.

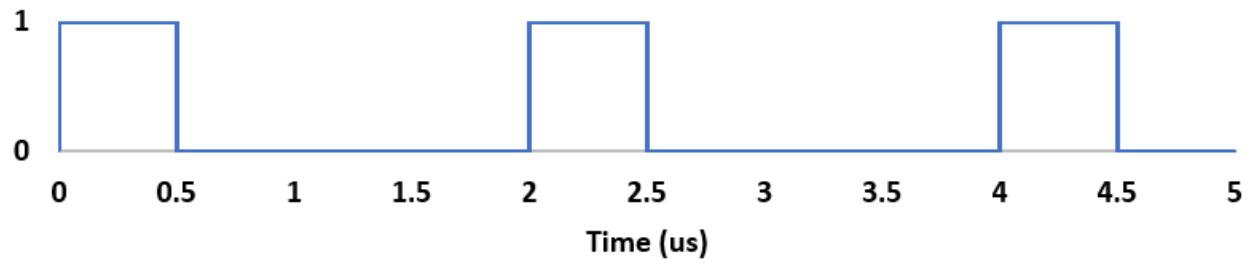

Figure 7. 1 MHz signal with 50% activity rate and 50% duty cycle

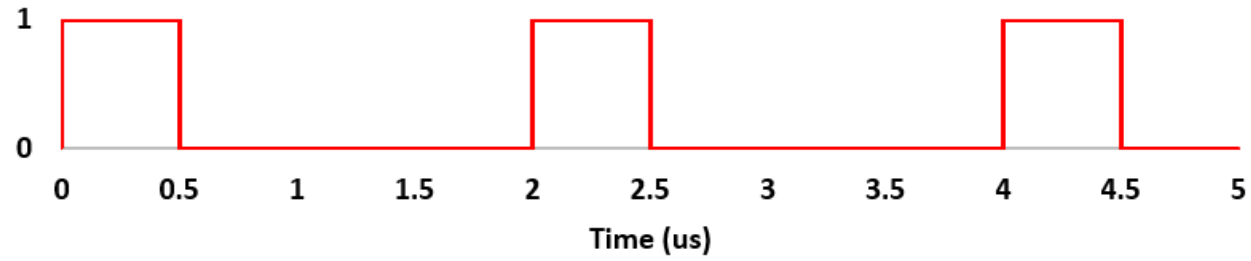

Figure 8. 500 kHz signal with 100% activity rate and 25% duty cycle

One of the other user inputs, frequency, refers to the desired frequency of the output I/O signal.

The SRE value enables slew rate control for the user based on the desired frequency of the I/O signal. For more specific information on frequency ranges of different SRE values, see the MSCR register of the SIUL2_x module that a specific I/O signal falls under. The SRE value also selects the CeffIO entry (nonuser input), which represents the parasitic capacitance of the I/O buffer.

The last modifiable field, Cload_total, is the external capacitive load on the I/O PAD that is specified by the user. Cpin (IBIS) must be included as part of Cload_total.

The total current consumption and total power consumption of all IOs in a VDDx domain is calculated and populated at the bottom right of the sheet. However, enabling more than one I/O pin per PAD highlights the dynamic current field of both rows red and then excludes both results from the total consumption calculations until the error is corrected. See Figure 9.

Port	Function	Module	Description	Direction	Pad Type	I/O Power Segment	I/O Voltage [V]	Enabled	Frequency [MHz]	Activity	SRE	Cload_total [pF]	CeffIO [pF]	Dynamic [mA]
PAD_092	GPIO[92]	SIUL2_4	General Purpose I/O 92	I/O	18FAST	VDD_IO_QSPI_0	1.8						13.6	
PAD_092	GTM_091_O	GTM	GTM Data Port	O			1.8						13.6	
PAD_093	GPIO[93]	SIUL2_4	General Purpose I/O 93	I/O	18FAST	VDD_IO_QSPI_0	1.8						13.6	
PAD_093	QSPI_0_CS_A0	QuadSPI_0	QuadSPI 0 Chip Select A0	O			1.8	y	100	50%	0	15.5	13.6	2.6
PAD_093	GTM_092_O	GTM	GTM Data Port	O			1.8						13.6	
PAD_094	GPIO[94]	SIUL2_4	General Purpose I/O 94	I/O	18FAST	VDD_IO_QSPI_0	1.8						13.6	
PAD_094	QSPI_0_DATA_A_O[	QuadSPI_0	QuadSPI 0 Data OUT	O			1.8	y	100	50%	0	15.5	13.6	ERROR
PAD_094	GTM_093_O	GTM	GTM Data Port	O			1.8	Y					13.6	ERROR
PAD_095	GPIO[95]	SIUL2_4	General Purpose I/O 95	I/O	18FAST	VDD_IO_QSPI_0	1.8						13.6	
PAD_095	QSPI_0_DATA_A_O[	QuadSPI_0	QuadSPI 0 Data OUT	O			1.8	y	100	50%	0	15.5	13.6	2.6
PAD_095	GTM_094_O	GTM	GTM Data Port	O			1.8						13.6	
PAD_096	GPIO[96]	SIUL2_4	General Purpose I/O 96	I/O	18FAST	VDD_IO_QSPI_0	1.8						13.6	
PAD_096	QSPI_0_DATA_A_O[	QuadSPI_0	QuadSPI 0 Data OUT	O			1.8	y	100	50%	0	15.5	13.6	2.6
PAD_096	GTM_095_O	GTM	GTM Data Port	O			1.8						13.6	
PAD_097	GPIO[97]	SIUL2_4	General Purpose I/O 97	I/O	18FAST	VDD_IO_QSPI_0	1.8						13.6	
PAD_097	QSPI_0_DATA_A_O[	QuadSPI_0	QuadSPI 0 Data OUT	O			1.8	y	100	50%	0	15.5	13.6	2.6
PAD_097	GTM_096_O	GTM	GTM Data Port	O			1.8						13.6	

Figure 9. Selecting multiple pins from the same PAD results in an error

Also, some of the I/Os can be configured for both 1.8V and 3.3V operations. These are grouped in ‘dual (QSPI1)’, ‘dual (ETH0)’, and ‘dual (ETH1)’ sheets. Use the dual voltage sheets in a similar way to the fixed voltage sheets. However, the dual voltage sheets require the operational voltage to be input at the bottom left of the sheet in Figure 10. The total power consumption is calculated in the sheet.

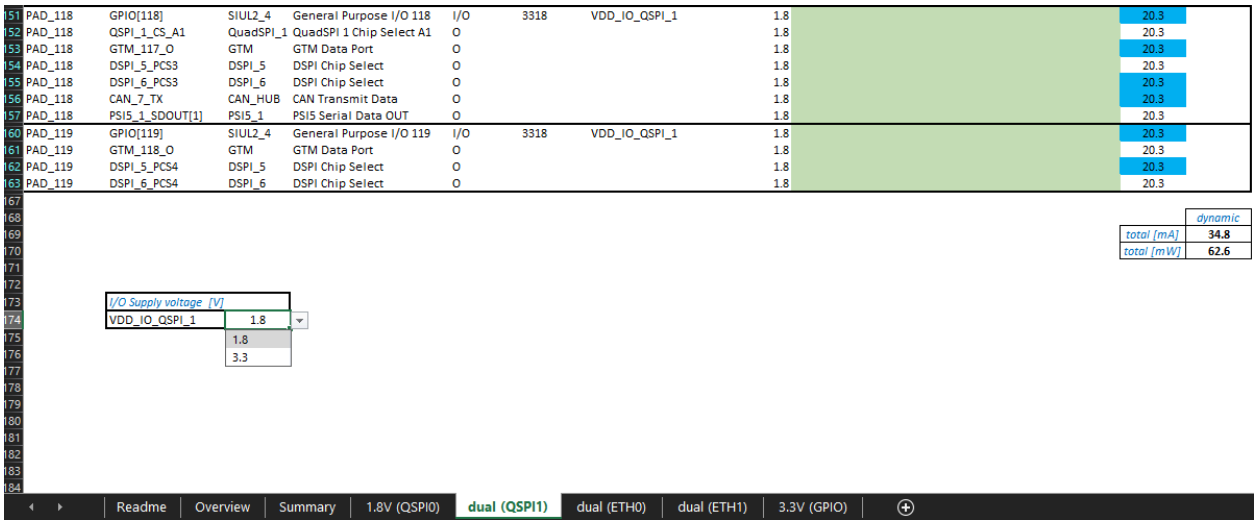

Figure 10. Dual voltage sheets require user input for operational voltage at the bottom left of the sheet

Finally, the ‘Summary’ sheet is a consolidated table of all calculated current and power consumption from each individual I/O group sheet. The total overall dynamic current and power consumption sum across all sheets will be found here at the bottom of the table.

5.1 Use Case - GPIO Toggle

Suppose a simple usage case, where GPIO pin 108 must be toggled at 100 MHz with a 50% activity rate, 50% duty cycle, 3.3V source, and a total capacitive load of 15.5 pF as in Figure 11.

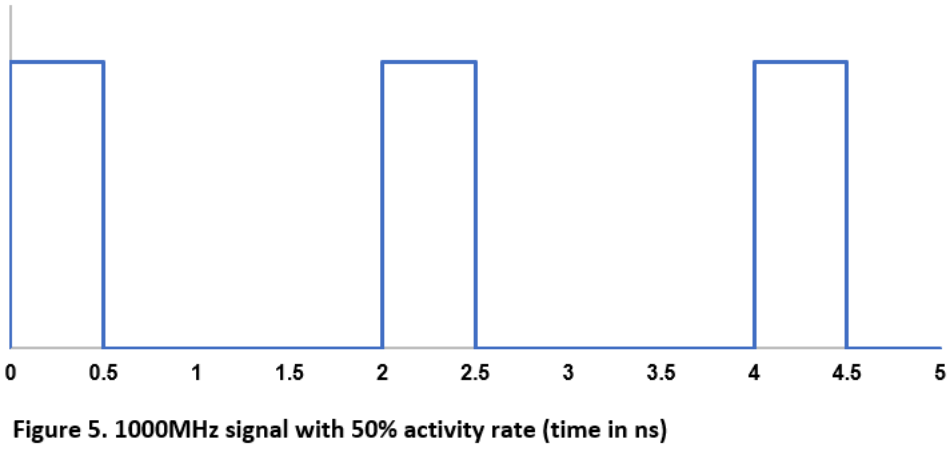

Figure 5. 1000MHz signal with 50% activity rate (time in ns)

Figure 11. 100MHz signal with 50% activity rate and 50% duty cycle

First, navigate to the “dual (QSPI1)” sheet and select 3.3 at the bottom left of the sheet in “VDD_IO_QSPI_1” as in Figure 12.

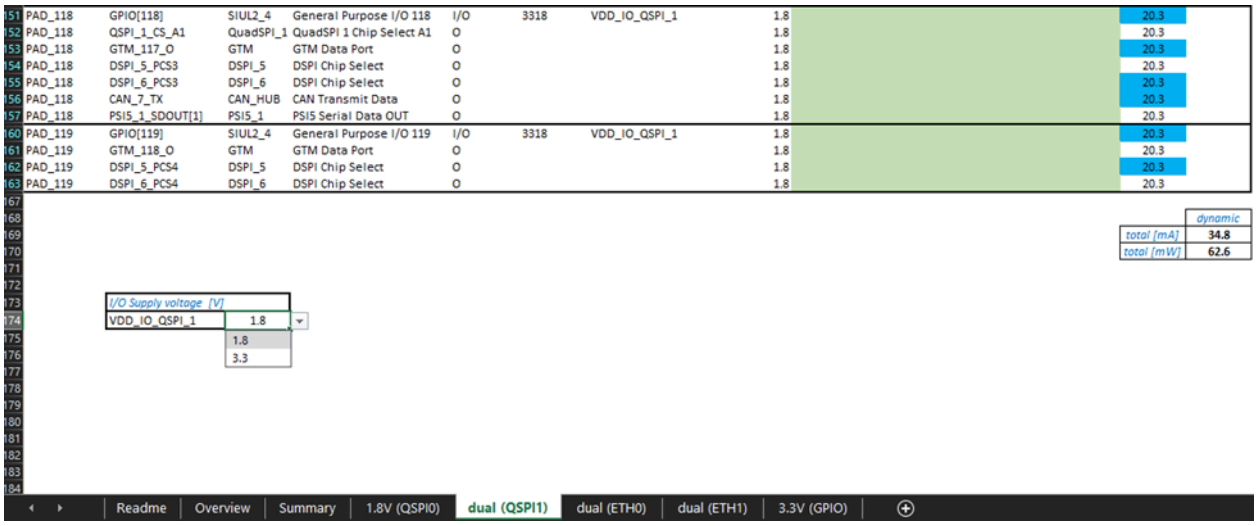

Figure 12. Select the operational voltage for the dual voltage sheet

Then, select “y” in the enabled column of the GPIO [108] row under PAD 108 and enter 100 in the frequency and 50 in the activity column as in Figure 13.

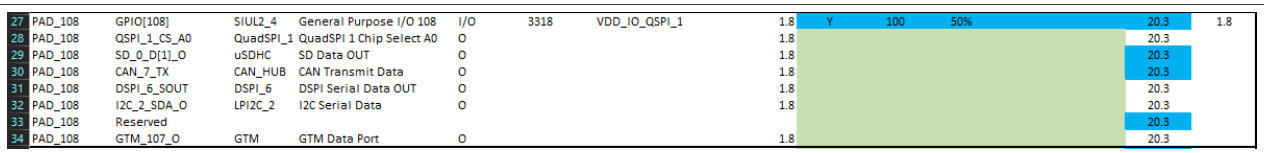

Figure 13. Enable the GPIO signal in PAD 108

Select the SRE according to the MSCR register of the SIUL2_x module this PAD falls under. See Figure 14. In this case, refer to the MSCR register of SIUL2_4 in the reference manual. For this example, the default option (0) is selected. The CeffIO column populates itself once the SRE is selected.

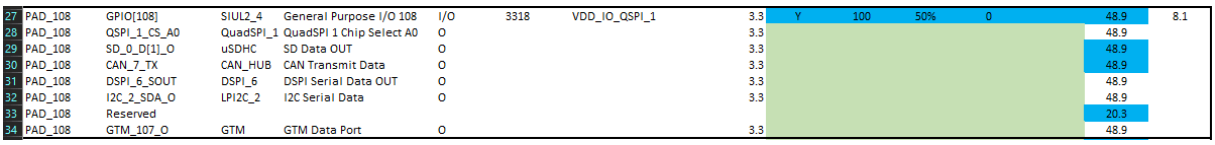

Figure 14. Select the appropriate SRE option

Finally, input 15.5 in the Cload_total column, and the calculated dynamic current will be found in its respective column at the end of the row as in Figure 15.

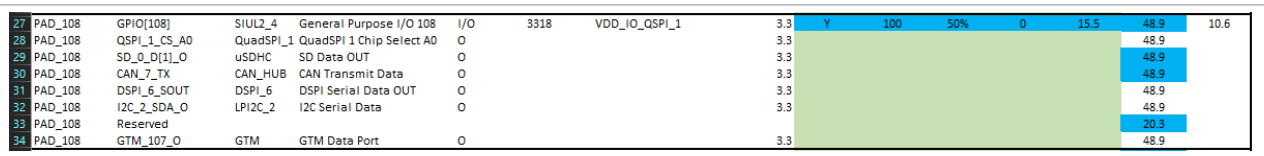

Figure 15. Input Cload_total value in the correct column

6 Additional Considerations

6.1 Power Impact from Clock Gating Peripheral Modules

For clock gating, supported peripherals are clock gated using the GPRx_PCTL register. For supported peripherals, all instances are turned on/off and the power delta is recorded. Table 1 and Figure 16 show the power consumed when all instances of a peripheral have their clock enabled using the GPRx_PCTL register compared to clock disabled.

Note: *The power measurements recorded here does not include the dynamic current of the peripheral running and, in all cases, the peripheral is disabled as applicable.*

Table 1. Peripheral Clock Gating Results

Module	Instances	Clock Gate Power (mW)
ADC	2	0.89
CE_CAN	24	4.67
CE_EDMA	1	1.71
CE_PIT	6	0.35
CTU	1	0.28
DDR	1	31.01
DMA_CRC	4	0.41
DMA_MUX	4	0.36
EDMA	5	5.55
ETH	1	42.32
FLEXRAY	2	1.51
GTM	1	11.9
I3C	3	0.36
LIN	12	2.01
MSC	2	0.52
NANO	1	1.49
PIT	4	0.3
PSI5	2	0.62
PSI5S	2	0.3
QSPI	2	0.31
RXLUT	1	0.13
SDHC	1	1.71
SINC	1	0.18
SIPI	2	1.23
SIUL2	4	0.41
SPI	10	1.5
SRX	2	1.28

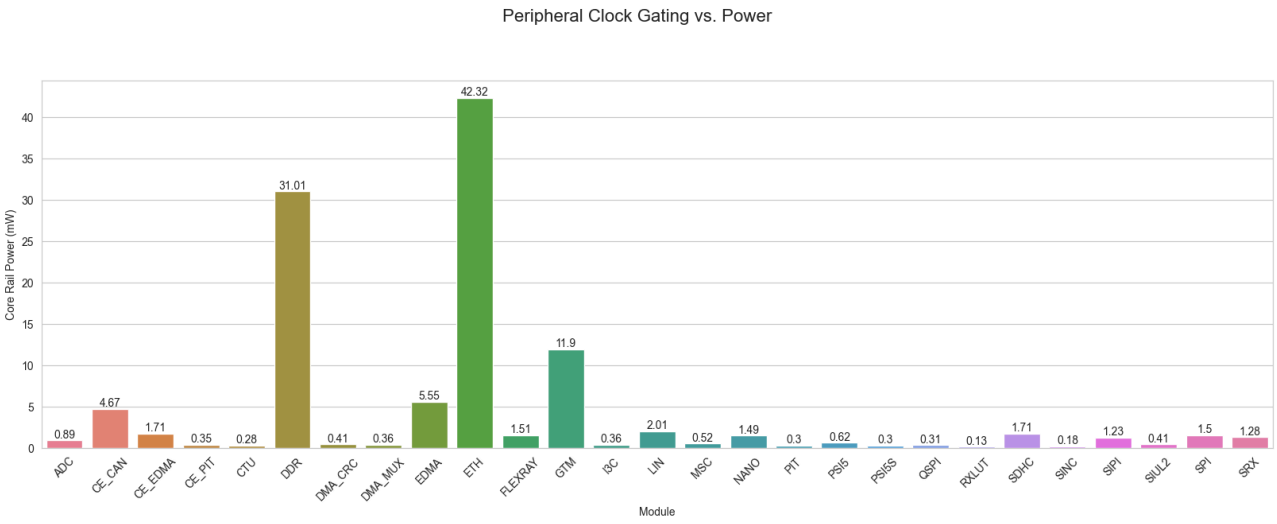

Figure 16. Clock Gating Peripherals Result

7 References

[1] S32Z2 Reference Manual
[2] S32E2 Reference Manual
[3] S32Z2 Data Sheet
[4] S32E2 Data Sheet

8 Revision history

Table 2. Revision history

Document ID	Release date	Description
AN15074 v.1.0	19 June 2026	Initial release

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