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Application Note

**Understanding the Multivibrator  
Based Crystal Oscillator Circuit  
Used on the BiCMOS MPC Family  
of Clock Drivers**

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Understanding the Multivibrator Based Crystal Oscillator Circuit Used on the BiCMOS MPC Family of Clock Drivers

When using a PLL as a clock generation device it is desirable to use a crystal controlled source as the reference clock. Crystal controlled sources provide accurate frequencies at a reasonable cost. To minimize implementation costs many PLL clock generators integrate the crystal oscillator circuitry on the chip, thus requiring only the crystal itself as an external component. There are many different forms of crystal oscillator designs used for PLL clock drivers with the standard inverter gate based Pierce oscillator being used most often. For many of Motorola's MPC clock drivers (see the individual data sheets to identify the oscillator type for a given device) an alternative multivibrator based oscillator design is used. There are some differences between the more widely known Pierce oscillator and the multivibrator type; this application note will outline some of the more important differences for the user. In addition, for applications where the absolute accuracy of the oscillator is of paramount importance there are some guidelines which must be considered. This application note will present those guidelines for those applications which require highly accurate clock frequencies.

Series vs Parallel Resonant Circuits

The most fundamental difference between a Pierce and a multivibrator oscillator is the crystal resonant mode that is used. The Pierce oscillator uses a crystal in its parallel resonant mode while the multivibrator uses the crystal in its series resonant mode. There is no structural difference between a series resonant mode crystal and a parallel resonant mode crystal, the only difference is in the way the device is tested and specified. Figure 1 illustrates the reactance vs frequency curve of a typical crystal along with an electrical model of its behavior. The Cload shown in the model is external to the crystal, CO is the capacitance associated with the crystal holder and will vary from one package style to the next. C1 and L1 model the frequency of oscillation, the appropriate equation is shown in Figure 1. The series resonant point of a crystal is defined as the frequency at which the crystal looks purely resistive. For a series resonant mode oscillator this is the frequency at which the circuit will oscillate. The Cload shown in Figure 1 is specific to a parallel resonant oscillator circuit. Parallel resonant crystals are specified for a specific capacitive load, variations in the load capacitance will lead to slight variations in frequency from the specified value. Because the Pierce oscillator is far more prevalent it may be difficult to find series mode crystals on short notice. If this is the case the user may want to go ahead and use a parallel resonant crystal. A parallel resonant specified crystal will oscillate at a frequency a few hundred ppm less than specified when used in a series resonant circuit. For many computer applications an error of a few hundred ppm is immaterial, for these applications a parallel resonant or series resonant crystal can be used interchangeably without significantly altering system performance.

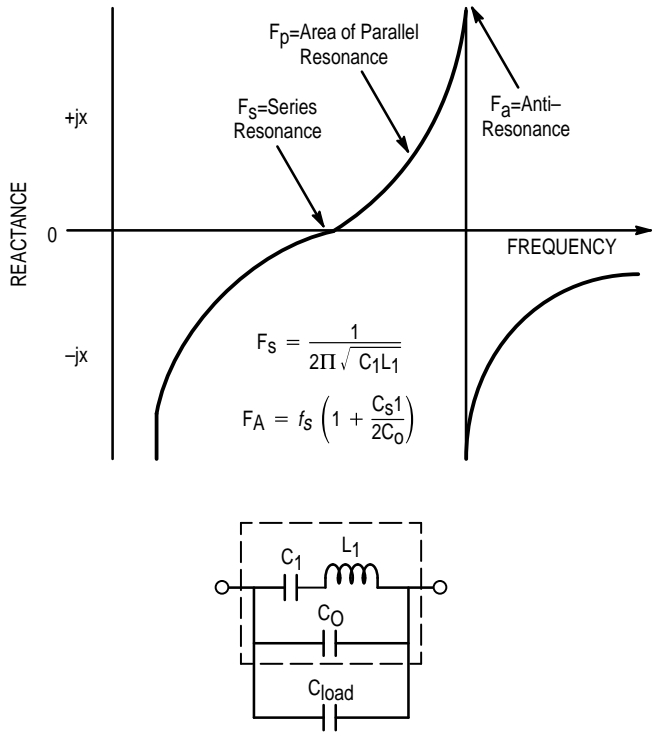


Figure 1. Reactance Curve of a Quartz Crystal

Another important difference between a Pierce and a multivibrator based oscillator circuit is in its behavior when the crystal input is overdriven with a logic signal. A Pierce oscillator circuit is comprised essentially of a large inverter gate. The xtal\_in (crystal) input of this circuit looks just like an input to a standard digital gate. Therefore the xtal\_in input of a Pierce oscillator can be overdriven with any standard logic device with the result of a simple logic inversion. The multivibrator design used in much of the MPC clock driver product line cannot be overdriven easily. In fact trying to overdrive these inputs is highly discouraged. There are some situations where driving a PLL reference clock input with a logic element is very desirable, to get around the constraints presented by the multivibrator oscillator used on the MPC products an alternative logic level compatible input for use as a reference clock is usually provided.

Finally there is one subtle difference between the two designs, a difference which likely is only important to an experienced crystal oscillator designer. In typical applications this difference is transparent to the user. In the Pierce oscillator circuit the crystal element is in the feedback path of the oscillator circuit. On the other hand for the multivibrator designs used on the Motorola clock drivers the crystal is not in the feedback loop. Figure 2 shows a simplified schematic of the two oscillator designs. For the Pierce designs the inverter and the two capacitors provide the 360° phase shift while the multivibrator designs relies on back to back

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inverters to provide this same phase shift. In both cases the crystal's responsibility is to provide the circuit with gain at the appropriate frequency and provide some degree of phase shift to account for the delays in the inverter stages. In the Pierce design the crystal reactance will work directly on the phase of the loop, however the phase effects on the loop from the crystal for the multivibrator circuit are not direct as the crystal is not in the actual feedback path. This phase shifting action of the crystal will cause problems in some applications as will be discussed in the following section.

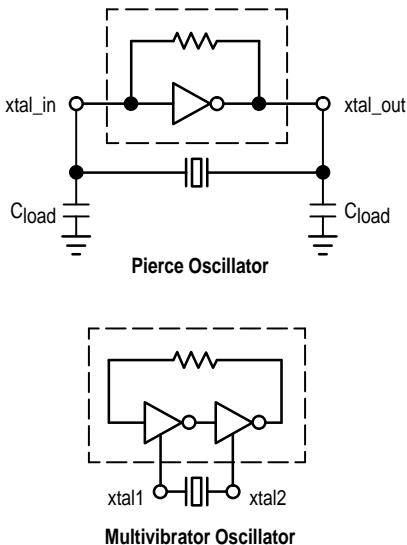


Figure 2.

## Guidelines for Precision Frequency Applications

In the preceding paragraphs it was noted that in most computer clocking applications, clock frequencies within a few hundred ppm of the desired frequency are acceptable as system performance is not significantly affected. However there are some applications where the clock driver plays in a real time environment; an environment where a few hundred ppm error can quickly accumulate and cause significant system problems. For these applications, special guidelines must be followed. To explain the inherent frequency error issue in Motorola's multivibrator based oscillator, we need to review the basics of the crystal oscillator design.

There are two criteria in any oscillator design which must be met for a circuit to oscillate: first the gain around the loop must be greater than 1 and second there must be a  $360^\circ$  phase shift around the loop at the frequency where the gain is greater than 1. The multivibrator oscillator design used in the Motorola clock driver family consists of two cascaded inverters with the output fed back to the input (Figure 2). The crystal sits outside this feedback loop and its main purpose is to interact with the oscillator design to induce significantly higher gain in the loop at its series resonant point. On the surface it would appear that the oscillator circuit provides exactly a  $360^\circ$  phase shift. However when one takes into account the fact that there are finite propagation delays

associated with these inverters, in reality the total phase shift around the loop is slightly more than  $360^\circ$ .

Although the crystal does not lie in the feedback path, its impedance does affect the overall phase of the loop. In addition the parasitic capacitances and resistances of the actual PCB layout will also affect the total phase of the oscillator loop. Because the crystal and the parasitics are not in the feedback path this influence is not in a 1:1 relationship and the phase difference measured between the xtal1 and xtal2 pins does not represent the phase around the oscillator. Because the crystal oscillator circuit requires  $360^\circ$  phase shift, the crystal needs to look capacitive to compensate for the extra phase introduced by the inverter delays and pull the total phase change in the loop back to  $360^\circ$ . From the crystal reactance curve in Figure 1 it is plain to see that as the crystal becomes more capacitive its frequency of oscillation will reduce. The amount of reduction is a function of the crystal reactance curve as well as additional board layout parasitics between the oscillator inputs and the actual crystal, but in general the error is in the 200 to 300 ppm range.

The easiest method to compensate for this shift is to add a reactive element into the oscillator network to provide the appropriate phase shift so that the crystal can return to its series resonant point. The schematic in Figure 3 illustrates the best way to do this. A capacitor is added in series with the crystal to provide the reactance required to compensate for the gate delays in the oscillator. The schematic in Figure 3 shows a variable capacitor, this may not be realistic as it may be prohibitively costly. The tunable capacitor is shown because the value will vary with the PCB and crystal parasitics of an application as well as with the specified crystal frequency. The dependence on the crystal frequency is explained by the fixed nature of the inverter delays of the crystal oscillator circuit. Because these delays are fixed with respect to frequency, as the frequency increases the delay induced phase error (the inverter delays are a larger percentage of the period of oscillation) around the loop will increase. As a result a smaller capacitor is needed to compensate for the larger phase adjustment that is required at higher frequencies.

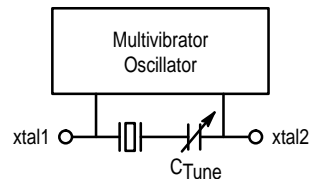


Figure 3.

With all of these factors it is extremely difficult to recommend specific capacitor values for every application. Figure 4 presents a curve of series capacitor values vs crystal frequency for a typical application. The user is encouraged to use these values as a starting point and then empirically identify the appropriate value for their application based on actual measurements. Through simulation, it has been determined that with the use of high performance, low ppm error crystals and an empirical measurement based setting of the series capacitor, the oscillator will provide

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$\pm 100$ ppm type error performance. If the performance required is better than  $\pm 100$ ppm then individual board tuning of the series capacitor will be required.

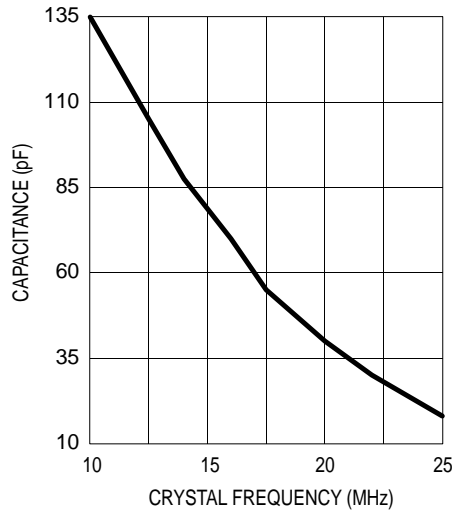


Figure 4.

### Summary

The use of crystal oscillators as the primary system clock reference is a common occurrence in today's clock driver devices. In most cases the type of oscillator design chosen will have little or no effect on the end user, but in some cases a better understanding of the integrated oscillator may prove to be beneficial. This application note provides a comparison of the basic differences between the often used Pierce oscillator and the multivibrator based oscillator used in many of Motorola's BiCMOS MPC clock drivers. In addition guidelines for optimizing the real time accuracy of the oscillator were presented to assist in those applications where real time accuracy is important. The principles presented were done so at a level of sophistication that was deemed appropriate for dealing with the fundamental issues faced by digital designers building PLL based clock trees. For more theoretical, mathematical based descriptions of crystal oscillators the user is encourage to review one of the many analog design books available in support of the industry.

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