AN1602

3.6 V and 4.8 V GSM/DCS1800 Dual-Band PA Application with DECT Capability Using Standard Motorola RFIC's

Prepared by: Gilles Montoriol, Christophe Fourtet, Dominique Brunel, Jean Baptiste Verdier and Jacques Trichet
Wireless Subscriber Group, RF Semiconductor Division. Motorola Semiconductor S. A.

INTRODUCTION

Wireless Cellular communications using GSM format in Europe is deployed in both the 900 and 1800 MHz bandwidths. The regulation is going to allow system interoperability. Then, an interest is coming in portable phones which are able to manage both bands.

This application note describes the realization and performances of a dual band power amplifier for GSM at 900 and 1800 MHz. With some modification, this board can also be used for GSM/DCS1800/DECT applications.

This application re–uses standards RFIC's already introduced on the market for single band application, which is an advantage regarding cycle time, cost and manufacturability of the PA compared to a specific dual band PA design.

BOARD FUNCTIONALITIES

The key parts used in this demonstration board are the MRFIC0917 (GSM IC power amplifier) and the MRFIC1817 (DCS1800 IC power amplifier). Both parts operate at 3.6 V.

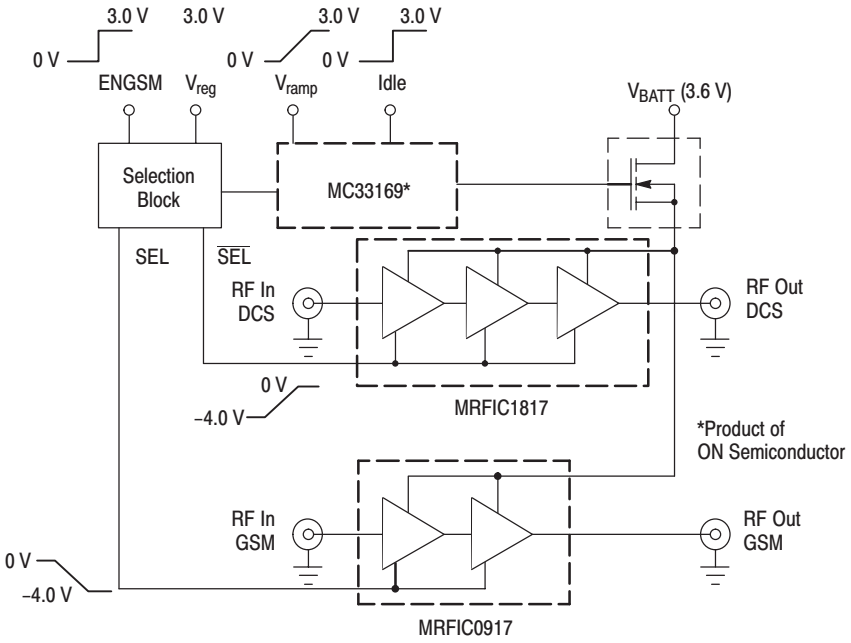
In the 4.8 V application, the MRFIC0913 is used for GSM and the MRFIC1818 is used for DCS1800. The negative voltage required by GaAs technology is provided by the MC33169 (product of On Semiconductor) support IC. In conjunction with a MMSF4N01HD (product of ON Semiconductor) N–channel MOSFET, this circuit is able to control the output power of both power amplifiers. This control, which is linear, increases performance and stability of the control loop.

The support IC integrates a negative supply, voltage tripler, and priority management for IPA drain switching.

Using the selection block, three small signal transistors, generates the ON–state for the selected path and the drive levels for an optional RF power switch.

Together, these components form a complete system solution for a dual band power amplifier function. A block diagram of the application circuit is shown in Figure 1.

Figure 1. Dual Band Amplifier Block Diagram



REV 1

MC33169 FUNCTIONALITY

The MC33169 integrated circuit provides negative voltage generation and regulation, direct drive of the N–channel drain switch transistor, a complete priority management system, and other possible facilities which are very useful for battery–operated designs ranging from 2.7 to 7.5 V. There are two possible modes of operation.

Mode 1: Negative Supply Continuous Operation

In Mode 1 of operation, the IDLE pin is connected to 2.7 or 3.0 V (logic “1”) during the entire transmitting period (even between bursts). Transmit burst shaping and output power control is implemented by applying the correct ramping voltage to the V_{ramp}.

Higher DC voltages are available from the V_{BB} double and V_{BB} triple pins on the MC33169. For low battery voltage designs, the doubled or tripled voltages are useful for operating a RF power switch. More than 3.0 mA of current is available from these pins.

Mode 2: Negative Supply Burst Operation

In Mode 2 of operation, the V_{ramp} is still a linear function of the desired output power; however, the Idle pin controls the MC33169 negative generator start–up. Some energy can be saved with this arrangement because the negative supply operates only during the transmit burst.

The currents available from V_{BB} double or V_{BB} triple are then slightly lower but are still large enough to supply the MRFIC0903 during the burst, or to drive the VCO’s varactor with a low current system. In this board an ENSWT signal is provided, allowing the drive of power switch between 3.0 V and –4.0 V, which is large enough to drive the MRFIC0903.

The timing control sequence in Mode 2 of operation is shown in Figure 2.

Figure 2. Dual Band Application Timing Sequence

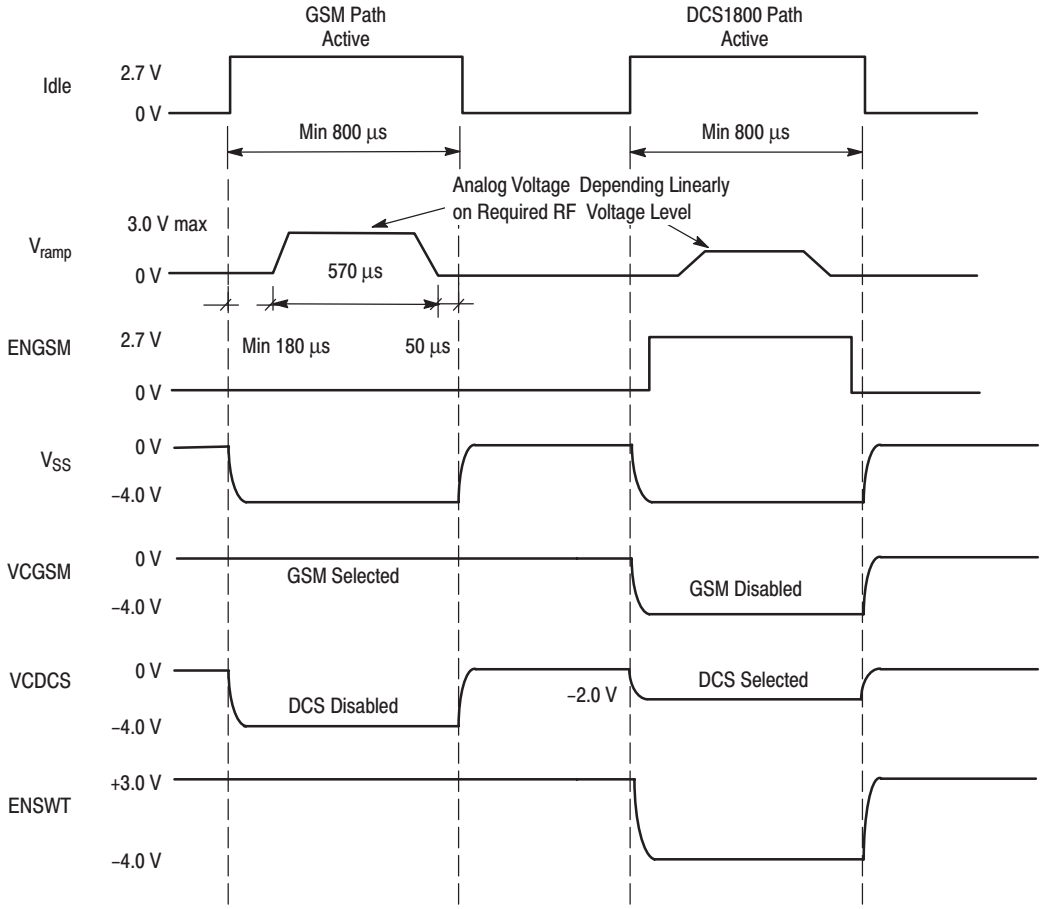
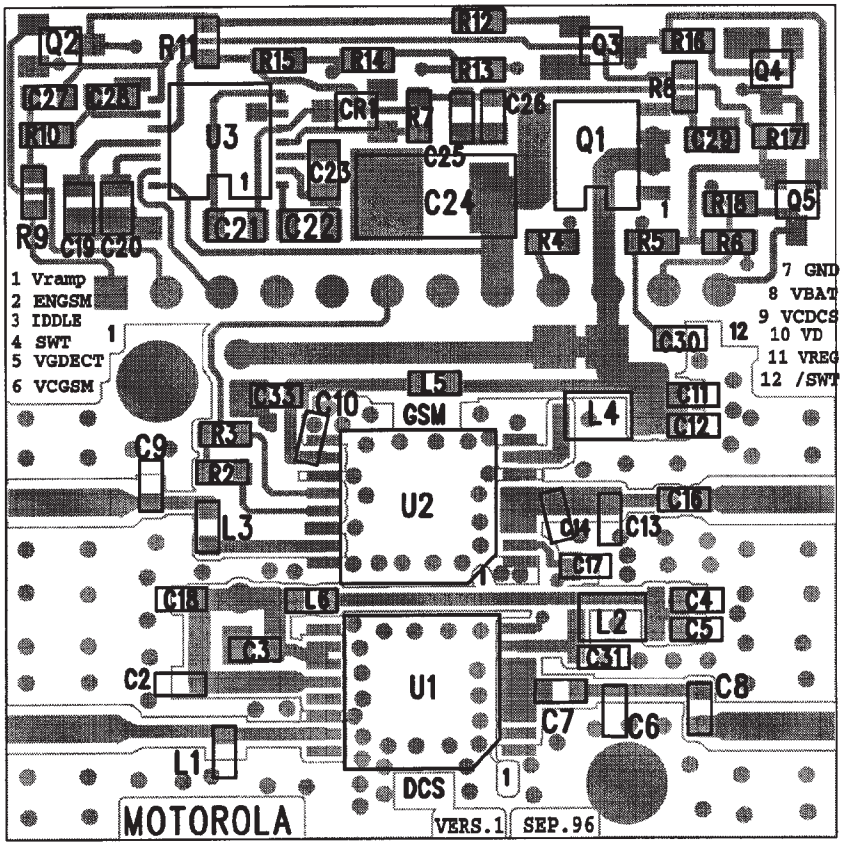
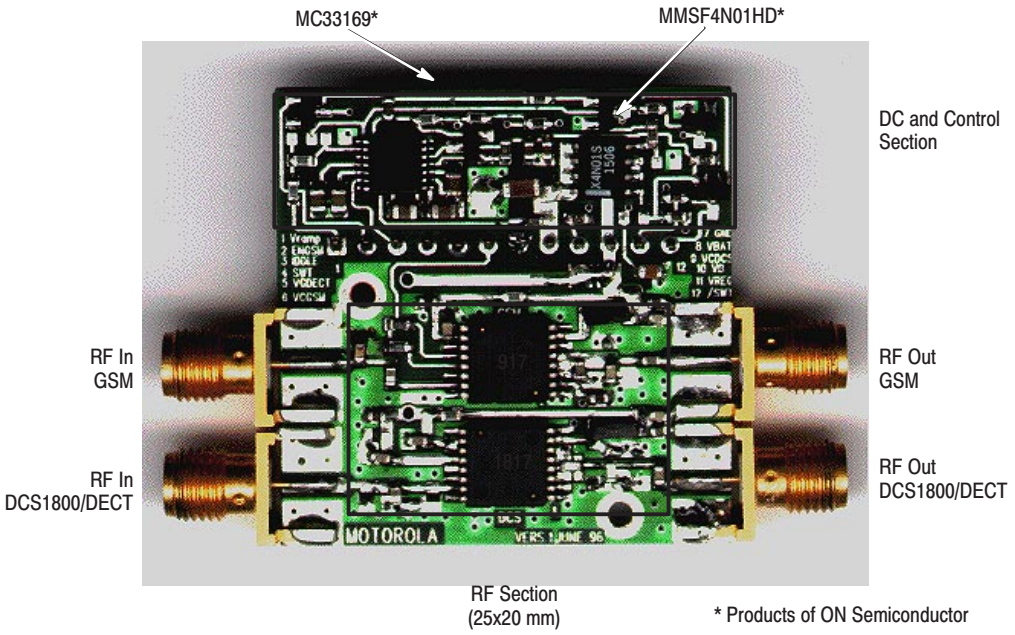


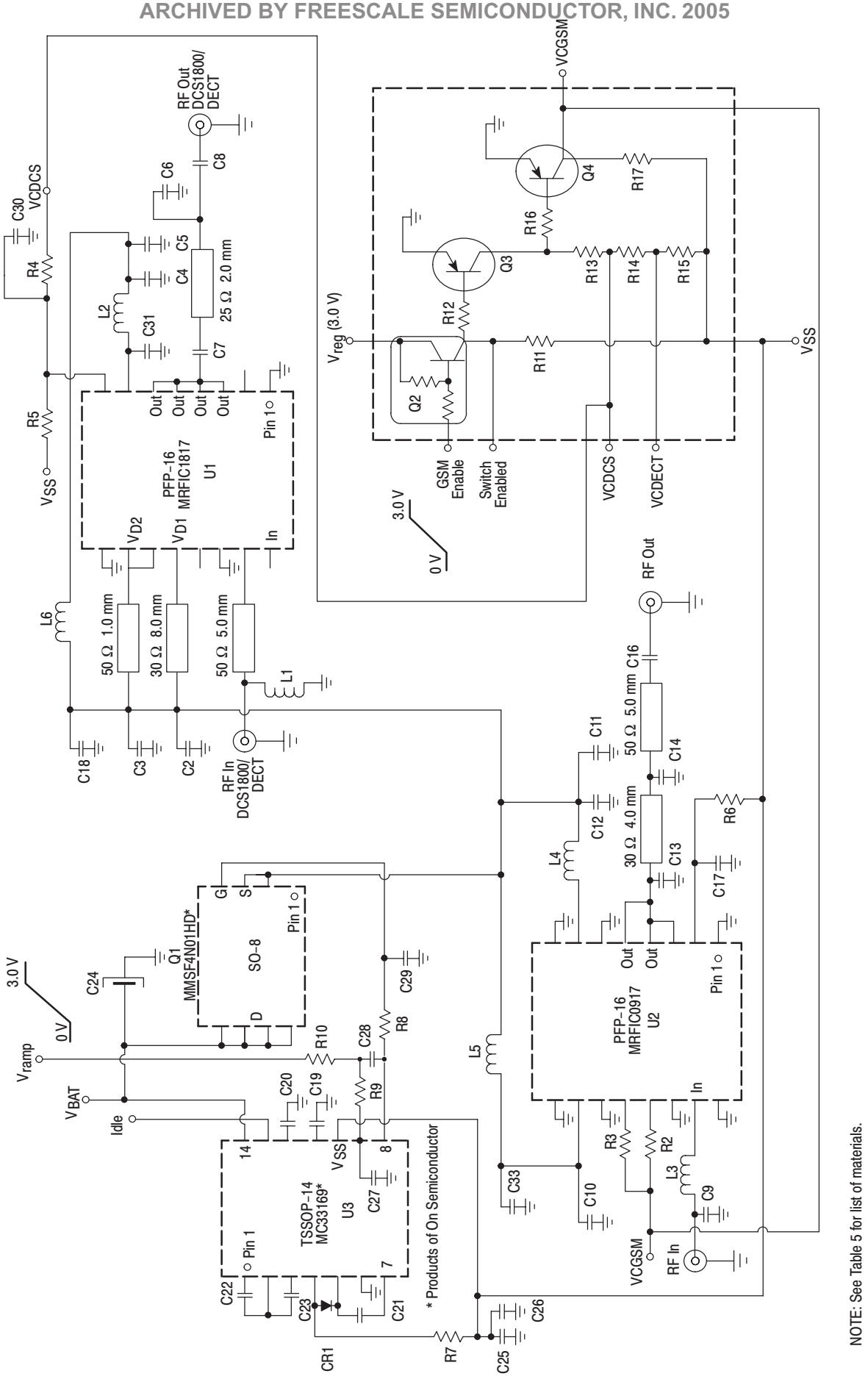
Figure 3. Component Placement for 3.6 V Application



Board Material: FR4 H = 0.48 mm Class 5 PCB (Scale: 3/1)

Figure 3a. Application Board for Dual Band PA at 3.6 V using MRFIC0917 and MRFIC1817





NOTE: See Table 5 for list of materials.

Figure 4. Application Circuit for Dual–Band GSM/DCS1800 PA at 3.6 V using MRFIC0917 and MRFIC1817

BOARD DESCRIPTION

DC and Control Section

The demonstration board layout and component placement for 3.6 V application is shown in Figure 3 and the placement for the 4.8 V board is shown in Figure 17.

- Input pins available on the DC connector are V_{BATT} (battery voltage), V_{REG} (regulated 3.0 V supply), IDLE (enable the negative voltage generator), ENGSM (selects the RF path), V_{RAMP} (RF power control) and V_{REG} (regulated 3.0 V supply).
- The output pins on the DC connector are ENSWT (optional control voltage for a RF power switch), VGDECT/VCDCS (gate bias voltage for DCS1800 PA), VCGSM (gate bias voltage for GSM PA), V_D (drain voltage for both PA's).
- Figure 4 shows an application schematic for a 3.6 V part while Figure 18 shows an application schematic for the 4.8 V part.
- The negative voltage generator and control are organized around Q1, Q2, Q3, Q4 and U3.
- C22, C23 (1.0 µF) are used for internal charge pump oscillator at 100 kHz. This value is not critical and could be decreased to 220 nF.
- C19, C20 are used for voltage doubler and tripler, which will allow to drive the NMOS transistor (Q1).
- CR1 diode, C21, C25, C26 allow negative voltage detection and filtering.
- R8 (470 Ω) gives additional filtering of 100 kHz spurious which could modulate Q1 gate and then be converted beside the carrier. The negative voltage is regulated with an internal zener diode.

As MC33169 is able to operate at 2.7 V, when the battery voltage is much higher than this value, there is a clamping current in this diode, which may generate some spurious signals on the negative supply.

To avoid this issue, a RC filter cell has been inserted on the power supply line of the MC33169 (R19, C32). When 3.6 V battery is at low voltage (3.0 V), there is a 0.2 V drop on the U3 supply line. This point is much more critical in the 4.8 V application where R19 resistor provides a 1.0 V drop in this case, which allows the MC33169 to work down to 4.0 V V_{BATT}.

- ENGSM pin which is compatible with CMOS logic, is biased by V_{REG} (regulated 3.0 V) and V_{SS} (regulated –4.0 V). Q2 operates as a simple inverter and provides the ENSWT signal and drives Q3 and Q4. Note that Q2 is a self–biased transistor (MMUN2112LT1).

When ENGSM = 0 V then VCDCS = –4.0 V, VCGSM = 0 V, MRFIC0917 is in ON–state, and MRFIC1817 is in OFF–state (MRFIC0913 and MRFIC1818 respectively for the 4.8 V application). MRFIC0917 (MRFIC0913) has an internal resistor bridge connected between VCGSM and V_{SS}, in order to be at this nominal quiescent current, about 800 mA to 1200 mA, (500 mA to 900 mA for the 4.8 V application) when VCGSM = 0 V. This biasing point can also be fine tuned by adjusting R2 and R3 resistors which impact first and second stage amplifier current respectively.

When ENGSM = 3.0 V then VCDCS = –2.0 V, VCGSM = –4.0 V, MRFIC0917 is in OFF–state, and MRFIC1817 is in ON–state. A difference between MRFIC0917 and MRFIC1817 is that the DCS amplifier does not have an internal resistor bridge, but does have a single biasing resistor which supplies the three stages. For this reason, –2.0 V is required on VCDCS to bias the amplifier at its nominal quiescent current.

To put the power amplifier in the OFF–state, –4.0 V are supplied to the gates. The pinch–off voltage of the GaAs transistors used is –2.5 V, so the current consumption is then lower than 0.5 mA. The user needs to keep the drive level low enough at the disabled PA input, otherwise it may operate as a class C amplifier and conduction may occur. This maximum drive level is about 5.0 dBm for MRFIC0917/MRFIC0913 and 3.0 dBm for MRFIC1817/MRFIC1818 as well. This is an important point which needs to be highlighted.

When the GSM mode is selected, RF drive on the DCS path needs to not exceed 3.0 dBm; and when the DCS mode is selected, RF drive on the GSM path needs to not exceed 5.0 dBm.

During all the sequence, drain pins of both power amplifiers are supplied together (Otherwise it would have been necessary to use two different N–MOS transistors).

RF SECTION

GSM Path

The input match is a shunt C (C9) series L (L3), low–pass cell which has been tuned at rated power. Interstage matching has been optimized by implementing (as shown in Figure 3) C10 and C12 decoupling capacitors on two microstrip lines. 33 pF in 0603 size has been found optimum for GSM.

The output matching is realized with a one–cell, low–pass filter using a 30 Ω microstrip line and C13 + C14 capacitors. L4 inductor allows for optimized efficiency while impacting harmonic impedances in the output transistor plane. However, the inductor needs to be a high–Q part with a high–DC maximum current (a Coilcraft Microspring Series has been implemented). This parallel inductor can also be realized with a 20 mm microstrip line. In this application the best surface solution has been selected. In the 4.8 V application, when efficiency is not critical those two parts can be avoided. The loss of efficiency will be then 3 to 4%. (For typical performances see Table 3/Table 4 in the Appendix). Typical gain and return loss at rated power are given in Figure 5 for GSM path (Figure 18 for the 4.8 V application).

Figure 5. Gain (1), Isolation (2) and Return Loss for GSM Path at 3.6 V

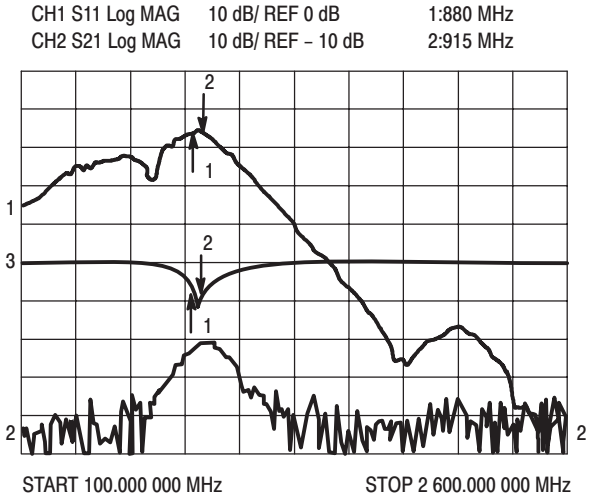


Table 1. Minimum and Typical Performances for GSM Path at 3.6 V

ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2} = 3.6 V, P_{in} = 10 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Frequency Range	880	–	915	MHz
Output Power	34	34.5	–	dBm
Power Added Efficiency	43	–	–	%
Input VSWR	–	2:1	–	VSWR
Harmonic Output 2nd f_o 3rd f_o	 – –	 – –	 –30 –35	dBc
Negative Supply Current	–	–	1.0	mA
Output Power at Low Voltage (V_{D1}, V_{D2} = 3.0 V)	32.5	33	–	dBm
Output Power, Isolation (V_{D1}, V_{D2} = 0 V)	–	–20	–15	dBm
3.0 dB V_{DD} Bandwidth (V_{D1}, V_{D2} = 0 to 6.0 V)	1.0	–	–	MHz
Noise Power in 100 kHz, 925 to 935 MHz	–	–	–90	dBm
Load Mismatch Stress (P_{in} = 10 to 13 dBm, P_{out} = 5.0 to 35 dBm, Load VSWR = 10:1 at any Phase Angle, V_{D1}, V_{D2} Adjusted for Specified P_{out})	No Degradation in Output Power after Returning to Standard Conditions			
Stability – Spurious Output (P_{in} = 10 to 13 dBm, P_{out} = 5.0 to 35 dBm, Load VSWR = 6:1 at any Phase Angle, Source VSWR = 3:1, at any Phase Angle, V_{D1}, V_{D2} Adjusted for Specified P_{out})	–	–	–60	dBc

DCS Path

The input match circuit is made with a single parallel inductor (L1) and a series inductor realized with a microstrip line. Drain matching is made with parallel stubs which are added to an internal prematching. A decoupling circuit is made with 0603 22 pF capacitors.

The output matching circuit is similar to the GSM one. L2 inductor and C31 capacitor allow for optimized efficiency, while impacting harmonic impedances in the output transistor plane. Like in the GSM PA, this inductor has to exhibit a high–Q and a high maximum current. Typical gain and return loss at rated power are given in Figure 6 for GSM path (Figure 19 for the 4.8 V application).

Figure 6. Gain (1), Isolation (2) and Return Loss for DCS1800 Path at 3.6 V

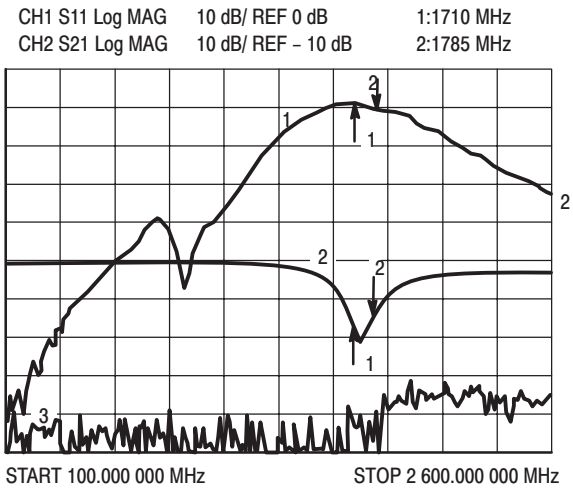


Table 2. Minimum and Typical Performances for DCS Path at 3.6 V

ELECTRICAL CHARACTERISTICS ($V_{D1, 2, 3}$ = 3.6 V, P_{in} = 5.0 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Frequency Range	1710	–	1785	MHz
V_{DD}	–	3.6	–	V
V_{SS}	–	–4.0	–	V
I_{SS}	–	–	1.0	mA
Output Power at (GSM Pulse)	32	33.5	–	dBm
Output Power at (GSM Pulse; Low Voltage: V_{DD} = 3.0 V)	30.5	–	–	dBm
Power Added Efficiency	35	42	–	%
Input Return Loss	–	–	–10	dB
Harmonic Output 2nd f_o 3rd f_o	 – –	 –45 –35	 –30 –30	dBc
Output Noise Power (P_{out} Nominal; 100 kHz Bandwidth; 20 MHz above f_o)	–	–85	–80	dBm

Control and Its Advantages

Figures 7 and 8 present rise and fall time within 30 dB dynamic range for the GSM path. Figures 9 and 10 show performance for the DCS path.

The transition is about 2.0 µs in the worst case.

Figures 11 and 12 check that spurious levels are lower than –60 dBc even for the minimum output power (5.0 dBm) when GMSK modulation is applied to the PA.

Figure 13 shows the output power when a linear control ramp is applied on V_{ramp} input. This depicts the superiority of the drain control for a PA versus gate control. The RF output voltage/V_{ramp} transfer function is linear for V_{ramp} input voltage up to approximately 1.5 V. Therefore, very simple, low–cost techniques can be used to generate the V_{ramp} voltage necessary to get the shaping and RF steps levels. This eliminates all stability loop problems due to gate control non–linearity.

This transfer function shape leads to a very stable and linear control loop and requests a lower loop bandwith. As the PA is in saturation within the full dynamic power range, AM to AM conversion remains very good, even at low power level.

Figure 7. Rise Time for GSM Path at 3.6 V within 30 dB Dynamic Range

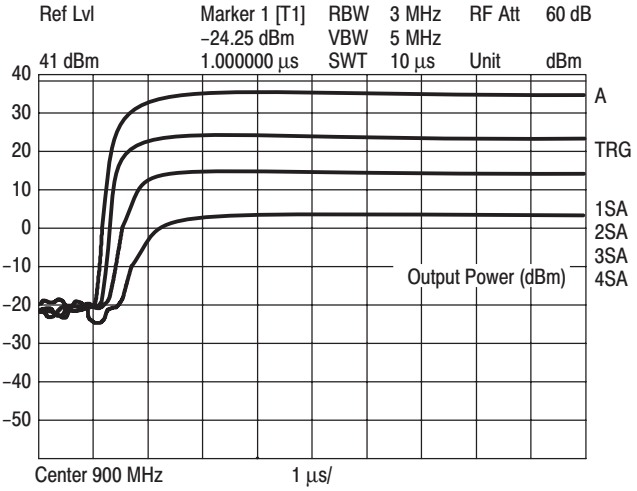


Figure 8. Fall Time for GSM Path at 3.6 V within 30 dB Dynamic range

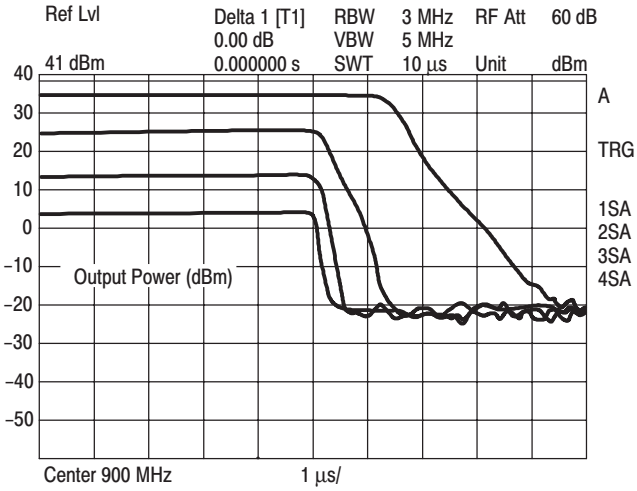


Figure 9. Rise Time for DCS1800 Path at 3.6 V within 30 dB Dynamic Range

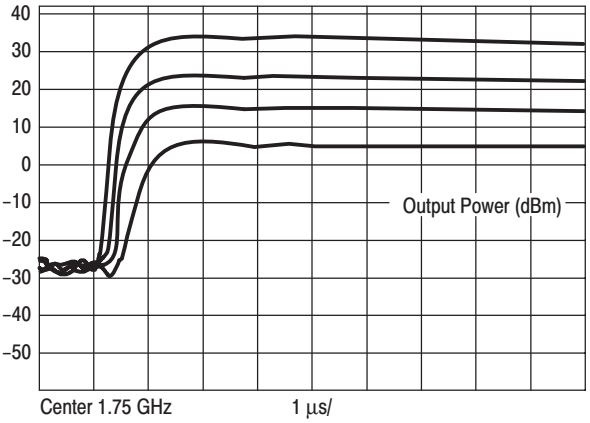


Figure 10. Fall Time for DCS1800 Path at 3.6 V within 30 dB Dynamic Range

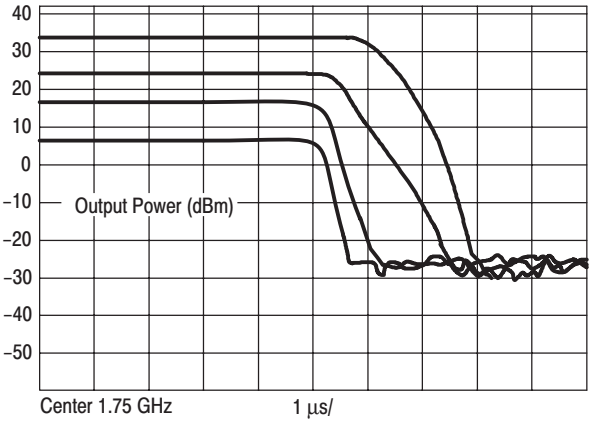


Figure 11. Spurious Spectrum for GSM Path at 3.6 V

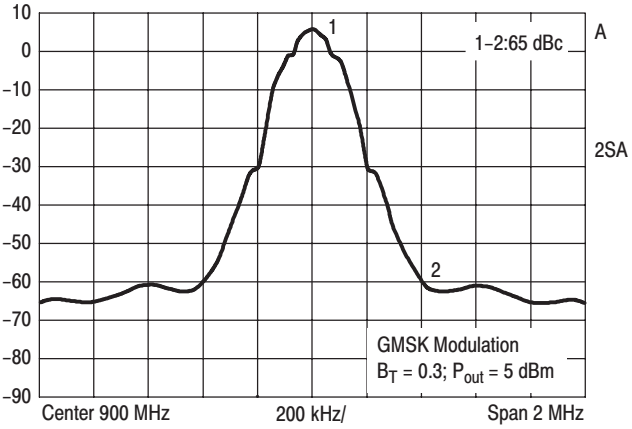


Figure 12. Spurious Spectrum for DCS Path at 3.6 V

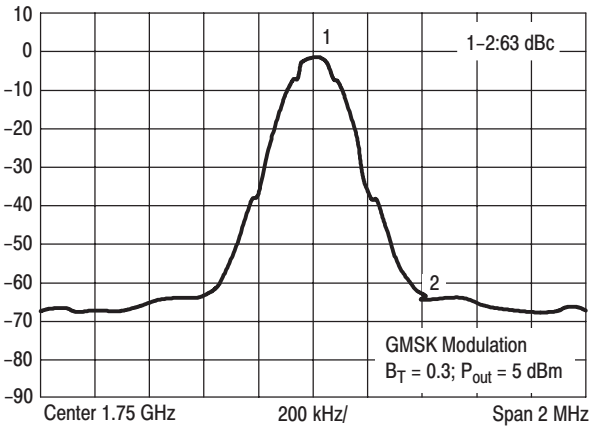
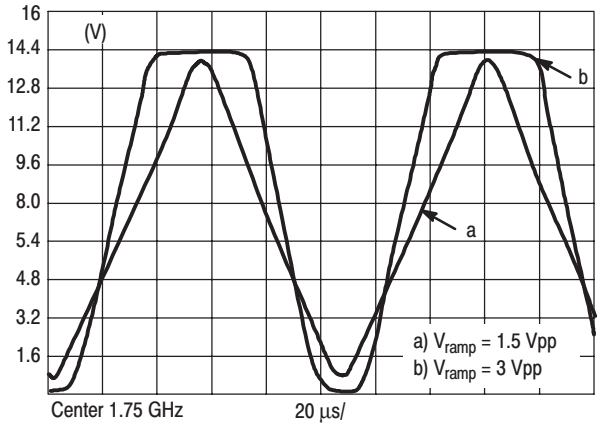


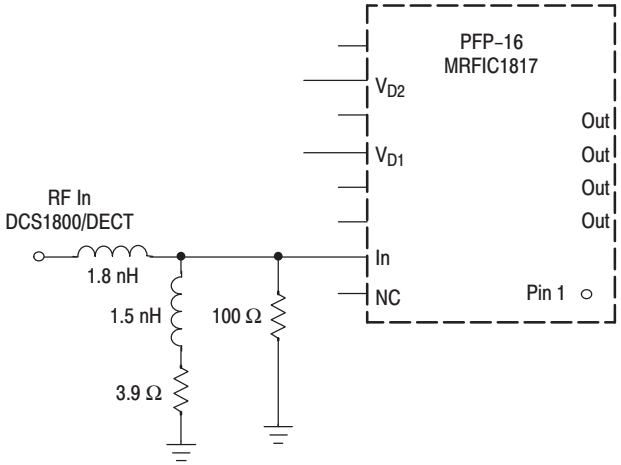
Figure 13. Output RF Voltage Variation with Linear Control Ramp at 3.6 V



DECT

The DCS path can also be evaluated in the DECT band. In that case the quiescent current of the DCS PA needs to be decreased in order to get an acceptable efficiency at about 27 dBm output power. This can be realized by increasing the R14 resistor value to 5.6 kΩ in order to get about –2.7 V at the VCDCS point. The user will also have to change the input matching network in order to match the DECT bandwidth. An example of such an input matching is given Figure 14. In this configuration, the gain on the DCS path is reduced by 2.0 dB because of higher losses at the input.

Figure 14. Input Matching for DCS and DECT Band



Open Loop

The highly linear transfer function achieved with the drain control has been experienced to suppress the control loop. This technique has been called “open–loop” control, and a separate application note, AN1599, describing this technique is available.

The dual band demonstration board is designed to allow the implementation of the open–loop concept. The user can experiment this technique by simply adding a 3 pole Sallen–key filter in the control circuit, in order to smooth the transitions (see Figure 12).

R8 resistor is changed to 1.0 kΩ, R9, R10 need to be set at 4.7 kΩ, C27 (560 pF), C28 (1.5 nF), C29 (1.0 nF) are added and the dual band board can be experimented in open loop mode.

SYSTEM SOLUTION

The antenna interface may require duplexers. Figure 15 shows a possible architecture in which the output switch can be the MRFIC0903. In that configuration the ENSWT pin can be used to control the switch.

Figure 16 shows a possible architecture without duplexer. Since the switch/filter block shown does not exist as a standard product, this demonstration board can help the user define a dedicated switch specification in order to drive the product definition.

MRFIC0913 is also suitable for AMPS standard (with a different matching). MRFIC1817/MRFIC1818 is also usable for PCS band. The application circuit shown here can also be used for other dual mode amplifiers such as AMPS/PCS with small changes in the component implementation.

Figure 15. Dual Band PA Architecture with Duplexers

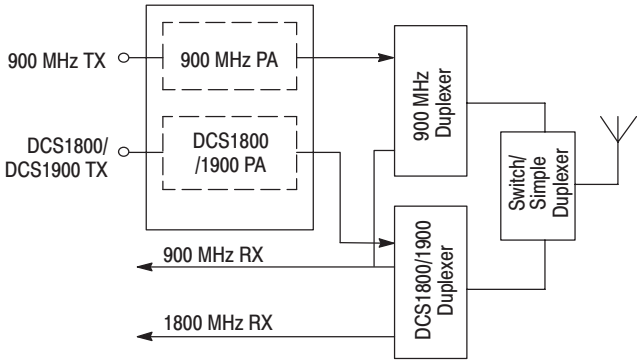


Figure 16. Dual Band PA Architecture without Duplexer

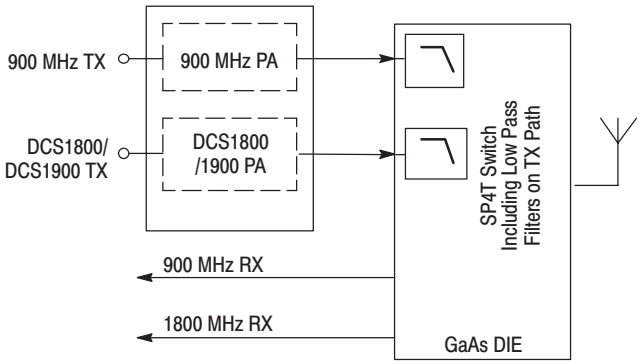
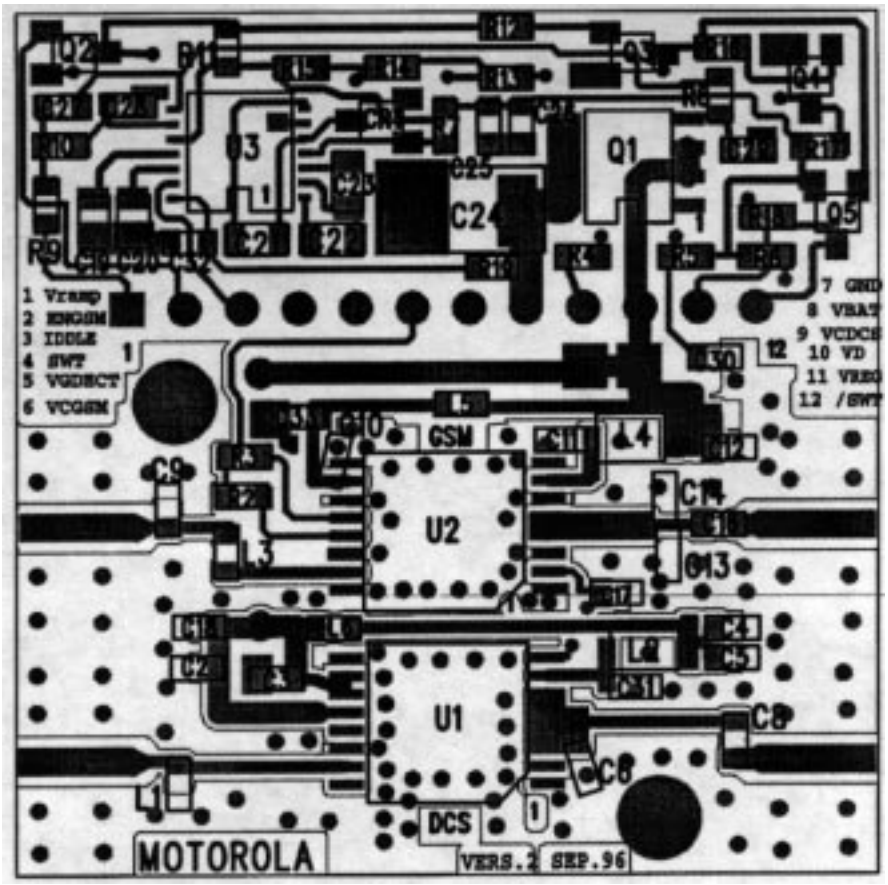


Figure 17. Component Placement for 4.8 V Application



Board Material: FR4 H = 0.48 mm Class 5 PCB (Scale: 3/1)

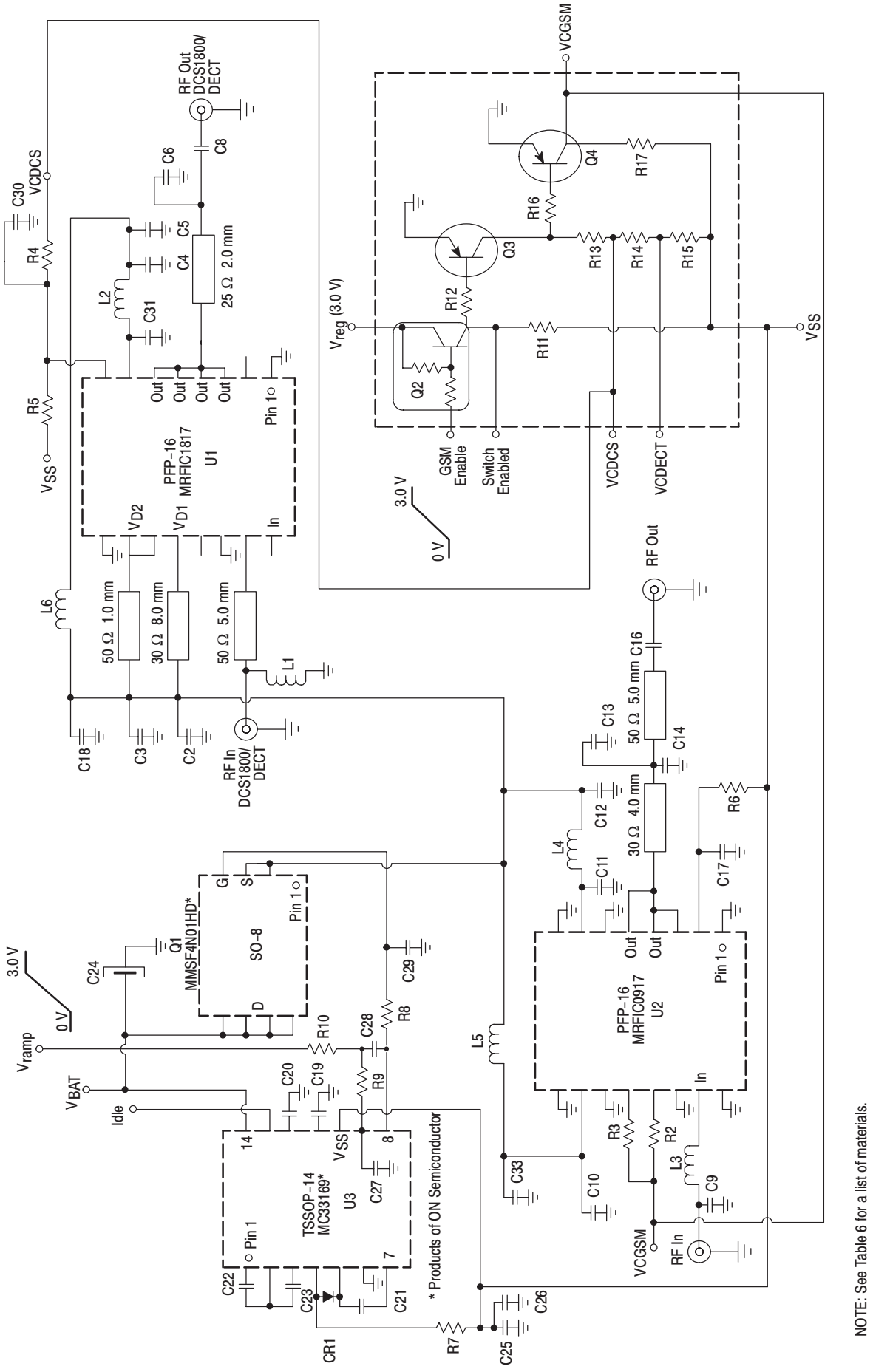


Figure 18. Application Circuit for Dual–Band GSM/DCS1800 PA at 4.8 V using MRFIC0913 and MRFIC1818

NOTE: See Table 6 for a list of materials.

Figure 19. Gain and Return Loss for GSM Path at 4.8 V

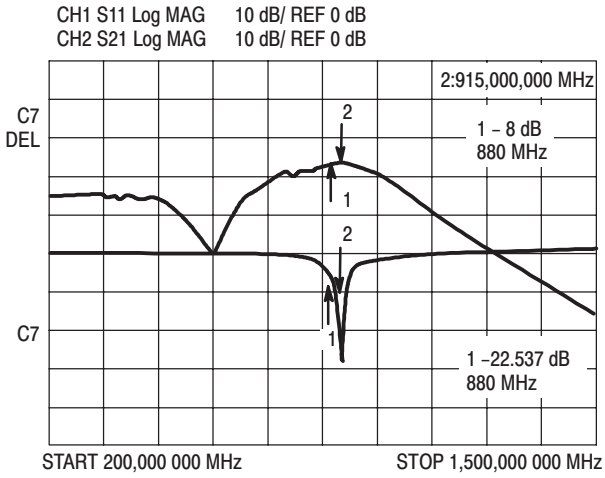
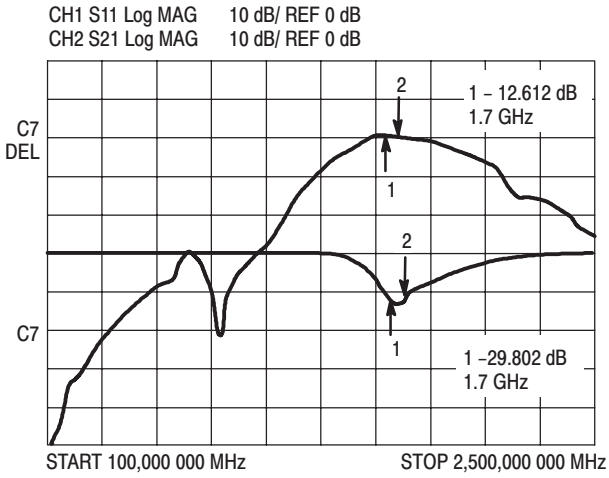


Figure 20. Gain and Return Loss for DCS1800 Path at 4.8 V



CONCLUSION

This demonstration board allows the user to evaluate a GSM/DCS1800 solution for dual band radios or dual band car antenna amplifiers with standard products such as MRFIC0917/MRFIC1817/MC33169/MMSF4N01HD at 3.6 V and MRFIC0913/MRFIC1818/MC33169/MMSF4N01HD at 4.8 V. Reusing these standard products leads to cycle–time reduction, ease–of–use and time–to–market advantages.

The future radio generations are designed for 3.6 V battery. Nevertheless, the dual band radio will have at the beginning more losses on RF path, due to duplexors/switches. A solution could be to use a DC/DC converter associated with 4.8 V PA.

This board is also intended to help the radio designer to define requirements for future dedicated dual band products.

Other dual mode PA can also be evaluated using this board with only some changes in the external matching parts.

ANNEX

Table 3. Minimum and Typical Performances for GSM Path at 4.8 V

ELECTRICAL CHARACTERISTICS (V_{D1}, V_{D2} = 4.8 V, V_{SS} = –4 V, P_{in} = 10 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Frequency Range	880	–	915	MHz
Output Power	34.5	35	–	dBm
Power Added Efficiency	48	–	–	%
Input VSWR	–	2:1	–	VSWR
Harmonic Output 2nd f_o 3rd f_o	 – –	 – –	 –30 –35	dBc
Negative Supply Current	–	–	1.25	mA
Output Power at Low Voltage (V_{D1}, V_{D2} = 4.0 V)	33.3	33.5	–	dBm
Output Power, Isolation (V_{D1}, V_{D2} = 0 V)	–	–20	–15	dBm
3 dB V_{DD} Bandwidth (V_{D1}, V_{D2} = 0 to 6 V)	1.0	–	–	MHz
Noise Power in 100 kHz, 925 to 935 MHz	–	–	–90	dBm

Table 4. Minimum and Typical Performances for DCS Path at 4.8 V

ELECTRICAL CHARACTERISTICS ($V_{D1, 2, 3}$ = 4.8 V, P_{in} = 3 dBm, Peak Measurement at 12.5% Duty Cycle, 4.6 ms Period, T_A = 25°C unless otherwise noted)

Characteristic	Min	Typ	Max	Unit
Frequency Range	1710	–	1785	MHz
V_{DD}	–	4.8	–	V
V_{SS}	–	–4.0	–	V
I_{SS}	–	–	2.0	mA
Output Power at (GSM Pulse)	33	–	–	dBm
Output Power at (GSM Pulse; Low Voltage: V_{DD} = 4.0 V)	31.5	–	–	dBm
Power Added Efficiency	35	40	–	%
Input Return Loss	–	–	–12	dB
Harmonic Output 2nd f_o 3rd f_o	 – –	 – –	 –30 –30	dBc
Output Noise Power (P_{out} Nominal; 100 kHz Bandwidth; 20 MHz above f_o)	–	–	–80	dBm

Table 5. Bill of Material for Dual Band Solution at 3.6 V

Ref	Description	Type	Value	Unit	Comment
C2	Capacitor 0603	NPO	22	pF	
C3	Capacitor 0603	NPO	22	pF	
C4	Capacitor 0603	NPO	22	pF	
C5	Capacitor 0603	X7R	47	nF	
C6	Capacitor 0603 AVX	ACCUF	3.9	pF	
C7	Capacitor 0603 AVX	ACCUF	6.8	pF	
C8	Capacitor 0603	NPO	27	pF	
C9	Capacitor 0603	NPO	5.6	pF	
C10	Capacitor 0603	NPO	33	pF	
C11	Capacitor 0603	NPO	33	pF	
C12	Capacitor 0603	X7R	47	nF	
C13	Capacitor 0603	NPO	10	pF	
C14	Capacitor 0603	NPO	4.7	pF	
C16	Capacitor 0603	NPO	47	pF	
C17	Capacitor 0603	X7R	33	nF	
C18	Capacitor 0603	X7R	47	nF	
C19	Capacitor 0805	X7R	1000	nF	
C20	Capacitor 0805	X7R	1000	nF	
C21	Capacitor 0805	X7R	1000	nF	
C22	Capacitor 0805	X7R	1000	nF	
C23	Capacitor 0805	X7R	1000	nF	
C24	Capacitor	Electro	68	µF	* Not needed when connected to a Battery
C25	Capacitor 0603	X7R	100	nF	
C26	Capacitor 0603	X7R	100	nF	
C27	Capacitor 0603	–	–	–	For open loop
C28	Capacitor 0603	–	–	–	For open loop
C29	Capacitor 0603	–	–	–	For open loop
C30	Capacitor 0603	X7R	6.8	nF	
C31	Capacitor 0603	NPO	1.0	pF	
C32	Capacitor 0603		–	–	N.C.
C33	Capacitor 0603	X7R	47	nF	
R2	Resistor 0603	–	330	Ω	
R3	Resistor 0603	–	1.0	kΩ	
R4	Resistor 0603	–	0	Ω	
R5	Resistor 0603	–	N.C.	–	
R6	Resistor 0603	–	330	Ω	
R7	Resistor 0603	–	100	Ω	
R8	Resistor 0603	–	470	Ω	
R9	Resistor 0603	–	0	Ω	For open loop
R10	Resistor 0603	–	0	Ω	For open loop

Table 5. Bill of Material for Dual Band Solution at 3.6 V (continued)

Ref	Description	Type	Value	Unit	Comment
R11	Resistor 0603	–	10	kΩ	
R12	Resistor 0603	–	120	kΩ	
R13	Resistor 0603	–	2.7	kΩ	
R14	Resistor 0603	–	2.7	kΩ	
R15	Resistor 0603	–	0	Ω	Jumper
R16	Resistor 0603	–	180	kΩ	
R17	Resistor 0603	–	4.7	kΩ	
R18	Resistor 0603	–	N/C	–	
L1	Inductor 0805	–	1.8	nH	TOKO 2012 Series
L2	Inductor 1606–10	–	12	nH	Coilcraft Microspring Series
L3	Inductor 0603	–	8.2	nH	TAIYO YUDEN
L4	Inductor 1606–10	–	12	nH	Coilcraft Microspring Series
L5	strap	–	0	nH	Jumper
L6	strap	–	0	nH	Jumper
CR1	Diode	SOT–23	MMBD701LT1	–	ON Semiconductor
U1	IPA DCS	PFP–16	MRFIC1817	–	
U2	IPA GSM	PFP–16	MRFIC0917	–	
U3		TSSOP–14	MC33169	–	ON Semiconductor
Q1	N–Channel MOSFET	SO–8	MMSF4N01HD	–	ON Semiconductor
Q2	PNP Transistor	SOT–23	MMUN2112LT1	–	ON Semiconductor
Q3	PNP Transistor	SOT–23	BC857LT1	–	ON Semiconductor
Q4	PNP Transistor	SOT–23	BC857LT1	–	ON Semiconductor

Table 6. Bill of Material for Dual Band Solution at 4.8 V

Ref	Description	Type	Value	Unit	Comment
C2	Capacitor 0603	NPO	22	pF	
C3	Capacitor 0603	NPO	22	pF	
C4	Capacitor 0603	NPO	22	pF	
C5	Capacitor 0603	X7R	47	nF	
C6	Capacitor 0603	NPO	3.3	pF	
C8	Capacitor 0603	NPO	27	pF	
C9	Capacitor 0603	NPO	5.6	pF	
C10	Capacitor 0603	NPO	33	pF	
C11	Capacitor 0603	NPO	33	pF	
C12	Capacitor 0603	X7R	47	nF	
C13	Capacitor 0603	NPO	5.6	pF	
C14	Capacitor 0603	NPO	5.6	pF	
C16	Capacitor 0603	NPO	47	pF	
C17	Capacitor 0603	X7R	33	nF	

Table 6. Bill of Material for Dual Band Solution at 4.8 V (continued)

Ref	Description	Type	Value	Unit	Comment
C18	Capacitor 0603	X7R	47	nF	
C19	Capacitor 0805	X7R	1000	nF	
C20	Capacitor 0805	X7R	1000	nF	
C21	Capacitor 0805	X7R	1000	nF	
C22	Capacitor 0805	X7R	1000	nF	
C23	Capacitor 0805	X7R	1000	nF	
C24	Capacitor	Electro	68	µF	* Not needed when Connected to a Battery
C25	Capacitor 0603	X7R	100	nF	
C26	Capacitor 0603	X7R	100	nF	
C27	Capacitor 0603	–	–	–	For Open Loop
C28	Capacitor 0603	–	–	–	For Open Loop
C29	Capacitor 0603	–	–	–	For Open Loop
C30	Capacitor 0603	XR7	6.8	nF	
C31	Capacitor 0603	NPO	1.0	pF	
C32	Capacitor 0805	Y5V	1.0	µF	
C33	Capacitor 0603	X7R	47	nF	
R2	Resistor 0603	–	1.8	kΩ	
R3	Resistor 0603	–	2.7	kΩ	
R4	Resistor 0603	–	0	Ω	
R5	Resistor 0603	–	N.C.	–	
R6	Resistor 0603	–	330	Ω	
R7	Resistor 0603	–	100	Ω	
R8	Resistor 0603	–	470	Ω	
R9	Resistor 0603	–	0	Ω	For open loop
R10	Resistor 0603	–	0	Ω	For open loop
R11	Resistor 0603	–	10	kΩ	
R12	Resistor 0603	–	120	kΩ	
R13	Resistor 0603	–	2.7	kΩ	
R14	Resistor 0603	–	2.2	kΩ	
R15	Resistor 0603	–	0	Ω	Jumper
R16	Resistor 0603	–	120	kΩ	
R17	Resistor 0603	–	4.7	Ω	
R18	Resistor 0603	–	N/C	–	
R19	Resistor 0603	–	100	Ω	
L1	Inductor 0805	–	1.8	nH	TOKO 2012 Series
L2	Inductor 1606–9	–	10	nH	Coilcraft Microspring Series
L3	Inductor 0603	–	8.2	nH	TAIYO YUDEN
L4	Inductor 1606–10	–	12	nH	Coilcraft Microspring Series
L5/L6	Strap	–	0	nH	Jumper

Table 6. Bill of Material for Dual Band Solution at 4.8 V (continued)

Ref	Description	Type	Value	Unit	Comment
CR1	Diode	SOT–23	MMBD701LT1	–	ON Semiconductor
U1	IPA DCS	PFP–16	MRFIC1818	–	
U2	IPA GSM	PFP–16	MRFIC0913	–	
U3		TSSOP–14	MC33169	–	ON Semiconductor
Q1	N–Channel MOSFET	SO–8	MMSF4N01HD	–	ON Semiconductor
Q2	PNP Transistor	SOT–23	MMUN2112LT1	–	ON Semiconductor
Q3	PNP Transistor	SOT–23	BC857LT1	–	ON Semiconductor
Q4	PNP Transistor	SOT–23	BC857LT1	–	ON Semiconductor

NOTES

NOTES

Freescale Semiconductor, Inc.
ARCHIVED BY FREESCALE SEMICONDUCTOR, INC. 2005

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217. 1–303–675–2140 or 1–800–441–2447

Customer Focus Center: 1–800–521–6274

HOME PAGE: http://www.motorola.com/semiconductors

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center,
3–20–1, Minami–Azabu, Minato–ku, Tokyo, 106–8573 Japan.
81–3–3440–3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre,
2, Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.
852–26668334