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MMA1201P Product Overview and Interface Considerations

Prepared by: Carlos Miranda
Systems and Applications Engineer
and
Gary O'Brien
New Product Development Engineer

INTRODUCTION

Silicon micromachined accelerometers designed for a variety of applications including automotive airbag deployment systems must meet stringent performance requirements and still remain low cost. Achieving the requisite enhanced functionality encompasses overcoming challenges in both transducer micromachining and subsequent signal conditioning. Motorola's accelerometer architecture includes two separate elements in a single package to achieve overall functionality: a sensing element ("g–cell") and a signal conditioning element ("control ASIC").

Figure 1 shows a functional block diagram of Motorola's new MMA1201P. The transducer is a surface micromachined differential capacitor with two fixed plates and a third movable plate. The movable plate is attached to an inertial mass. When acceleration is applied to the device, the inertial mass is displaced causing a change in capacitance. The second die is a CMOS control ASIC which acts as a capacitance to voltage converter and conditions the signal to provide a high level output. The output signal has an offset voltage nominally equivalent to $V_{DD}/2$ so that both positive and negative acceleration can be measured.

This document describes Motorola's new MMA1201P accelerometer, which uses a new control ASIC architecture. It explains important new features that have been incorporated into the ASIC, and presents an overview of the key performance characteristics of the new accelerometer. The document also details the minimum supporting circuitry needed to operate a Motorola accelerometer and interface it to an MCU. Finally, the power supply rejection ratio (PSRR) characteristics and an aliasing gain model are presented.

MMA1201P FEATURES

Several design enhancements have been implemented into the new MMA1201P. The oscillator circuit, which is the heart of the ASIC, has been redesigned to improve stability over temperature. A filter has been added to the power supply line for internally generated biases. A new sensing scheme is used to sample the differential capacitor transducer and condition the signal. Finally, the temperature compensation stage has been redesigned to be trimmable. A block diagram representation of the new accelerometer, in a 16 pin DIP package, is shown in Figure 1. For simplicity, the EPROM trim and the self–test circuit blocks have been omitted.

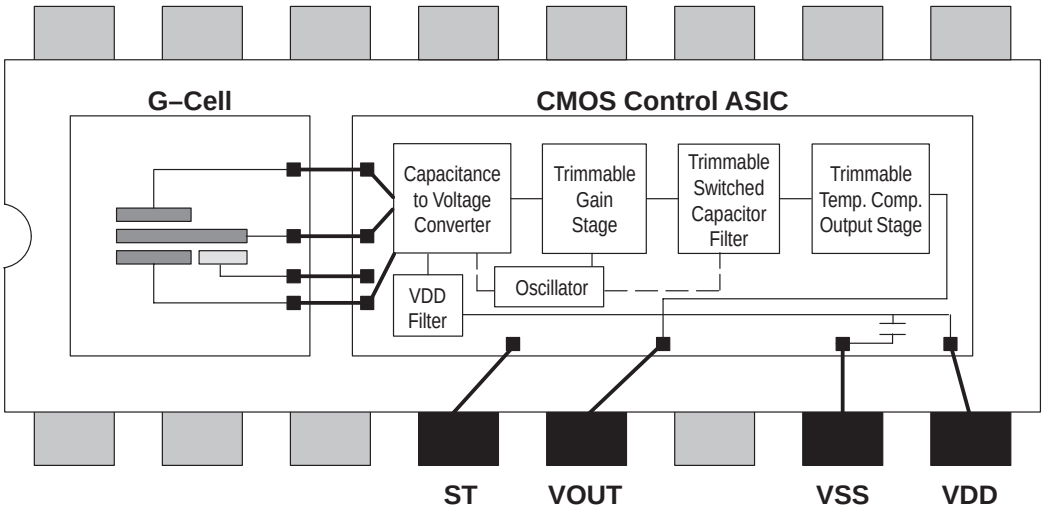

Figure 1. Block Diagram Representing the MMA1201P

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- *Oscillator*
  The oscillator has been redesigned to center the nominal frequency within the trimming range and to have better temperature compensation. As shown in Figure 1, the oscillator controls three switched capacitor circuit sub–blocks within the ASIC, thus having direct impact on their performance. The trimmable oscillator enhances the control of other performance parameters and enables the part to meet tighter specification tolerances. Additionally, the placement of the oscillator on the silicon die has changed, contributing to a 50% reduction in the noise of the part.
- *Power Supply Filter*
  An internal capacitor has been added between the V_{DD} and V_{SS} pins to provide some de–coupling of the power supply. Also, a lowpass filter has been added to the circuitry that supplies power to the transducer element and that sets the DC level of the capacitance–to–voltage converter stage. The filter response suppresses high frequency noise, but maintains a ratiometric output.
- *New Sensing Scheme*
  The capacitance–to–voltage converter employs innovative circuit techniques (at the time of this writing, patents are pending) to improve signal ratiometricity. Amplification is achieved using an EPROM trimmable gain stage, providing capability for both coarse and fine tuning. As in the previous version of the control ASIC, the second gain stage is cascaded by a switched capacitor four pole Bessel lowpass filter, with a unity gain response and –3 dB frequency at 400 Hz.
- *Temperature Compensation*
  The final stage in the ASIC performs temperature compensation of gain. Thus, the temperature coefficient for sensitivity is set using EPROM trim.

PERFORMANCE ENHANCEMENTS

Motorola's new MMA1201P accelerometer provides performance enhancements in a number of areas, including ratiometric output, signal–to–noise ratio, output filter response, and temperature compensation. For complete details, refer to the MMA1201P data sheet.

- *Ratiometric Output*
  The offset voltage and the sensitivity of the part are ratiometric with supply voltage. Typical error values are less than 0.5%.
- *Signal to Noise Ratio*
  The noise has been reduced by 50% and is specified at 3.5 mV_{RMS} maximum. Typical values are about 2.0 mV_{RMS}. As a result, the signal to noise ratio of the part is about 50 dB.
- *Lowpass Filter Response*
  The frequency response of the four pole Bessel lowpass filter has the –3 dB frequency at 400 Hz. The tolerance has been narrowed by 60% and is specified at ±40 Hz.
- *Temperature Compensation*
  The sensitivity is very uniform over temperature, with typical errors of about ±1% over the specified temperature range. Also, although the spec allows for the equivalent of 5 mV/°C for the temperature coefficient of offset, typical values are actually less than 2 mV/°C, at V_{DD} equal to 5 V.

INTERFACE CONSIDERATIONS

With only four active pin connections, Motorola's accelerometers are very easy to use. There are only a few simple considerations to be taken into account to ensure reliable operation and attain the high level of performance that the can part offer.

- *Power Supply*
  Power is applied to the accelerometer through the V_{DD} pin. For optimum performance, it is recommended that the part be powered with a voltage regulator such as the Motorola MC78L05. An optional 0.1 µF capacitor can be placed on the V_{DD} pin to complement the accelerometer's internal capacitor and provide additional de–coupling of the supply. The capacitor should be physically located as close as possible to the accelerometer.
- *Ground*
  Ground is applied through the V_{SS} pin. Whenever possible it is recommended that a solid ground plane be used so that the impedance of the ground path is minimized. If this is not possible, it is strongly recommended that a low impedance trace (no additional components should be connected to it) be used to directly connect the V_{SS} pin to the power supply ground.
- *Self–test*
  The ST pin is an active, high logic level input pin that provides a way for the user to verify proper operation of the part. It is pulled down internally. Therefore, for normal operation, the user could apply a logic level "0" or leave it unconnected. Applying a logic level "1" to the ST pin will apply the equivalent of a 25 g acceleration to the transducer, and the user should see a change in the output equivalent to 25 times the part's rated sensitivity.
- *Output*
  The accelerometer's output is measured at the V_{OUT} pin. As shown in Figure 1, the ASIC's oscillator controls the switched capacitor lowpass filter, with a nominal operating frequency of 65 kHz. As a result, a clock noise component of about 2 mV_{peak} may be present at 65 kHz. Therefore, it is recommended that the user place a simple RC lowpass filter on the V_{OUT} pin to reduce the clock noise present in the output signal. Recommended values are a 1 kΩ resistor and a 0.01 µF capacitor. These values produce a filter with a –3 dB frequency at about 16 kHz, which will not interfere with the response of the internal Bessel filter, yet will provide sufficient attenuation (approximately –12 dB) of the clock noise.

  Placing a filter on the output is especially recommended for applications where the signal will be fed into a stand–alone A/D converter, and in cases where the signal will be amplified to a level where the amplified clock noise may begin to contribute significantly to the noise floor of the system. However, if using an MCU or microprocessor in the system, the user may choose to use a software algorithm to digitally filter the signal, instead of using the analog RC filter. This option would have to be evaluated based on the system performance requirements.

- *Connection to the A/D on an MCU*
  When using the accelerometer with the analog to digital converter on an MCU, it is important to connect the supply and ground pins of the accelerometer and the V_{RH} and V_{RL} pins of the MCU to the same supply and ground traces, respectively. This will maximize the ratiometricity of the system by avoiding voltage differences that may result from trace impedances.

Figure 2 shows the recommended supporting circuitry for operating the new accelerometer. Part (a) shows the16 pin DIP package version, the MMA1201P, while part (b) shows the 6 pin Wingback package version, the MMA2200W. For the MMA1201P, pins 1, 2, 3, 6, 14, 15, and 16 have no internal connections, and pins 9 through 13 are used for calibration and trimming in the factory. These pins should all be left unconnected. For the MMA2200W, pins 1 and 4, and the wings (supporting pins) should be left unconnected.

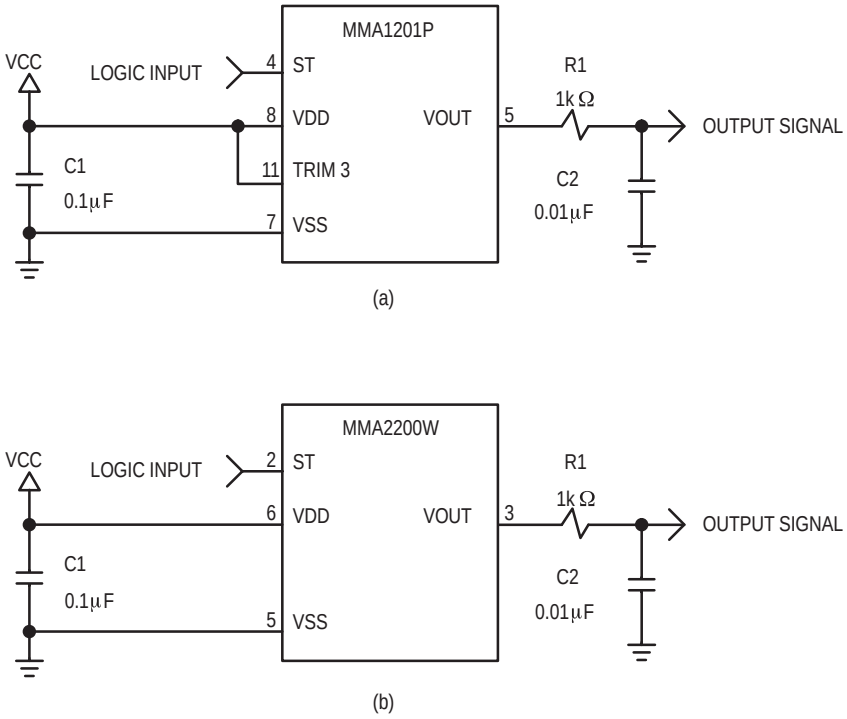

Figure 2. Accelerometers with Recommended Supporting Circuitry

PSRR AND ALIASING GAIN MODEL

Although the operational amplifiers in the MMA1201P's control ASIC have a high power supply rejection ratio with a fairly wide bandwidth, because the accelerometer is in reality a sampled analog system using switched capacitor technology, it is possible that when powered with a switching power supply, noise from the supply will appear in the output signal. This is known as aliasing, the result being a signal with frequency equal to the difference between the frequency of the power supply noise and the accelerometer's sampling frequency. Aliasing gain is defined as the power of the output signal relative to an injected sinusoid on the V_{DD} line powering the accelerometer.

Typical switching power supplies have operating frequencies between 50 and 100 kHz. The operating frequency of the accelerometer's switching capacitor circuitry is roughly 65 kHz. Should the fundamental frequency of the switching power supply, or its harmonics, fall within 400 Hz of the ASIC's fundamental frequency (or its harmonics), then any noise present in the power supply will be aliased into the passband of the accelerometer. As will be explained later in this section, there are several simple ways to avoid aliasing.

As shown in Figure 1, there are many different signal processing stages in the ASIC. As a result, the aliasing gain characteristics of the part are a little bit more complex than explained in the previous paragraph. An analysis was done to characterize the worst case aliasing gain of the accelerometer. Devices from three production lots were used. The parts were tested at 105°C with 5.25 V on V_{DD}. The gain code was set to the nominal value plus 4σ. Thus, the parts had a sensitivity that was approximately twice that of standard parts. Figure 3, shows a plot of the aliasing gain model that was developed. The model is based on the worst case results; typical parts should perform much better having much lower aliasing gain.

The following equation was used to fit the data and generate the model:

$$\text{Aliasing Gain} = 1.6965 + 0.0029 * \text{Freq. (kHz)} + HRC_1 * \text{Freq. (kHz)} + HRC_2$$

where HRC_1 and HRC_2 are coefficients used in the model. Their values vary for each harmonic. Figure 4 lists the values of HRC_1 and HRC_2 for the fundamental frequency and the first 5 harmonics.

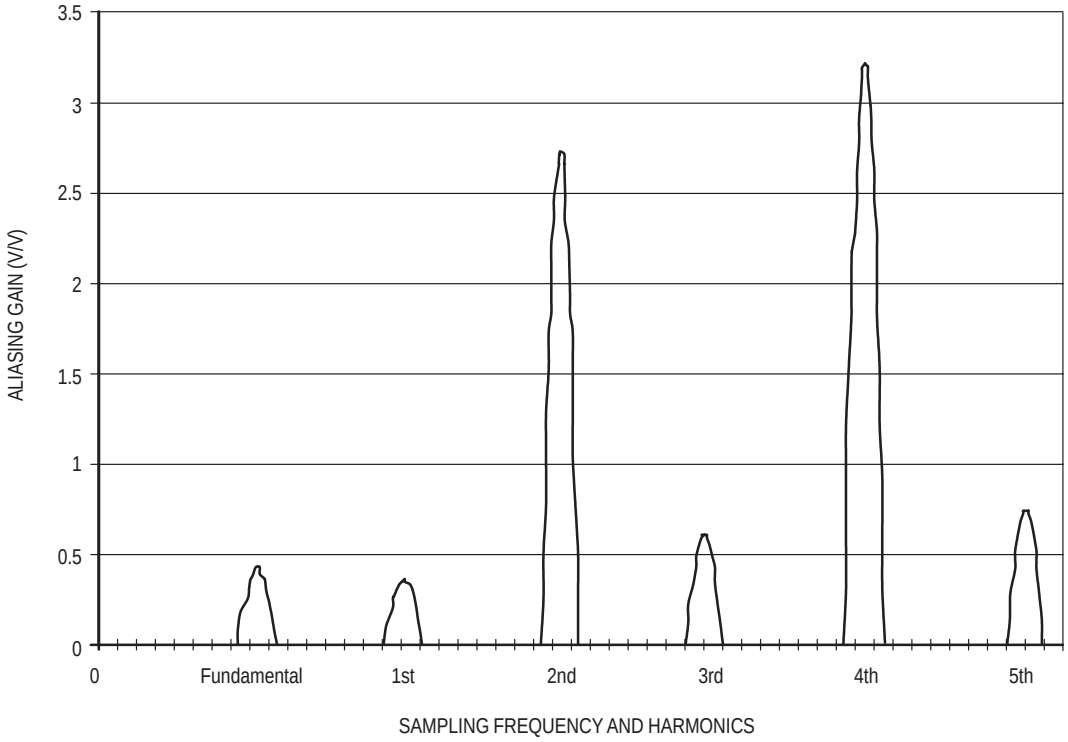

Figure 3. Worst Case Aliasing Gain Model Derived from Characterization Data

Harmonic	Freq. (kHz)	HRC_1	HRC_2	Aliasing Gain
Fundamental	65	0.0101	−2.1120	0.4242
1st	130	−0.0016	−1.4881	0.3674
2nd	195	0.0237	−4.1572	2.7116
3rd	260	−0.0060	−0.2919	0.6007
4th	325	−0.0098	3.7439	3.2017
5th	390	−0.0164	4.3054	0.7361

Figure 4. Values for Worst Case Aliasing Gain Model

The aliasing gain model can be used to estimate the amount of noise that can be expected on the output due to noise in the switching power supply. As an example, consider a switching power supply operating at 65.05 kHz, with peak–to–peak noise levels of 10, 6, 3.3, 2.5, 2, and 1.4 mV for the fundamental and the first five harmonics, respectively. Assume the worst case scenario, an almost perfect match of power supply fundamental frequency with the fundamental of the ASIC and all noise signals in phase. The power supply noise that would be seen at the output due to each harmonic would be calculated as follows:

Harmonic	Aliasing Gain	P.S. Noise	Output Noise
Fundamental	0.4242	10.00 mV	4.24 mV
1st	0.3674	6.00 mV	2.20 mV
2nd	2.7116	3.33 mV	9.04 mV
3rd	0.6007	2.50 mV	1.50 mV
4th	3.2017	2.00 mV	6.40 mV
5th	0.7361	1.40 mV	1.03 mV

The total output noise would be the sum of the individual components:

Total Output Noise = (4.24 + 2.20 + 9.04 + 1.50 + 6.40 + 1.03) mV

Total Output Noise = 24.41 mV peak–to–peak.

If this output signal were fed into an 8 bit A/D converter, referenced to 5 V full scale, the worst case error due to power supply noise would be equivalent to ±1 bit count.

The error that can occur in the output due to aliasing gain can be avoided very easily. The easiest method is to power the part with a voltage regulator. Since the voltage regulator provides a clean, steady supply, the possibility of aliasing is eliminated. If the accelerometer is powered with a switching supply, a filter should be placed on the power supply output to eliminate the noise of the harmonics. If placing a filter on the switching supply is not feasible, the user must ensure that the operating frequency of the switching power supply is outside the frequency ranges of the peaks shown in Figure 3. The plot shown is a superposition of the response of the internal four pole Bessel lowpass filter, scaled by the corresponding aliasing gain for each harmonic. The Bessel filter has the –3 dB frequency at 400 Hz and, being of fourth order, has a very steep roll–off outside the passband, with approximately –80 dB of attenuation at 4 kHz. If a switching power supply must be used, its operating frequency should be at least 800 Hz from the accelerometer's sampling frequency. Any switching noise present will be aliased to 800 Hz or higher, where the attenuation will be approximately –24 dB or lower, thus reducing the power supply induced noise below the part's noise floor.

CONCLUSION

The MMA1201P accelerometer demonstrates Motorola's commitment to continuous product improvement. A new oscillator lowers the noise in the part and enables tighter control of the –3 dB bandwidth of the internal lowpass filter. The supply voltage is routed to the transducer and the DC level reference of the capacitance–to–voltage converter stage through a newly added filter, thus reducing the part's susceptibility to power supply noise. The capacitance–to–voltage converter stage uses new signal conditioning methods, which virtually eliminate ratiometric errors. The temperature compensation for sensitivity is improved, producing a very flat response over temperature. Overall the part offers much enhanced performance and is simpler to use. Equally important, Motorola's MMA1201P accelerometer has remained very price competitive, making it ideal for most applications requiring acceleration sensors.

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