NOTE: The theory in this application note is still applicable, but some of the products referenced may be discontinued.

RF LDMOS Power Modules for GSM Base Station Application: Optimum Biasing Circuit

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INTRODUCTION

The performances of RF power amplifiers for base station transceivers results in a tradeoff between linearity, efficiency and gain. This tradeoff leads to an optimum quiescent current. But the following parameters modify this bias point: temperature range (commonly -40°C/+85°C), supply voltage and bias voltage variations (commonly +/-5%) and manufacturing spread. The purpose of this paper is to present a new biasing circuit which minimizes quiescent current variations suitable for LDMOS RF power transistors.

STANDARD BIASING CIRCUIT

A standard biasing circuit commonly used for Class AB transistors is shown in Figure 1.

For each LDMOS transistor, it is necessary to adjust the R1 and R2 values in order to set the quiescent current as specified at ambient temperature. Laser-trimmable resistors can be used in mass production for that purpose.

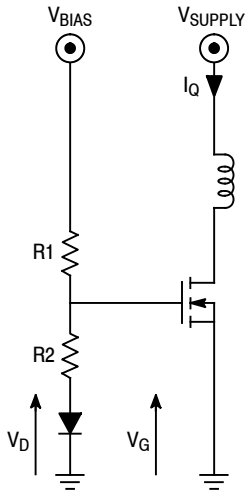

Figure 1. Standard Biasing Circuit

The addition of a diode in series with the two resistors allows for reduction of the quiescent current variation over temperature. We have:

$$V_G = \frac{R2}{R1 + R2} \cdot V_{BIAS} + \frac{R1}{R1 + R2} \cdot V_D \quad \text{(Equation 1)}$$

then,

$$dVg = \frac{R2}{R1 + R2} \cdot dV_{BIAS} + \frac{R1}{R1 + R2} \cdot dVd \quad \text{(Equation 1.bis)}$$

when $dV_{BIAS} = 0$, we have:

$$dVg = \frac{R1}{R1 + R2} \cdot dVd \quad \text{(Equation 2)}$$

Considering variations due to temperature, the coefficient $\frac{dVd}{dT}$ to apply to the LDMOS is related to the bias point, i.e., the quiescent current. For class AB biasing, this coefficient is around -2mV/°C. For full thermal tracking, more than one diode may be required because of the ratio $\frac{R1}{R1 + R2}$ in equation 2.

However, this standard biasing circuit presents two major limitations:

Limitation 1: the manufacturing spread of threshold voltage leads to a different $\frac{R1}{R1 + R2}$ ratio for each die. Therefore, all the die is not compensated for in the same way. A die with a high threshold voltage requires a ratio $\frac{R1}{R1 + R2}$ lower than for a die with a low threshold voltage. Subsequently, the thermal compensation is lower for a die with a high threshold voltage than for a die with a low threshold voltage. This results in quiescent current over or under compensation versus temperature.

Limitation 2: equation 1 shows that Bias voltage variations induce proportional gate voltage variations weighed by a ratio $\frac{R2}{R1 + R2}$. Thus these gate voltage variations lead to quiescent current variations via the die transconductance.

As a result, we have designed a new biasing circuit to cope with those limitations.

NEW BIASING CIRCUIT

The new biasing circuit is shown in Figure 2.

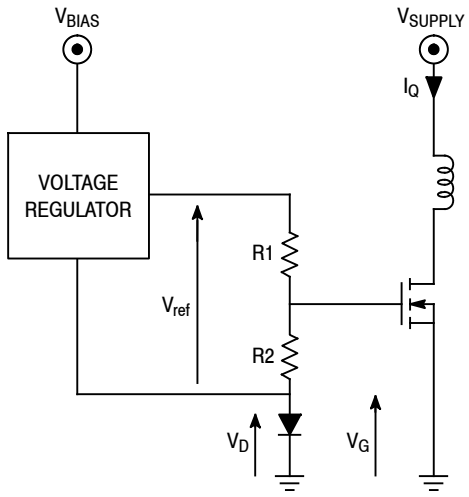

Figure 2. New Biasing Circuit

The bias bridge is adjusted to set the quiescent current as specified at ambient temperature. Laser trimmable resistors can be used in mass production for that purpose.

Thermal tracking is introduced to compensate the quiescent current variations versus temperature. A diode in the bias bridge compensates the LDMOS temperature coefficient. We have now:

$$V_G = \frac{R2}{R1 + R2} \times V_{ref} + V_D \qquad \text{(Equation 3)}$$

Assuming no reference voltage variation versus bias voltage and temperature ($dV_{ref} = 0$), we have:

$$dVg = dVd \qquad \text{(Equation 4)}$$

Thermal tracking: The thermal compensation is now independent of R1 and R2 values and thus independent of the manufacturing spread of transistor's threshold voltage.

Bias voltage variations: As the bias voltage is now regulated, we can see from equation 3 that the bias voltage variations are no longer applied on the gate. This results in a constant quiescent current at a given temperature.

Note that in this case the bias voltage can be directly connected to the power supply voltage.

IMPLEMENTATION

This new biasing circuit is already implemented in three Freescale RF LDMOS power modules designed for GSM base station applications. The MHW910 (10 W GSM900), MHW1810 (10 W GSM1800) and MHW1910 (10 W GSM1900) modules take advantage of this solution.

This new biasing circuit allows keeping this optimum bias point in every temperature and bias voltage combination. One is now able to get the best performances, especially within the whole temperature range.

Another advantage from a customer standpoint is that these new power modules no longer require external bias regulation circuitry for optimum performances.

The voltage regulator used in the MHW910 and MHW1810 is the LP2951. This IC provides the required performances of a very low output voltage temperature coefficient and a very good input voltage variations rejection.

Another feature of the LP2951 is the availability of the shutdown input which allows a logic level signal to turn–off or turn–on the regulator output.

This biasing circuit can be used in the same way for discrete LDMOS transistors as well. Special attention must be taken regarding the DC and RF decoupling.

This circuit guarantees best possible performance by maintaining a constant quiescent current regardless of temperature, bias voltage and gate threshold voltage variations.

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