

AN1676

A Cascade 2 Stage Low Noise Amplifier Using the MRF1047T1 Low Noise Transistor

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INTRODUCTION

This Application Note describes the performance of a cascade LNA circuit using the Motorola MRF1047T1 low noise bipolar transistor. The design demonstrates 19 dBm output IP3 performance, 24 dB gain with 1.6 dB noise figure. The print layout, components list, circuit schematic, simulated and measured data and general information on the LNA circuit are provided.

Design goals for the LNA are based on the requirements for a paging application. These are:

Frequency Range:	920 to 940 MHz
Bias level:	3.3 V and 10 mA max
Noise figure:	1.6 dB
Gain:	20 dB min
Input Return Loss:	-12 dB min
Output Return Loss:	-20 dB min
Input IP3:	-5.0 dBm min
Stability:	Unconditional stability

CIRCUIT APPLICATION

This circuit design is intended to demonstrate the performance of the MRF1047T1 in a cascade LNA design for a pager application. The circuit provides a good compromise between low NF, high IP3 and high return losses with unconditional stability.

DEVICE SELECTION

The Motorola MRF1047T1 is a low noise bipolar junction transistor, which, along with the MRF1027T1 and MRF1057T1 comprise a family of sub-micron geometry devices. The main difference between these devices is their current carrying capabilities. The data sheet for the MRF1047T1 shows it to have a 12 GHz peak transition frequency, f_t at 15 mA, 1.0 dB minimum noise figure, NF_{min} , 14 dBm output power at 1.0 dB gain compression, P_{1dB} and a maximum of 26 dBm for the output third order intercept, OIP3. This transistor is available in the industry standard SC-70 package and is ideally suited for low voltage, high frequency wireless applications. The MRF1047T1 was preferred for this design over the MRF1027T1 and MRF1057T1 because it offers a good compromise between the higher gain at low current of the MRF1027T1 and the low impedance of the MRF1057T1 and because of its noise performance and high IP3 qualities.

BIASING AND MODEL DESCRIPTION

The LNA is designed to operate from a typical supply voltage (V_{CC}) of 3.3 V and have low power consumption. The collector current (I_C) maximum is limited to 10 mA. The basic bias networks for each stage utilize passive components. For the first stage a collector resistor of 100 Ω and a base resistor of 130 k Ω comprise the bias network. For the second stage, a 75 k Ω resistor fed through the collector resistance is used. This stabilizes the collector current to 9.2 mA, $\pm 20\%$ for h_{FE} ranges of 100 to 200. This scheme is not intended to provide bias stability over temperature. Active bias circuitry can be added to improve stability over temperature and reduce the impact of variation of h_{FE} on performance. Motorola's MDC5001, a bias stabilizer chip, can be incorporated into the design for improved stabilization over temperature.

Design of the cascade LNA circuit relied on use of the MRF1047T1 Spice Gummel-Poon model, which includes the packages parasitics of the SC-70. The accuracy of the model can be seen in the comparison between the measured and simulated results.

CIRCUIT DESIGN

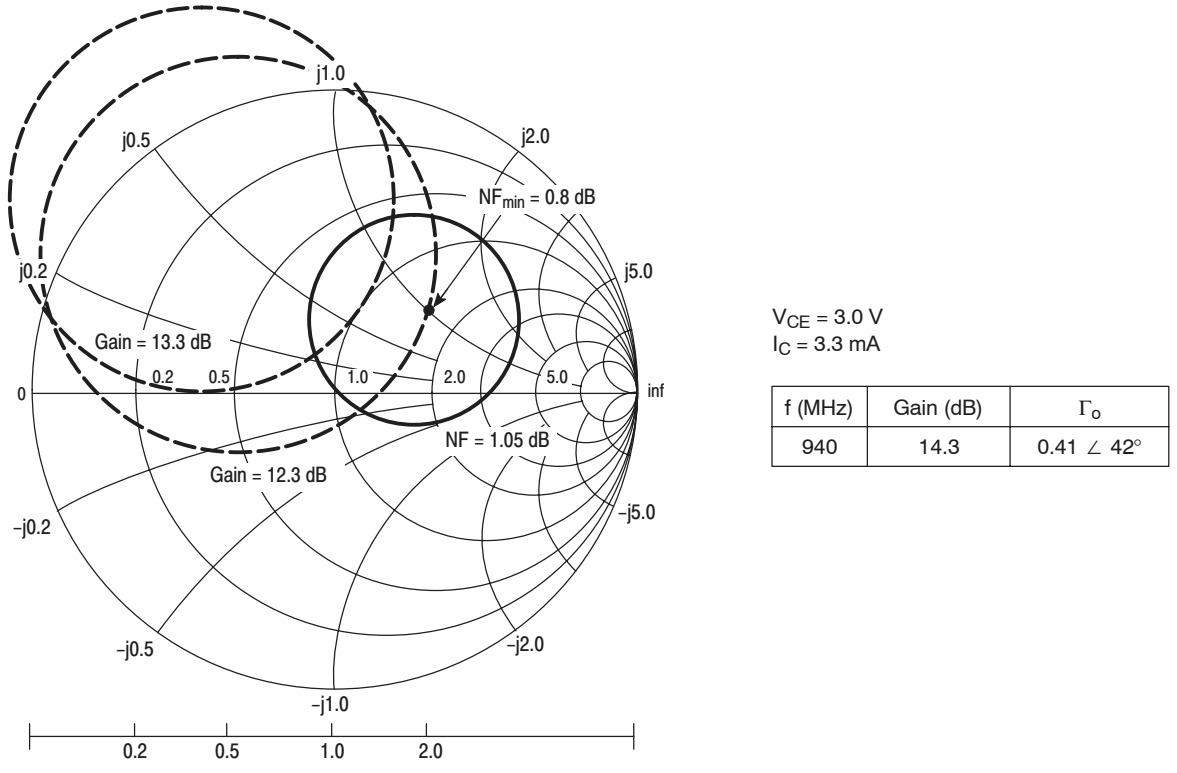
This two stage cascade LNA design uses both transistors in the common emitter configuration. Negative feedback in the emitter legs provides a means of matching noise and gain. The emitters are connected to ground through a 1.0 nH inductor to bring the optimum reflection coefficient (Γ_o) closer to S_{11}^* . This results in an improvement in the NF and IRL tradeoff. The value of the inductor is low due to its negative impact on gain. Both the input and output are capacitively coupled to prevent dc from affecting adjacent circuitry.

First Stage

Since the noise figure of the first stage sets the noise performance of the entire design as well as the sensitivity, the first stage is designed to have the lowest possible noise figure. This is accomplished by setting the input match to Γ_o rather than a conjugate match. Noise and gain circles are plotted using the circuit simulator to find the best input match at the required bias and frequency. These are shown in Figure 1. With optimum noise match a 0.8 dB NF is achieved in the first stage. To meet the -12 dB input return loss (IRL) requirement the input match uses a 3.9 nH inductor in series with a blocking capacitor. This provides the lowest noise figure while surpassing the IRL design requirement. The base dc is fed through a 56 nH shunt inductor, which improves the IP3 performance of the LNA.

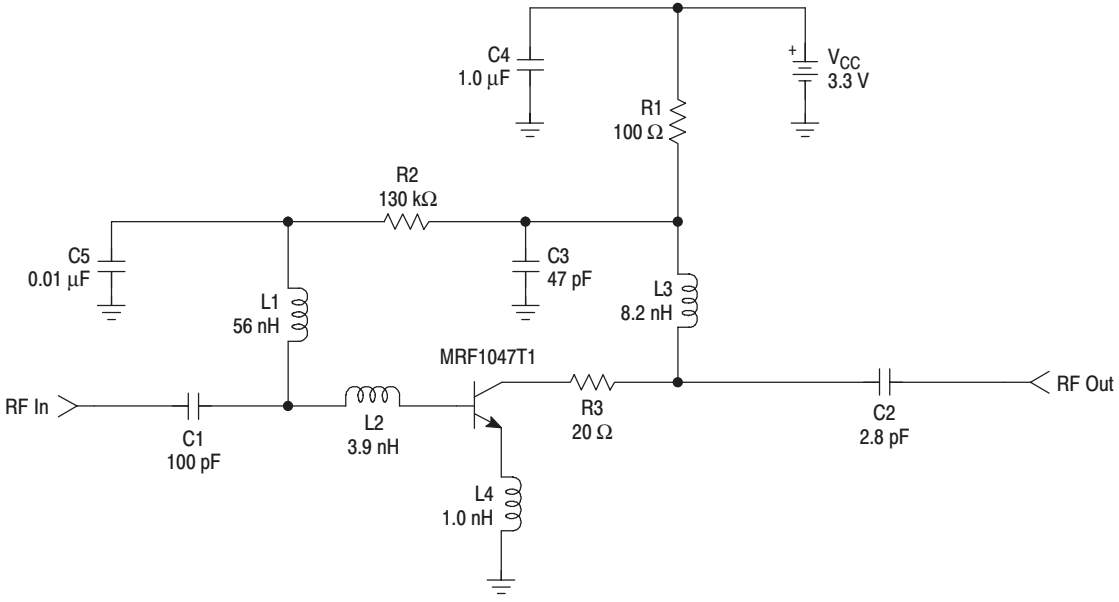


Figure 1. Noise and Gain Circles



The output of the first stage is conjugately matched to the MRF1047T1. The output match of the first stage consists of an 8.2 nH inductor, which serves as a tuning element and dc bias feed, followed by a small series dc blocking capacitor of 2.8 pF.

Figure 2. First Stage of the LNA Using the MRF1047T1



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Second Stage

The second stage is designed to optimize IP3 and gain. NF is less important in this stage. Both the input and output of this stage are conjugately matched to the active device. The second stage input match uses a 10 nH parallel inductor, which also serves as a dc feed, resulting in better IP3. The

output match of the second stage is similar to that of the first stage, having a parallel inductor of 8.2 nH and a series capacitor of 2.8 pF. This matching network provides the best IP3 while meeting the gain and output return loss requirements. The IP3 contours for 940 MHz are shown in Figure 3.

Figure 3. IP3 Contours

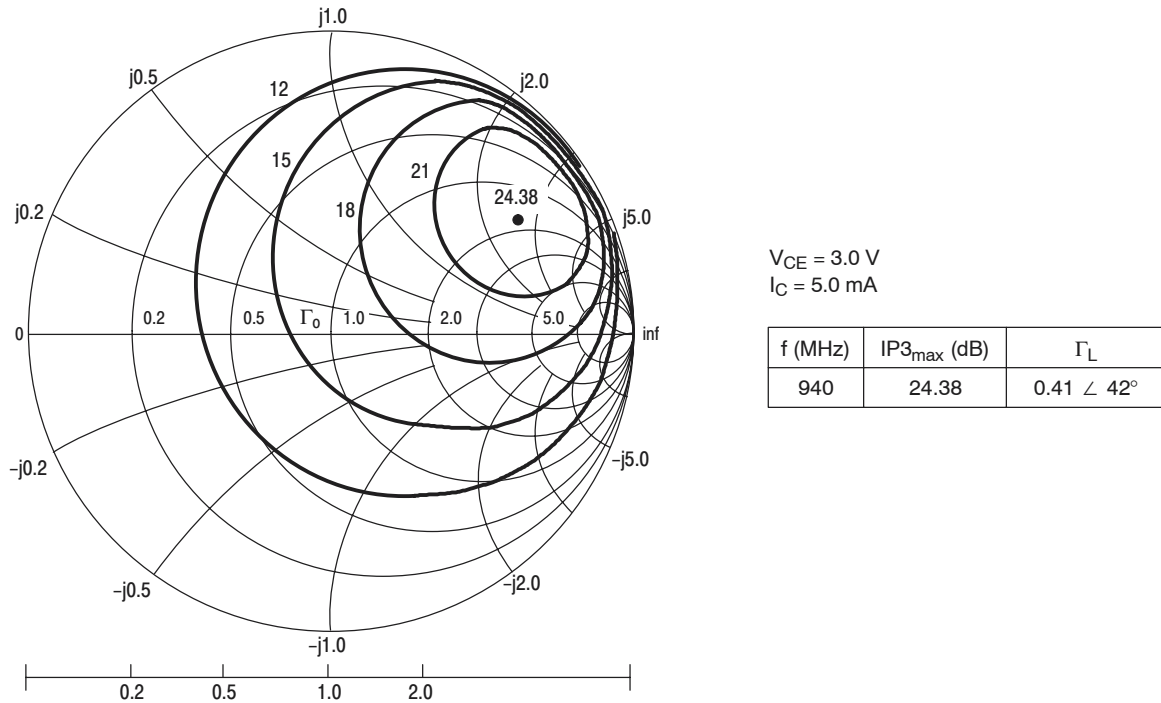
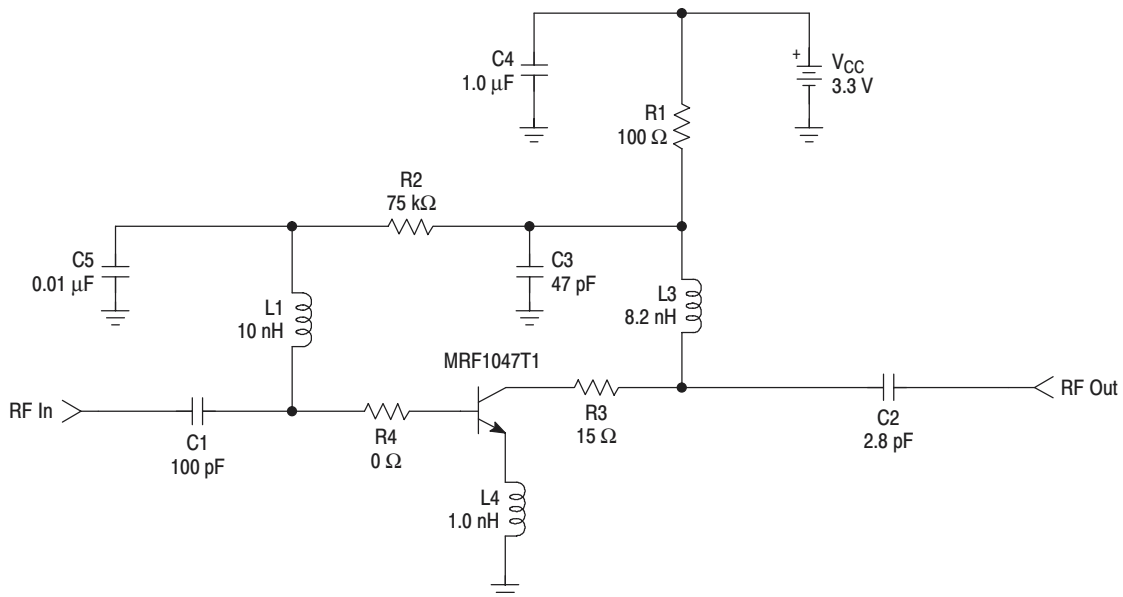


Figure 4. Second Stage of the LNA Using the MRF1047T1



Unconditional stability was one of the design goals for this circuit. Stability improves by decreasing the feedback through the collector-to-base capacitance and adding resistance to the input or output of the device. The disadvantage of using a resistor in the output of the device is degradation in gain, IP3 and NF. The degree of degradation to the noise figure depends on the reverse transmission insertion gain. However, noise figure is affected when a resistor is placed in the input of the device. Since the LNA was intended to provide gain while adding minimum noise, series resistors are inserted at the device outputs. A 20 Ω resistor is used in the first stage and a 15 Ω resistor is used in the second stage to enhance overall stability. The tradeoff in achieving unconditional stability is a gain degradation of 1.5 dB and a IP3 reduction of 2.0 dBm.

Another option to improve the stability of the LNA is inserting a shunt capacitor in the base and/or in the collector

that will result in a RF short at the frequency where oscillation is occurring.

BOARD LAYOUT AND LIST OF COMPONENTS

Simulated circuit performance can only be achieved with measured board performance if the components used in the design are carefully chosen. Component value tolerances, Q and resonant frequency affect performance. Board material may also cause the measured results to fall short of the design goals. For this demonstration the board is constructed from two layers of FR4 with ground planes connected by through vias. The first layer of FR4 is used to create the microstrip lines. The second, thicker layer of FR4 adds thickness, which improves the strength of the solder connections to the SMA connectors. See Figure 5.

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Figure 5. Demonstration Board Layout Used for Both Stages

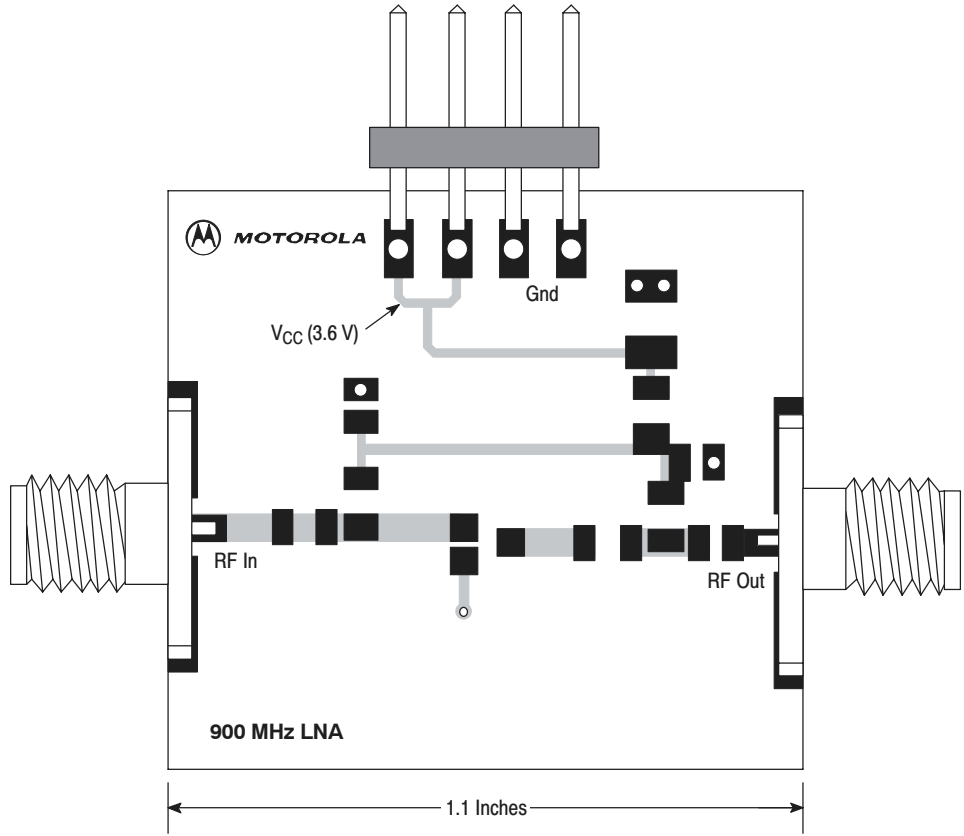


Figure 6. First Stage PCB Board Layout and Parts Placement

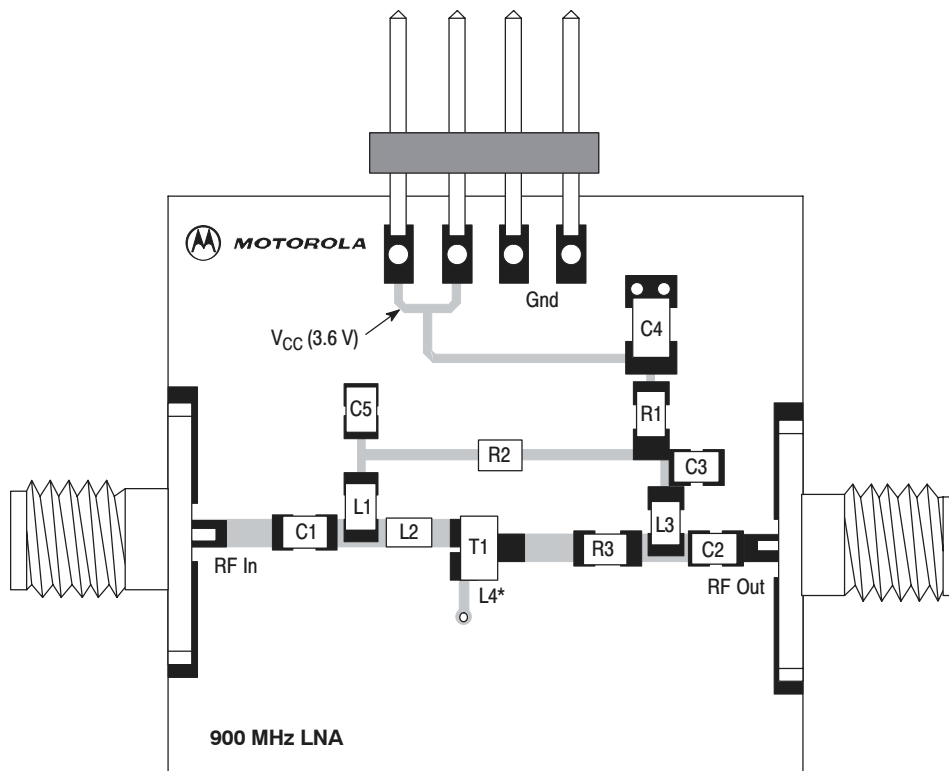


Figure 6 shows the printed circuit board layout and parts placement for the first stage, and Table 1 shows the list of components used on the LNA demo board first stage.

Table 1. List of Components for the First Stage

Component	Value	Comments
C1*	100 pF	DC Block
C2*	2.8 pF	DC Block and Output Match
C3*	47 pF	900 MHz Short
C4*	1.0 μ F	RF Short
C5*	0.01 μ F	Bypass and Improve IP3
L1**	56 nH	Improve IP3
L2**	3.9 nH	Input Match
L3**	8.2 nH	DC Feed, Improve IP3 and Output Match
L4	1.0 nH	100 mil x 15 mil (Printed Inductor) Stability
R1***	100 k Ω	Bias
R2***	130 k Ω	Bias
R3***	20 Ω	Stability
Via Substrate	FR4	D = 15 mil, H = 25 mil ϵ_r = 4.5, H = 25 mil, T = 1.75 mil

* ATC chip caps: 100 A series, case size: 0.055" x 0.055", Q: >10000 @ 1.0 MHz.

** Toko chip inductors: LL2012 series, 0805 package.

*** KOA Speer flat chip resistors, Part#: RK73H2A-F, 1% tolerance, 0805 package.
Additional piece parts required: Two SMA connectors and one single row 4 pin header.

Figure 7. Second Stage PCB Layout and Parts Placement

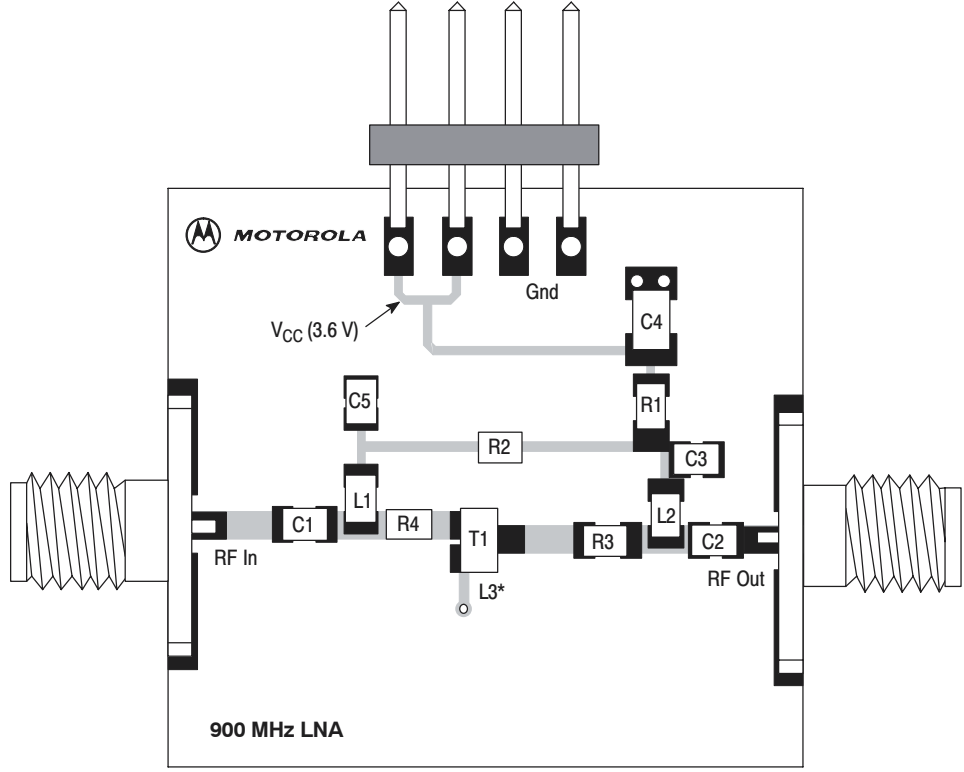


Figure 7 shows the printed circuit board layout and parts placement for the second stage, and Table 2 shows the list of components used on the LNA demo board second stage.

Table 2. List of Components for the Second Stage

Component	Value	Comments
C1*	100 pF	DC Block
C2*	2.8 pF	DC Block and Output Match
C3*	47 pF	900 MHz Short
C4*	1.0 μF	RF Short
C5*	0.01 μF	Bypass and IP3 Improvement
L1**	10 nH	Input Match and Improve IP3
L2**	8.2 nH	Output Match
L3**	1.0 nH	100 mil x 15 mil (Printed Inductor) Stability
R1***	100 kΩ	Bias
R2***	75 kΩ	Bias
R3***	15 Ω	Stability
R4***	0 Ω	
Via Substrate	FR4	D = 15 mil, H = 25 mil ε _r = 4.5, H = 25 mil, T = 1.75 mil

* ATC chip caps: 100 A series, case size: 0.055" x 0.055", Q: >10000 @ 1.0 MHz.
 ** Toko chip inductors: LL2012 series, 0805 package.
 *** KOA Speer flat chip resistors, Part#: RK73H2A-F, 1% tolerance, 0805 package.
 Additional piece parts required: Two SMA connectors and one single row 4 pin header.

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LNA PERFORMANCE

The design goals for this LNA specify a gain of 20 dB minimum, input return loss of -12 dB minimum, output return loss of -20 dB minimum, an input IP3 of -5.0 dBm minimum, NF of 1.6 dB with unconditional stability. The measured gain of this LNA is 24 dB across the frequency range, which exceeds the gain minimum specified in the design goals. Additional gain is undesirable because of the potential for increasing the intermodulation distortion products in the subsequent mixer stage. The output IP3 measured on the

board is 19 dBm, demonstrating very good linearity. Another way to quantify the linearity of this LNA is with the 1.0 dB compression point (P_{1dB}) parameter, which specifies the output power where the linear gain is 1.0 dB below its projected value. As a general rule of thumb the P_{1dB} of a LNA is 10 dB below the output IP3. This LNA has 9.0 dBm output power when gain is compressed by 1.0 dB. The measured noise figure of 1.6 dB offers a low contribution to signal degradation through the LNA circuit. Additionally, the output and input stability circles are completely outside the Smith chart in this design.

Figure 8. Simulated IRL and ORL

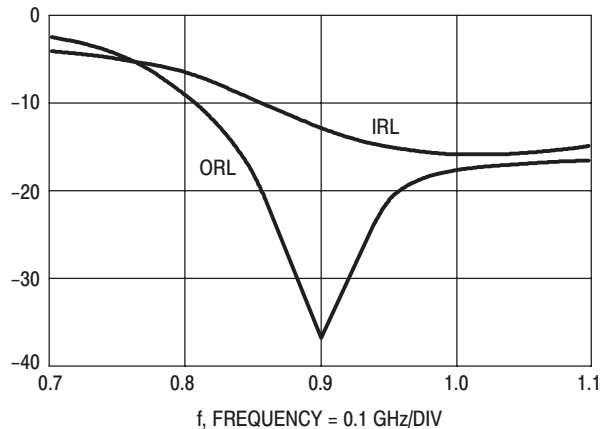
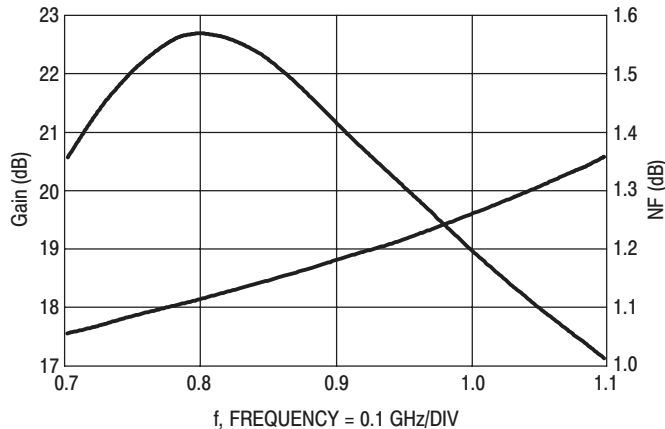


Figure 9. Simulated Gain and Noise Figure



Detailed simulation RF performance is shown in Table 3 and the measured data is shown in Table 4.

Table 3. Simulated RF Performance

Frequency (MHz)	S[1,1] (dB)	S[2,1] (dB)	S[2,2] (dB)	NF (dB)	OIP3 (dBm)
920	-13.7	20.8	-25.7	1.24	19.2
930	-14.2	20.6	-23	1.24	19.4
940	-14.6	20.4	-21.5	1.25	19.6
950	-14.9	20.1	-20.3	1.26	19.9
960	-14.2	20.0	-23	1.26	20

Table 4. Measured RF Performance

Frequency (MHz)	S[1,1] (dB)	S[2,1] (dB)	S[2,2] (dB)	NF (dB)	OIP3 (dBm)
920	-13.6	24.1	-53.6	1.6	18.7
940	-15	24	-54	1.6	19
950	-16	23.9	-54.1	1.6	19.3


CONCLUSION

This cascade LNA circuit was designed to demonstrate the performance of the MRF1047T1 in an unconditionally stable, low power consumption, low noise, high IP3 design for paging applications. A noise figure of 1.6 dB, gain of 24 dB and 19 dBm output IP3 were measured at 940 MHz, meeting

the design goals for the pager application. While this circuit design offers a good compromise between competing performance characteristics, tradeoffs in gain, NF or IP3 offer opportunities for increased performance for a particular application by varying the matching elements using the information provided in this application note.

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