

# BurstRAM to ZBT™ RAM

Prepared by: Joe Haas

The recent product announcements for the ZBT family of synchronous memories have received a warm reception with a wide range of customers. The ability to perform back-to-back read/write cycles without any intermediate deselect cycles offers a substantial performance improvement for a variety of platforms which now utilize standard BurstRAMs. This application note describes some of the footprint changes required to adapt a current BurstRAM socket to a ZBT device. In addition, some of the operational differences are also discussed.

## PINOUT DIFFERENCES

Figure 1 shows a comparative pinout for the MCM69P737 BurstRAM and the MCM63Z736 ZBT RAM. Note there are relatively few pinout differences, most of which are easily modified. The changes in pin assignment required to modify a BurstRAM socket to a ZBT device are listed in Table 1.

The ZBT devices do not have a global byte write pin (SGW), but instead relies upon the state of the byte select inputs (SBa – SBd) to select the current byte write mode. The SGW functionality is replicated by forcing all four of the byte selects to a binary low state during a write cycle instantiation (SBa – SBd = 0). Figure 2 shows a gate-level description of an external implementation of SGW in combination with SW.

Another difference of interest to the designer is that of the simplified burst logic. The ZBT has only the ADV pin to indi-

cate burst cycles. Address and control information is latched with ADV = 0 to initiate a burst cycle. Subsequent cycles have ADV = 1 which causes the address and control inputs to be ignored until the ADV pin is deasserted. For most burst mode applications, tying the BurstRAM ADSC to the ZBT ADV will accomplish the burst functionality.

## FUNCTIONAL DIFFERENCES

The primary functional difference between the ZBT and BurstRAM involves the write cycles (both burst and non-burst). A typical pipelined BurstRAM (ie., the MCM69P737) requires write data to be presented to the part coincident with the address at the initiation of the write cycle. The ZBT, however, is pipelined for both reads and writes, so the write data is latched into the part two (2) clock cycles after the initiation of the write. It is this one fundamental difference that will require the most attention on the part of the circuit designer.

## CONCLUSION

While logic changes may be required for most BurstRAM applications, the conversion to a ZBT architecture should require minimal effort on the part of PCB layout teams. In addition, the logic changes are generally manageable and should require only a modest effort on the part of the circuit designer to allow quick and easy migration to this new and exciting memory technology.

**Table 1. Pipelined BurstRAM and ZBT Pin Assignment Differences**

Pin Locations	BurstRAM Pin Assignment	ZBT Pin Assignment
14	NC	V <sub>DD</sub>
16	NC	V <sub>DD</sub>
64	NC	V <sub>SS</sub>
66	NC	V <sub>DD</sub>
83	ADV	NC
84	ADSP	NC
85	ADSC	ADV
87	SW	CKE (Tie to V <sub>SS</sub> )
88	SGW	SW

ZBT and Zero Bus Turnaround are trademarks of Integrated Device Technology, Inc., and the architecture is supported by Micron Technology, Inc. and Freescale, Inc.

© Freescale Semiconductor, Inc., 2004. All rights reserved.

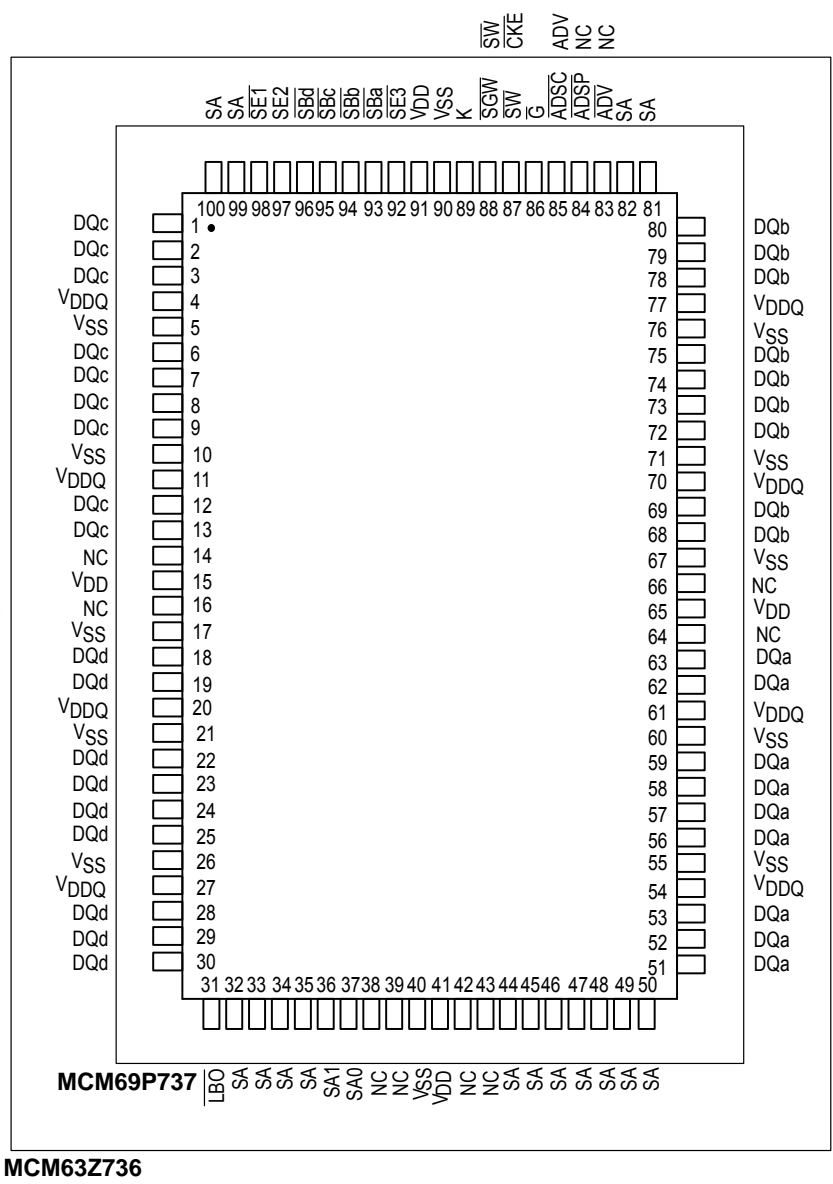


Figure 1. Pipelined BurstRAM and ZBT Pinout Comparison

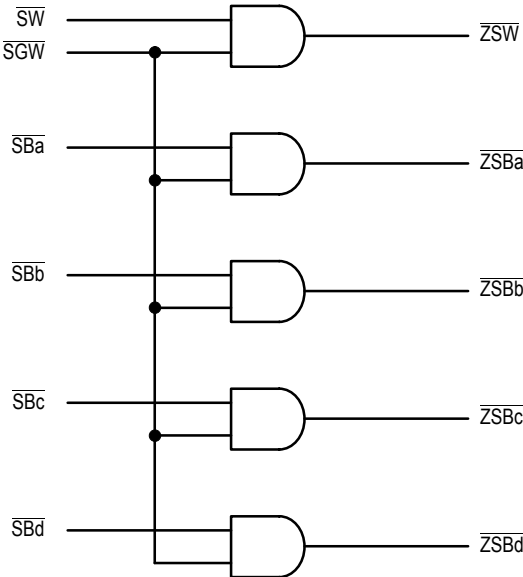


Figure 2. External  $\overline{SGW}$  Logic

## How to Reach Us:

### Home Page:

[www.freescale.com](http://www.freescale.com)

### E-mail:

[support@freescale.com](mailto:support@freescale.com)

### USA/Europe or Locations Not Listed:

Freescale Semiconductor  
 Technical Information Center, CH370  
 1300 N. Alma School Road  
 Chandler, Arizona 85224  
 +1-800-521-6274 or +1-480-768-2130  
[support@freescale.com](mailto:support@freescale.com)

### Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH  
 Technical Information Center  
 Schatzbogen 7  
 81829 Muenchen, Germany  
 +44 1296 380 456 (English)  
 +46 8 52200080 (English)  
 +49 89 92103 559 (German)  
 +33 1 69 35 48 48 (French)  
[support@freescale.com](mailto:support@freescale.com)

### Japan:

Freescale Semiconductor Japan Ltd.  
 Headquarters  
 ARCO Tower 15F  
 1-8-1, Shimo-Meguro, Meguro-ku,  
 Tokyo 153-0064  
 Japan  
 0120 191014 or +81 3 5437 9125  
[support.japan@freescale.com](mailto:support.japan@freescale.com)

### Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.  
 Technical Information Center  
 2 Dai King Street  
 Tai Po Industrial Estate  
 Tai Po, N.T., Hong Kong  
 +800 2666 8080  
[support.asia@freescale.com](mailto:support.asia@freescale.com)

### For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center  
 P.O. Box 5405  
 Denver, Colorado 80217  
 1-800-441-2447 or 303-675-2140  
 Fax: 303-675-2150  
[LDCForFreescaleSemiconductor@hibbertgroup.com](mailto:LDCForFreescaleSemiconductor@hibbertgroup.com)

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document. Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters which may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.