AN1737

Migrating from the MC68HC705J2 to the MC68HC705JJ7

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Introduction

This application note describes the changes needed in both hardware and software to migrate a design from the MC68HC705J2 (J2) to the MC68HC705JJ7 (JJ7). Not only is the JJ7 less expensive than the J2, but migrating to the JJ7 also allows the designer to utilize some of its features not found on the J2.

The JJ7's additional features are:

- 6160 bytes of user EPROM; J2 has 2064 bytes
- 224 bytes of low-power user RAM; J2 has 112 bytes
- 64 bits of personality EPROM, serial port accessible
- 16-bit programmable timer with input capture and output compare
- Simple serial input/output port (SIOP) with interrupt capability
- Two voltage comparators, one of which can be combined with the 16-bit programmable timer to create a 4-channel, single-slope A/D (analog-to-digital) converter
- Output of voltage comparator can drive port pin PB4 directly under software control
- High-source/sink current capability on six I/O (input/output) pins

- Selectable software programmable pulldowns on all I/O pins and keyboard scan interrupt on four I/O pins
- Software mask and request bit for IRQ interrupt
- On-chip oscillator with device option of crystal/ceramic resonator or RC operation and MOR (mask option register) selectable shunt resistor, approximately 2 MΩ
- Internal oscillator for lower-power operation, approximately 100 kHz; 500 kHz selected as device option
- EPROM security bit[1] to aid in locking out access to programmable EPROM array
- Selectable STOP conversion to halt and option for fast 16-cycle restart and power-on reset
- On-chip temperature measurement diode
- Selectable low-voltage inhibit to reset CPU in low-voltage conditions
- Internal steering diode and pullup device on $\overline{\text{RESET}}$ pin to V_{DD}

Additional features of the JJ7 are addressed later in this application note.

Migrating to the JJ7

The minimal changes required to move from the J2 to the JJ7 are illustrated in this section.

Pinouts and Package Types

Because the JJ7 has a different pinout than the J2, layout changes are necessary when migrating. The pinout was changed on the JJ7 to decrease noise susceptibility. The power and XTAL pins were put close together to ensure proper grounding of the crystal circuit. See **Figure 1** and **Figure 2** for illustrations of the pinouts.

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the EPROM/OTPROM difficult for unauthorized users.

Both parts are available in either plastic DIP (dual in-line package) or SOIC (small outline integrated circuit) packages.

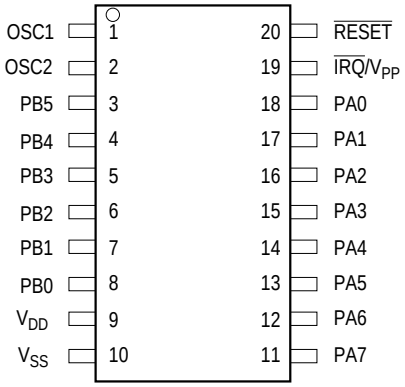


Figure 1. MC68HC705J2 Pinout

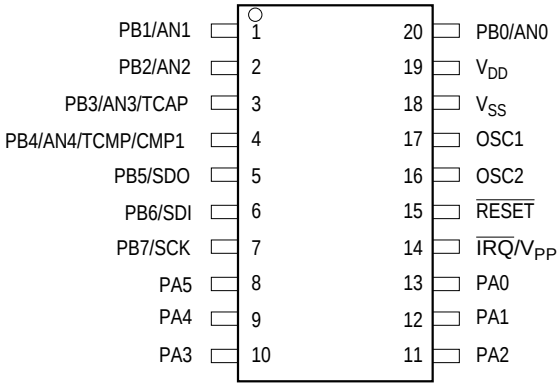


Figure 2. MC68HC705JJ7 Pinout

Block Diagrams

For reference throughout this application note, the block diagrams for the two parts are shown in **Figure 3** and **Figure 4**.

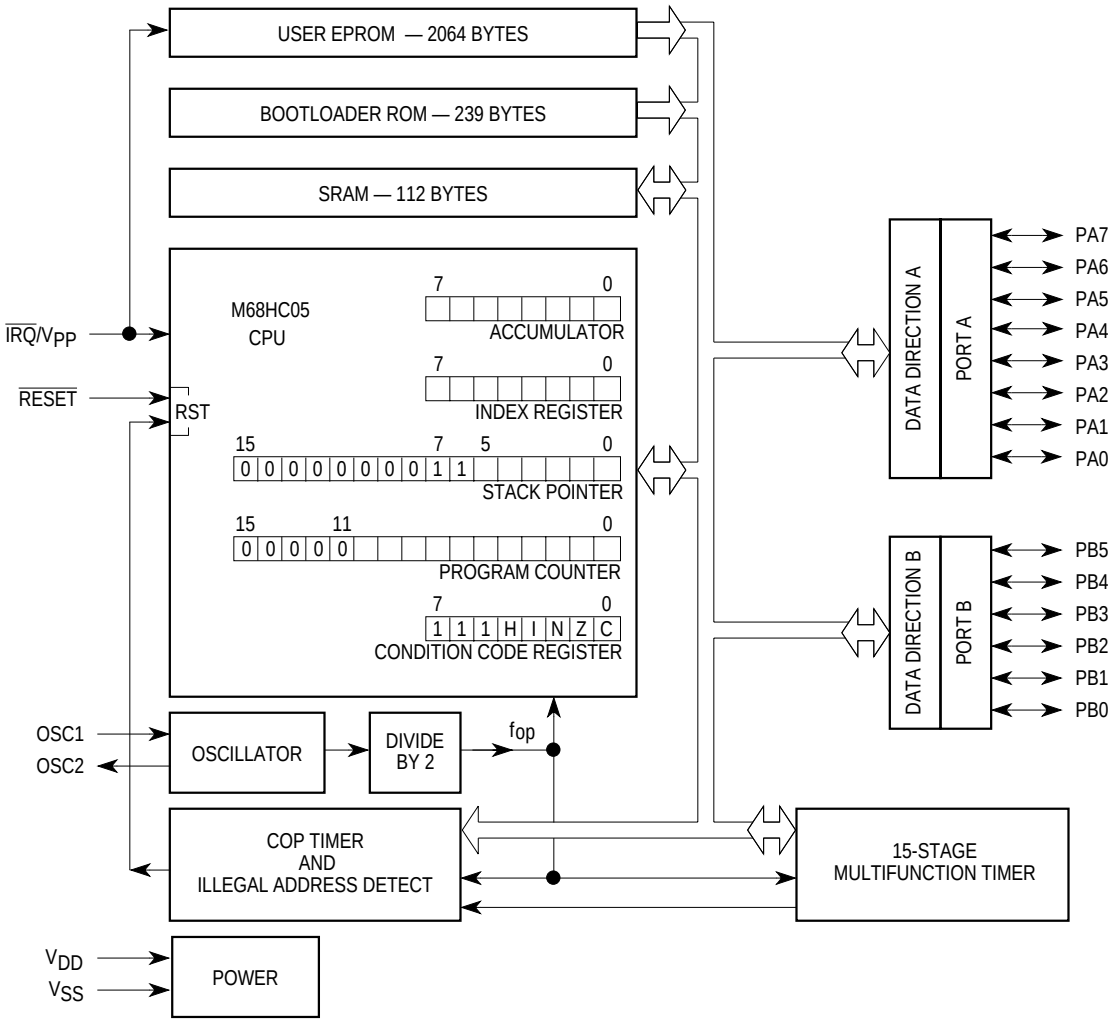
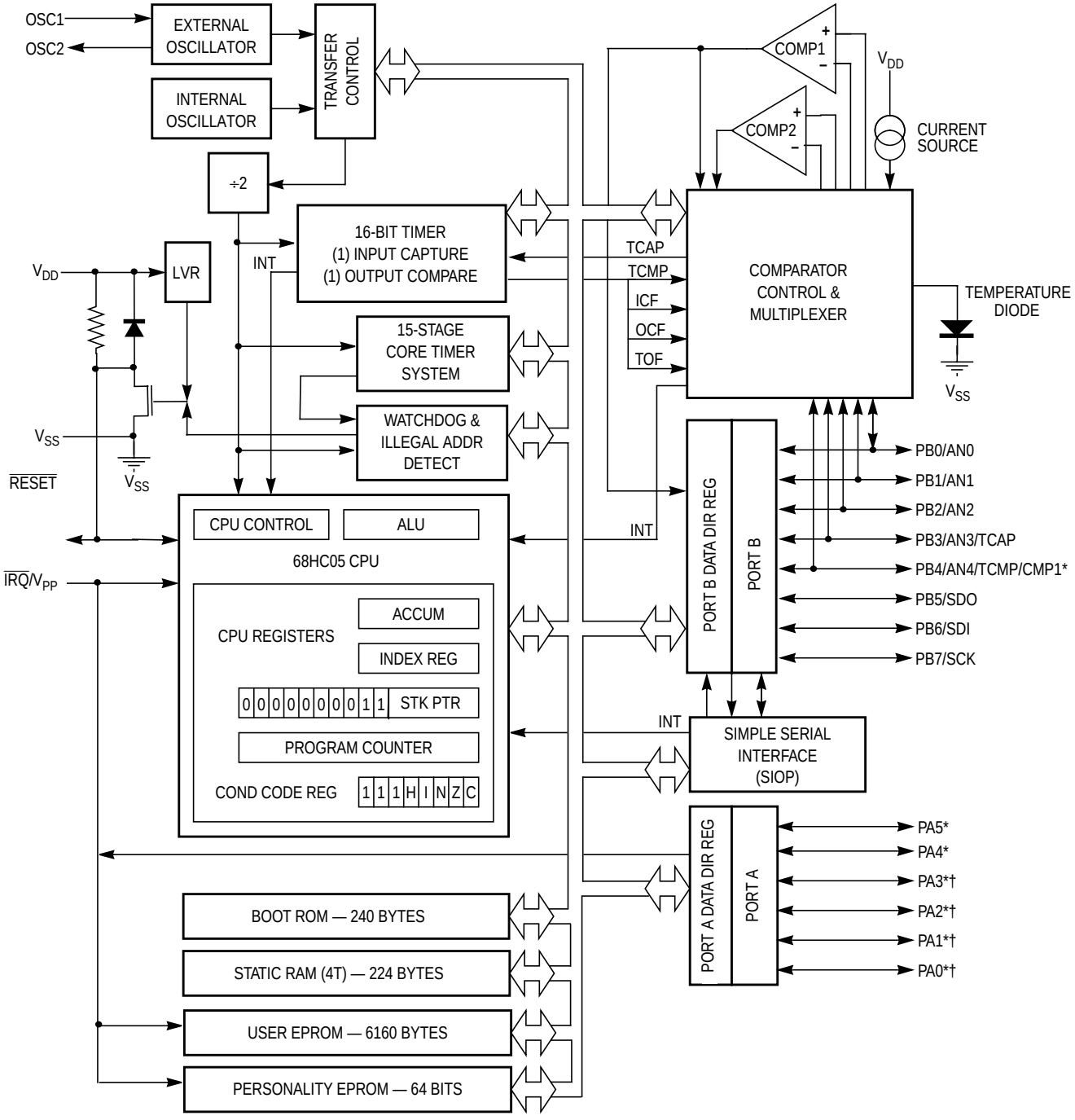


Figure 3. MC68HC705J2 Block Diagram



* High current sink/source capability
† Interrupt capability

Figure 4. MC68HC705JJ7 Block Diagram

Memory Maps and Registers

Figure 5 and Figure 6 show the memory maps and registers of the J2 and JJ7. Only the COP register and interrupt vectors have to be changed. The rest of the J2 memory can map directly to the JJ7.

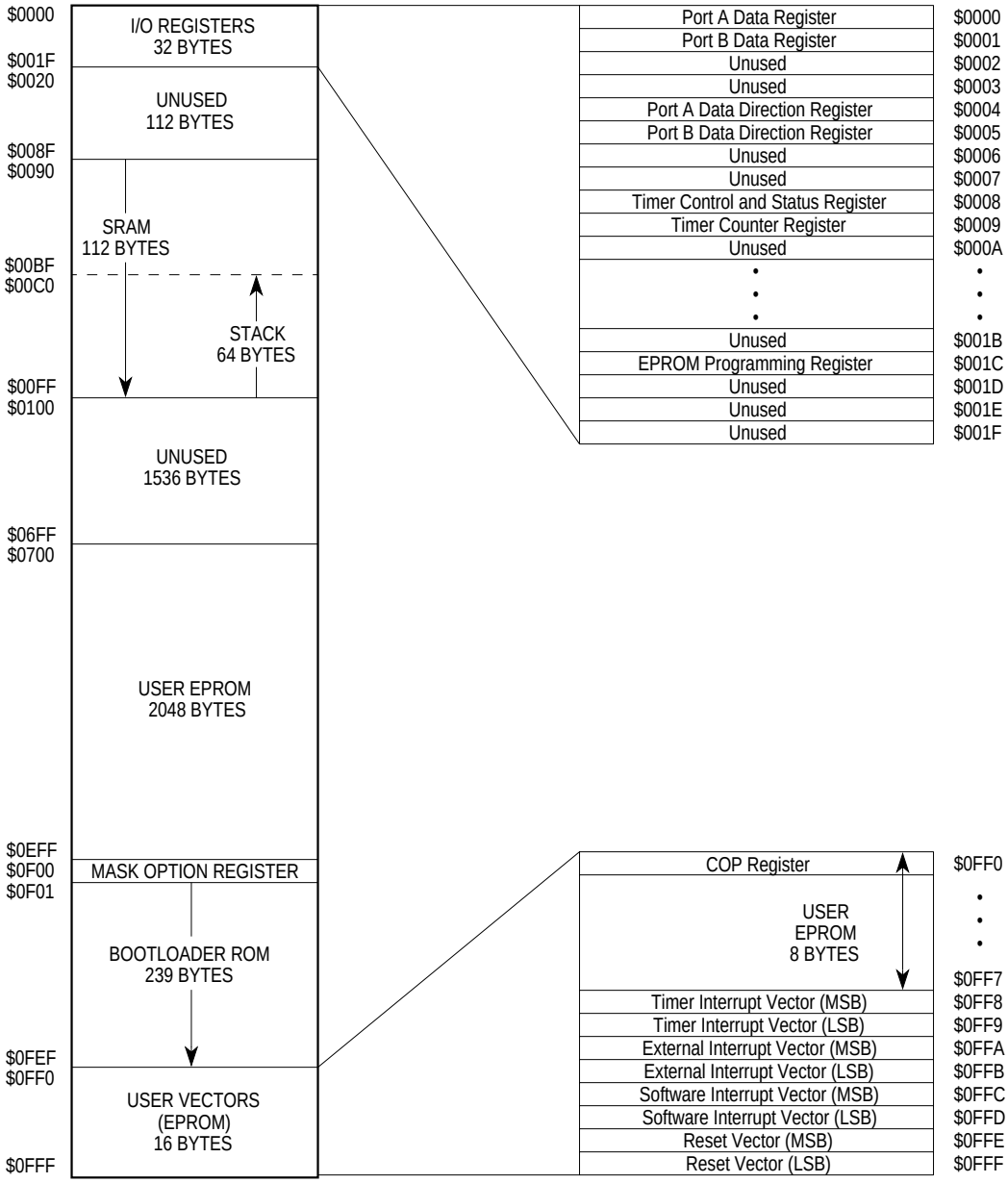


Figure 5. MC68HC705J2 Memory and Register Map

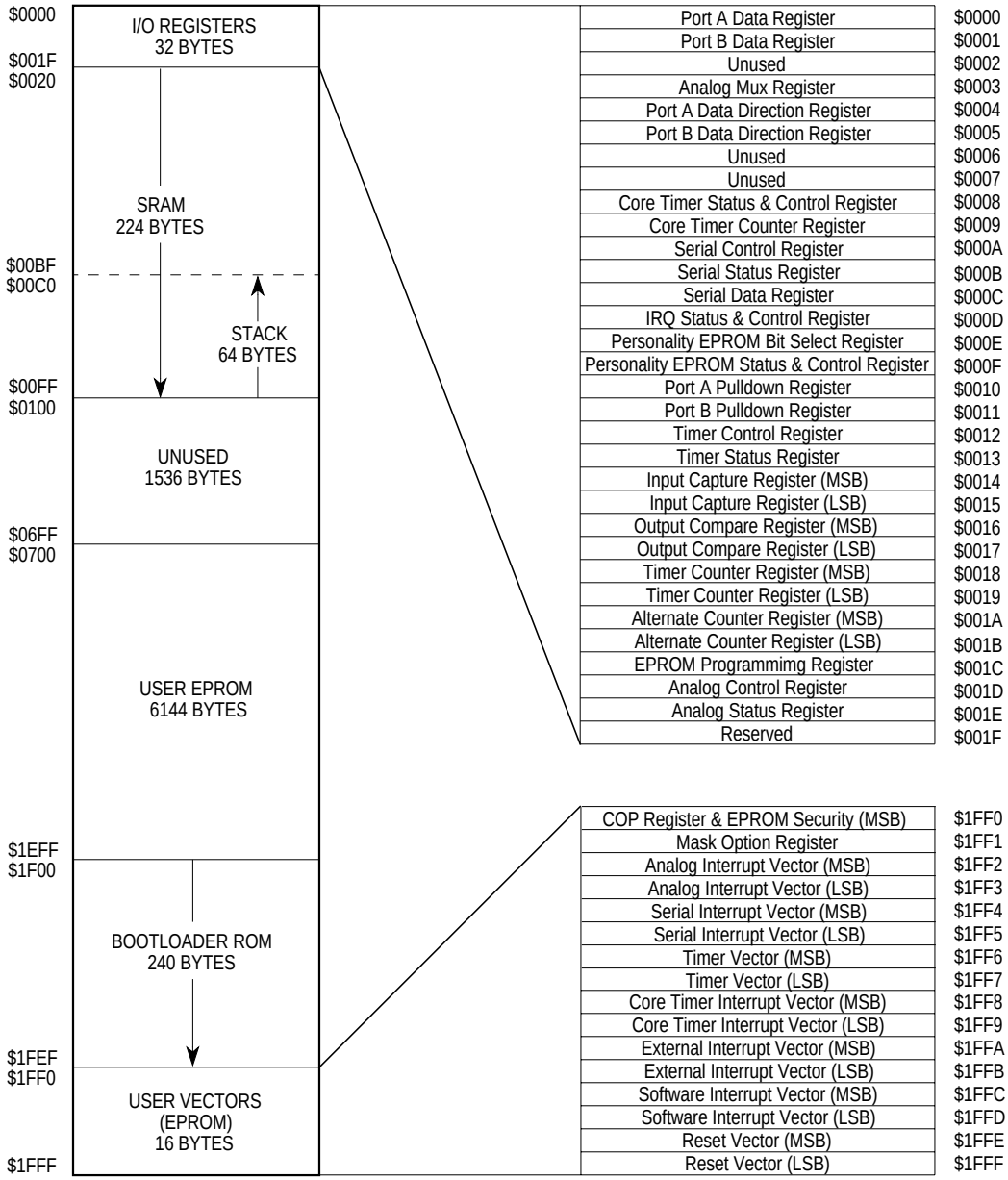


Figure 6. MC68HC705JJ7 Memory and Register Map

Port A and Port B

The J2 has port A configured as an 8-bit register and port B as a 6-bit register. The JJ7 has this configuration swapped, with port B being the 8-bit register and port A the 6-bit register. Change your code by mapping the data and data direction registers from A to B and B to A. The JJ7 registers are shown in **Figure 7** through **Figure 10**.

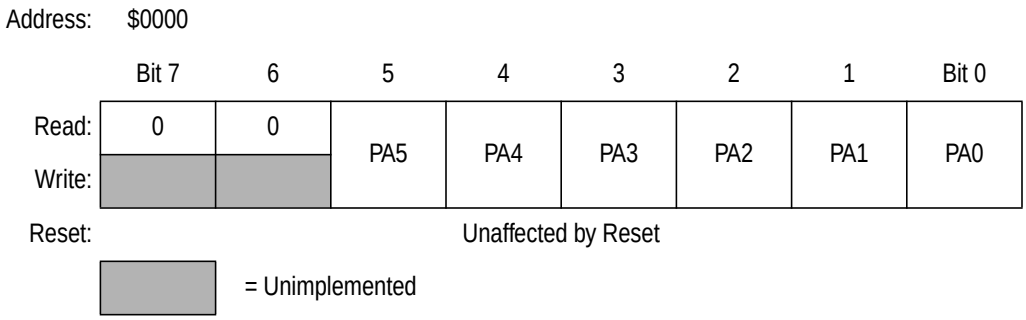


Figure 7. Port A Data Register (PORTA)

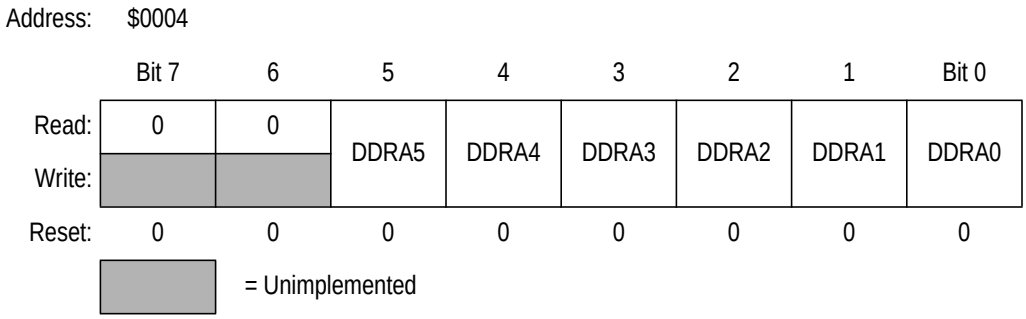


Figure 8. Data Direction Register A (DDRA)

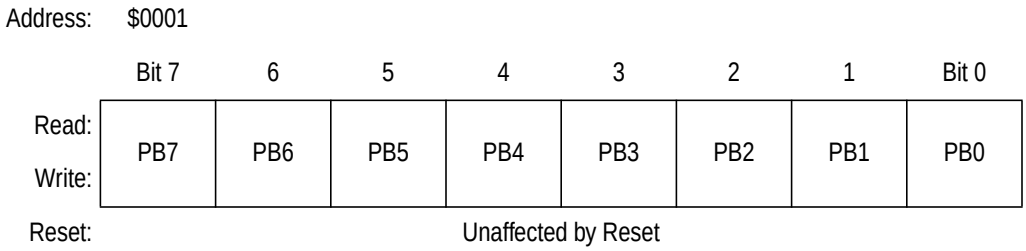


Figure 9. Port B Data Register (PORTB)

Address: $0005	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRA0
Reset:	0	0	0	0	0	0	0	0

Figure 10. Data Direction Register B (DDRB)

Clock

The JJ7 has the same external clock circuitry as the J2 as well as some additional features. Just like the J2, the JJ7 OSC1 and OSC2 pins can use either a crystal, ceramic oscillator, or external clock as a clock input.

The JJ7 has a low-power oscillator (LPO) in addition to its external pin oscillator (EPO). The LPO is the default oscillator out of reset. The LPO runs at either 100 kHz or 500 kHz. The default frequency is selected by the JJ7 part number. For proper chip selection, see **Table 3** in this application note.

To change from the LPO to the EPO, software has to be written. The oscillator is chosen by the OMx bits in the IRQ status and control register (ISCR) at location $000D. See **Figure 11**.

Address: $000D	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQE	OM2	OM1	0	IRQF	0	0	0
Write:				R			IRQR	
Reset:	1	1	0	0	0	0	U	0

= Unimplemented R = Reserved U = Unaffected

Figure 11. IRQ Status and Control Register (ISCR)

OM1 and OM2 — Oscillator selects

These bits control the selection and enabling of the oscillator source for the MCU. The choices are:

- The internal low-power oscillator (LPO)
- The external pin oscillator (EPO), which is common to most MC68HC05 MCU devices

The EPO uses external components – like filter capacitors and a crystal or ceramic resonator – and consumes more power. (The selection and enable conditions for these two oscillators are shown in **Table 1**.)

Table 1. Oscillator Selection

OM2	OM1	Oscillator selected by CPU	Internal low-power oscillator (LPO)	External pin oscillator (EPO)	Power consumption
x	0	Internal	Enabled	Disabled	Lowest
0	1	External	Disabled	Enabled	Normal
1	1	Internal	Enabled	Enabled	Normal

Therefore, the lowest power is consumed when OM1 is cleared. The state with both OM1 and OM2 set is provided so that the EPO can be started and allowed to stabilize while the LPO still clocks the MCU. The reset state is for OM1 to be cleared and OM2 to be set, which selects the LPO and disables the EPO.

To properly turn on the EPO, follow these steps:

1. Set OM1 = 1 and OM2 = 1. This will turn on the EPO while keeping the LPO on.
2. Wait for 1 ms to allow EPO to stabilize. This time may be longer or shorter, depending on the startup time for your oscillator circuit.
3. Set OM1 = 1 and OM2 = 0. This will turn off the LPO but keep the EPO running.

Code should be written at the beginning of the initialization routines for your application. This is a sample of the assembly code:

```
InitOSC     bset    5,$0D           ;OM2 = 1 & OM1 = 1 in ISCR
            lda     #16             ;load ACC w/16
OSCWait     deca                    ;loop takes approx 1 ms
            bne     OSCWait         ;with a 100-kHz LPO
            bclr    6,$0D           ;OM2 = 0 & OM1 = 1 in ISCR
                                    ;EPO is on, LPO is off
```

Reset

The $\overline{\text{RESET}}$ pin on the J2 is an input-only pin. The JJ7 $\overline{\text{RESET}}$ pin is bidirectional and has an internal pullup resistor and a steering diode.

Three events can cause an internal reset which in turn drives the $\overline{\text{RESET}}$ pin low:

- COP timeout
- Illegal address reset
- Low-voltage reset

Low-voltage reset is discussed later in this application note.

See **Figure 12** for the internal view of the JJ7's internal reset sources.

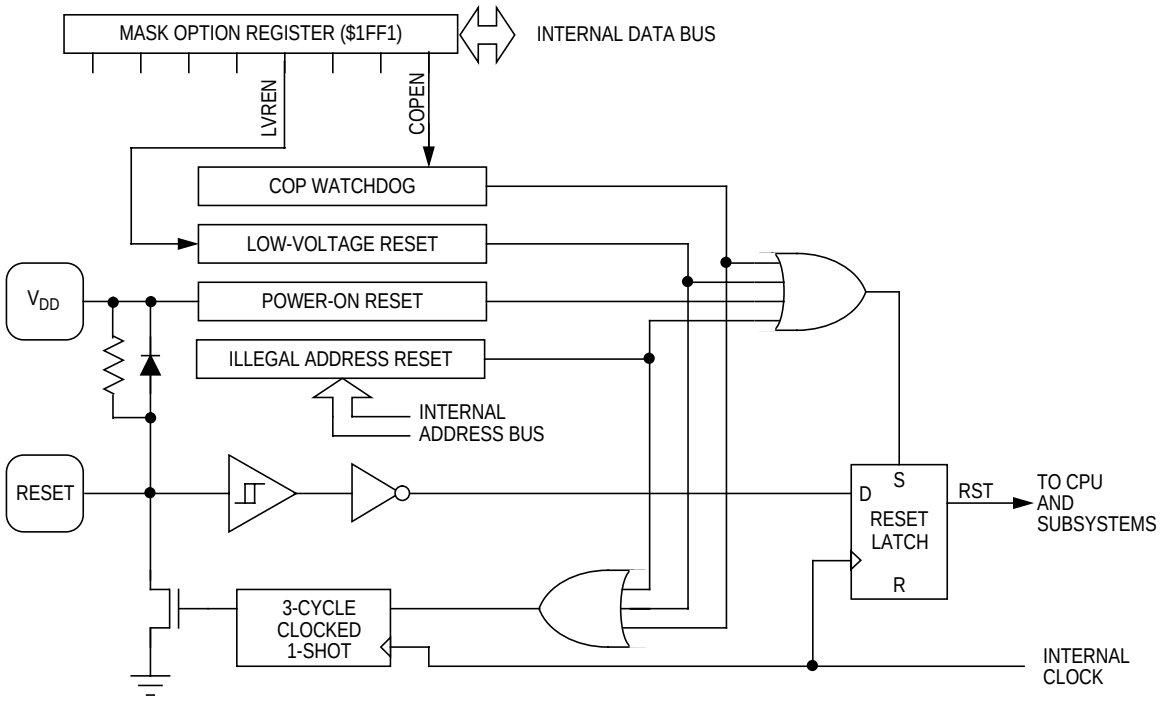


Figure 12. Reset Sources

Interrupts

To configure the external interrupt sensitivity, program the LEVEL bit (bit 1) of the MOR at location $1FF1. As with the J2, for edge-only detection, the bit should be 0. For edge- and low-level detection, program the bit to a 1.

The JJ7 has given the programmer more control over the interrupt function. Interrupts can be enabled and cleared by using the IRQ status and control register (ISCR). See **Figure 13**.

Address: $000D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQE	OM2	OM1	0	IRQF	0	0	0
Write:				R			IRQR	
Reset:	1	1	0	0	0	0	U	0

= Unimplemented R = Reserved U = Unaffected

Figure 13. IRQ Status and Control Register (ISCR)

IRQE — External interrupt request enable

This read/write bit enables external interrupts. Reset sets the IRQE bit.

1 = External interrupt processing enabled
0 = External interrupt processing disabled

IRQF — External interrupt request flag

The IRQ flag is a clearable, read-only bit that is set when an external interrupt request is pending. Writing to the IRQF bit has no effect. Reset clears the IRQF bit.

1 = Interrupt request pending
0 = No interrupt request pending

These conditions set the IRQ flag:

- An external interrupt signal on the $\overline{IRQ}/V_{PP}$ pin
- An external interrupt signal on pin PA0, PA1, PA2, or PA3 when the PA0–PA3 pins are enabled by the PIRQ bit in the MOR to serve as external interrupt sources.

These conditions clear the IRQ flag:

- When the CPU fetches the interrupt vector
- When a logic 1 is written to the IRQR bit

IRQR — Interrupt request reset

This write-only bit clears the IRQF flag bit and prevents redundant execution of interrupt routines. Writing a logic 1 to IRQR clears the IRQF. Writing a logic 0 to IRQR has no effect. IRQR always reads as a logic 0. Reset has no affect on IRQR.

1 = Clear IRQF flag bit
0 = No effect

To enable external interrupts, write a 1 to the IRQE bit. This is different than using an SEI instruction to set the I bit of the condition code register. The I bit allows the CPU to process interrupts for both external and internal requests. The IRQE bit is used to control external interrupts.

Write a 1 to the IRQR bit to clear any redundant external interrupt requests.

Timer

The JJ7 has two timers:

- Core timer
- 16-bit timer

The core timer is similar to the timer on the J2. Only a few changes were made to the core timer on the JJ7.

Both timers have their timer counter register (TCR) at location $09 and their timer control and status register (TCSR) at location $08. The JJ7's register is called the core timer status and control register (CTSCR). **Figure 14** and **Figure 15** are register diagrams for the two parts.

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	RTIF	TOIE	RTIE	0	0	RT1	RT0
Write:								
Reset:	0	0	0	0	0	0	1	1

= Unimplemented

Figure 14. J2 Timer Control and Status Register

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	CTOF	RTIF	CTOFE	RTIE	0	0	RT1	RT0
Write:					CTOFR	RTIFR		
Reset:	0	0	0	0	0	0	1	1

= Unimplemented

Figure 15. JJ7 Core Timer Status and Control Register

With the J2, the TOF (timer overflow flag) and the RTIF (real-time interrupt flag) bits are cleared by writing a 0 to the TOF and RTIF bits.

The JJ7 uses bit 3 and bit 2 in the CTSCR to clear the CTOF and the RTIF flags. Change your code to reflect the following.

CTOFR — Core timer overflow flag reset

Writing a logic 1 to this write-only bit clears the CTOF bit. CTOFR always reads as a logic 0. Reset does not affect CTOFR.

1 = Clear CTOF flag bit
0 = No effect on CTOF flag bit

RTIFR — Real-time interrupt flag reset

Writing a logic 1 to this write-only bit clears the RTIF bit. RTIFR always reads as a logic 0. Reset does not affect RTIFR.

1 = Clear RTIF flag bit
0 = No effect on RTIF flag bit

COP

The J2's COP (computer operating properly) is enabled by programming the COP bit (bit 0) of the mask option register (MOR) at location $0FF0 to a 1. On the JJ7, program the COPEN bit (bit 0) of the MOR at location $1FF1 to a 1.

The J2's COP timer is cleared by writing a 0 to bit 0 of the COPR (computer operating properly register). On the J2, the COPR is located at $0FF0.

To clear the JJ7's COP, use the same clearing procedure you used on the J2, but change your code to write a 0 to bit 0 of the COPR at location $1FF0 instead of $0FF0.

Just like the J2, the JJ7 COP timeout is set by RT1 and RT0 of the core timer status and control register. No code changes are needed.

Utilizing the JJ7 Features

The extra features found on the JJ7 can be used to lower overall system costs as well as to provide additional value to your microcontroller design. The major benefits are described here. For further reference, consult the *68HC705JJ7 General Release Specification*, Freescale document order number HC705JJ7/D.

Expandability

If your system is I/O (input/output) constrained and needs additional port pins, the JJ7 can be upgraded to the MC68HC705JP7 (JP7). The JP7 has the same memory and feature set as the JJ7 but with an additional eight I/O pins. These eight port pins constitute port C and are high sink/source current pins. The JP7 comes in a 28-pin package, and the pinout is shown in **Figure 16**.

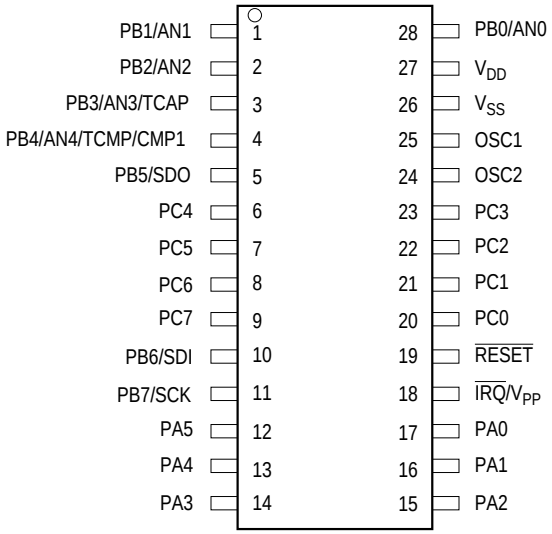


Figure 16. MC68HC705JP7 Pinout

Timers

The JJ7 has a programmable timer in addition to the core timer. The programmable timer has a 16-bit timer with an input capture function and an output compare function. If those functions are utilized, port B bit 3 becomes the input capture pin and port B bit 4 becomes the output compare pin.

The basis of the capture/compare timer is a 16-bit free-running counter which increases in count with every four internal bus clock cycles. The counter is the timing reference for the input capture and output compare functions. The input capture and output compare functions provide a means to latch the times at which external events occur, to measure input waveforms, and to generate output waveforms and timing delays. Software can read the value in the 16-bit free-running counter at any time without affecting the counter sequence.

Memory

The JJ7 has considerable more memory than the J2. Besides having 6160 bytes of EPROM and 224 bytes of RAM, the JJ7 also has 64 bits of personality EPROM (PEPROM). The PEPROM is arranged internally as an 8 x 8 matrix of bits.

PEPROM can be used to give a product an identification code or a serial number. It can be programmed by the user's code or at the time of production, thus making it easy to store calibration data if needed.

Simple Serial I/O Port

The simple synchronous serial I/O port (SIOP) subsystem is designed to provide efficient serial communications with other MCUs.

SIOP is implemented as a 3-wire master/slave system with serial clock (SCK), serial data input (SDI), and serial data output (SDO). When the SIOP is enabled, the port B I/O pins 5, 6, and 7 are bypassed and used by the SIOP.

Although not as flexible as the serial peripheral interface (SPI) bus found on other Freeescale microcontrollers, the SIOP can work with the most popular MCU peripherals, including:

- Analog-to-digital converters
- Digital-to-analog converters
- Serial EEPROM devices
- Time-keeping peripherals
- Digital potentiometers

Analog Subsystem

The analog subsystem of the JJ7 is based on two on-chip voltage comparators and a selectable current charge/discharge function as shown in **Figure 17**.

This configuration provides several features:

- Two independent voltage comparators with external access to both inverting and non-inverting inputs
- One voltage comparator can be connected as a single-slope A/D and the other can be connected as a single-voltage comparator.
- The possible single-slope A/D connection provides these features:
  - A/D conversions can use V_{DD} or an external voltage as a reference with software used to calculate ratiometric or absolute results.
  - Channel access of up to four inputs via multiplexer control with independent multiplexer control allowing mixed input connections
  - Access to V_{DD} and V_{SS} for calibration
  - Divide by 2 to extend input voltage range
  - Each comparator can be inverted to calculate input offsets
  - Internal sample and hold capacitor
  - Direct digital output of comparator 1 to the PB4 pin

High Current Pins

The JJ7 and the JP7 I/O pins have high current capabilities that allow them to source or sink current to a device. Depending on the current requirements, these pins can be used to switch power to other parts of the system, light LEDs (light-emitting diodes), or switch optically coupled triacs without external transistors. **Table 2** shows the maximum ratings for the I/O pins.

Table 2. I/O Maximum Current Specifications

Characteristic	Symbol	Max	Unit
High source current Total for all six PA0:PA5 pins and PB4 Total for all eight PC0:PC7 pins (JP7)	I_{OH}	 20 30	mA
High sink current Total for all six PA0:PA5 pins and PB4 Total for all eight PC0:PC7 pins (JP7)	I_{OL}	 40 60	mA

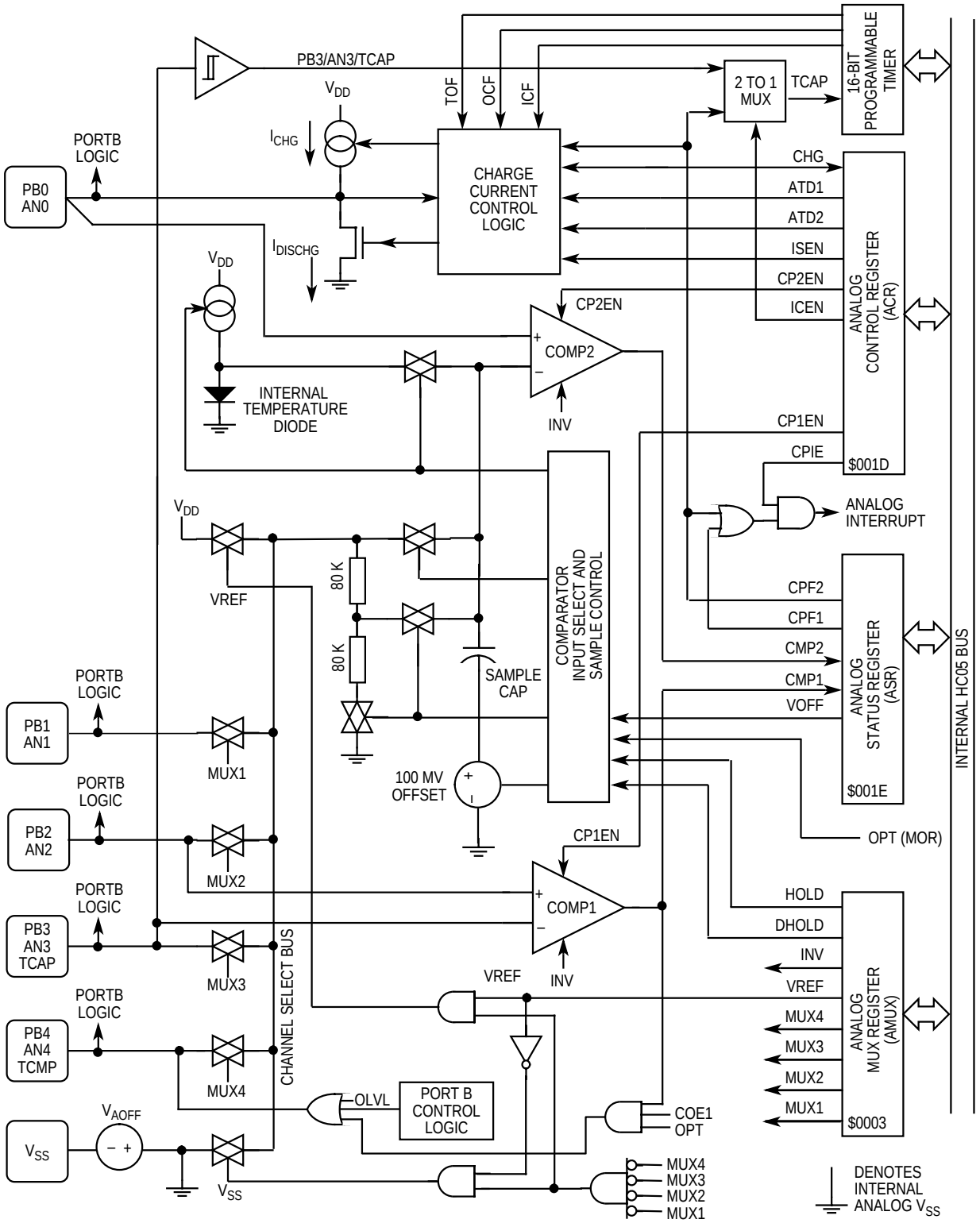


Figure 17. Analog Subsystem Block Diagram

Programmable Pulldowns

All I/O pins have software programmable pulldown devices which can be enabled or disabled globally by the SWPDI bit in the JJ7's MOR. Tying unused input pins to ground decreases digital noise and current consumption often caused by a floating input.

Port Interrupt Capability

Four port pins, PA0 to PA3, can be configured to serve as additional interrupt sources. Combined with the programmable pulldown resistors, this option allows for easy implementation of scanning a matrix of keypad buttons.

Enhanced Oscillator

As mentioned earlier, the oscillator circuitry has a low-power oscillator (LPO) that runs at either 100 kHz or 500 kHz, depending on the part number. This oscillator is the default oscillator out of reset and can be turned on or off.

Also, for crystal and ceramic resonator circuits, a feedback resistor can be selected internally to the chip.

In addition to a crystal, ceramic resonator or external clock source, an RC oscillator also can be used for an economical clock solution. The RC oscillator is chosen by proper part ordering.

EPROM Security

To protect your software investment, the JJ7 has a security option that locks out unwanted access to the program code. An EPROM programmable bit is provided at location $1FF0, bit 7 of the COP register. This bit allows control of access to the EPROM array. Any accesses to the EPROM locations will return undefined results when the security bit is set.

On-Chip Temperature Diode

An internal diode located in the analog subsystem is forward biased to V_{SS} and will have its voltage change approximately 2 mV for each degree centigrade rise in the temperature of the device. The diode can be selected by software to be connected to comparator 2. Single slope analog-to-digital conversion is then used to derive the temperature.

Low-Voltage Reset

For added system reliability, the JJ7 has a low-voltage reset (LVR) function. When the JJ7 drops below its specified operating voltage range, the LVR is asserted and the part goes into reset. Once the LVR circuitry establishes that the operating voltage is within specification, the LVR is released and the part continues to run out of reset. This function is selectable via the MOR.

The JJ7 also adds an internal pullup resistor and a steering diode to the internal reset circuitry of the chip. Refer to the JJ7 block diagram in **Figure 4**.

System Enhancements

The STOP instruction's function can be changed by a bit in the MOR register to act more like a WAIT instruction. When this feature is used, a STOP instruction puts the MCU in halt mode. Halt mode is a wait-like, low-power state. The internal oscillator and timer clock continue to run, but the CPU clock stops. In this state, the COP watchdog will not be turned off.

When this feature is not used, the STOP instruction will stop the internal oscillator, the internal clock, the CPU clock, the timer clock and the COP watchdog timer.

For faster startup after reset, the programmer can select a shorter delay out of reset. A bit in the MOR register determines whether the delay after reset is 4064 bus cycles or 16 bus cycles.

Ordering Information

Table 3 shows the MC order numbers for the JJ7. All parts are specified to run at –40 to 85 °C temperature.

Table 3. Ordering Information

Package type	EPO oscillator type	LPO frequency (kHz)	Order number
Plastic DIP	XTAL	100	MC68HC705JJ7CP
SOIC	XTAL	100	MC68HC705JJ7CDW
CERDIP	XTAL	100	MC68HC705JJ7CS
Plastic DIP	RC	100	MC68HRC705JJ7CP
SOIC	RC	100	MC68HRC705JJ7CDW
CERDIP	RC	100	MC68HRC705JJ7CS
Plastic DIP	XTAL	500	MC68HC705SJ7CP
SOIC	XTAL	500	MC68HC705SJ7CDW
CERDIP	XTAL	500	MC68HC705SJ7CS
Plastic DIP	RC	500	MC68HRC705SJ7CP
SOIC	RC	500	MC68HRC705SJ7CDW
CERDIP	RC	500	MC68HRC705SJ7CS

References/Additional Reading

MC68HC705J2 Technical Data, Freescale document order number MC68HC705J2/D,

MC68HC705JJ7 General Release Specification, Freescale document order number HC705JJ7GRS/D,

Application Note

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