

Application Note

Using the SDRAM Controller on the MCF5307 ColdFire® Integrated Microprocessor

INTRODUCTION

There's a new type of memory that's becoming very popular in systems designs. It's called synchronous DRAM (SDRAM), and it specifically supports the high-speed bus designs required to fully utilize current high-performance microprocessors. The MCF5307 ColdFire® integrated microprocessor is the first of the ColdFire Family to contain the Version 3 clock-doubled core. The MCF5307 SDRAM controller can interface with over 2,000 MBytes of DRAM and supports bursting and page-mode operations. In addition, the SDRAM controller can connect to both extended-data-out DRAMs and synchronous DRAMs.

Running synchronously with the system clock rather than responding to traditional asynchronous control signals, SDRAM can (after an initial latency period) be read or written on every clock cycle. A 5-1-1-1 burst rate is typical at 100 MHz. To support interleaving, many SDRAM devices contain multiple banks and all banks can have an open page at any time.

DRAMs use a multiplexed address bus in which the processor provides the address in two cycles. The most significant portion of the address is transmitted first (the row), followed by the lower

portion (the column). Gated by the system clock, the row and column are latched by the DRAM and together form the complete address required to identify the requested data. The multiplexing reduces the pin count of the packages as well as the number of pad connections on the chip, and so lowers the memory cost. The trade-off for this pin count and memory reduction is slower performance because it mandates an additional cycle to transmit the address. Memory designers have developed new interfaces to reduce the impact of this trade-off. One example is page-mode operation. Page mode sends the row address portion only once for multiple accesses within a memory region (a page). The newest concept is SDRAM, which can accept new column addresses on every system clock cycle and, after an initial pipeline latency period, deliver or receive data at the same rate.

SDRAM controllers require a higher level of sophistication than asynchronous DRAM controllers. Not only must addresses and data be managed, but SDRAM chips also need special "commands" to be sent from the controller to initialize the memory as well as to instruct the memory which operations are to occur. These commands include instructions to precharge, read, write, burst, auto-refresh, and various

combinations of these functions. A good controller is necessary to unburden the CPU from the overhead of these tasks. The MCF5307 ColdFire microprocessor's synchronous/asynchronous DRAM controller (SADRAMC) performs these functions for a variety of DRAMs through the use of internal configuration registers. These registers let programmers set up the controller according to specific memory system requirements.

SDRAMs operate in a different fashion than asynchronous DRAMs. The use of commands to initiate special actions is particularly unique, as is the use of data pipelines. Commands are issued to memory by using specific encoding on the address and control pins. One of the first operations after a system reset must be to configure the SDRAM operating parameters by issuing a command to the SDRAM mode register. Using the MCF5307 SADRAMC, this can only be accomplished after setting up the MCF5307 SDRAM Controller Control Register (DCR), the DRAM Address and Control Register(s) (DACRx) and the DRAM Mask Register(s) (DAMRx) appropriately. These registers set the address space and operating parameters for the controller. Once the MCF5307 DRAM controller is set up, it's time to begin the initialization sequence for the SDRAM itself.

First, a "Precharge All" (PALL) command is sent to the SDRAM. To do this, write a "1" to the IP bit (bit 3) in the DACRx register and access any memory space in the preferred SDRAM bank. Next, enable refresh by writing a "1" to the RE bit of DACR0 and DACR1 and then wait until at least eight refresh cycles have occurred. At this time, the Mode Register Set (MRS) command can be issued. Writing to the mode register simply involves setting the IMRS bit in the DACRx registers and then writing to the SDRAM. Use an address that contains the proper information on its lower bits and also has the upper address bits set so that the access

falls in the established SDRAM space as previously programmed into the DACRx and DMRx registers. This step is further detailed in Example 1.

MCF5307 SADRAMC SIGNALS

The MCF5307 SADRAMC interfaces to SDRAMs through the use of the following signals:

Synchronous Row Address Strobe ($\overline{\text{SRAS}}$) indicates a valid row address is present and can be latched by the SDRAM.

Synchronous Column Address Strobe ($\overline{\text{SCAS}}$) indicates a valid column address is present and can be latched by the SDRAM.

DRAM Read/Write ($\overline{\text{DRAMW}}$) is asserted (active-low) when a write operation is to be performed. It will be negated (high) for read operations.

Synchronous DRAM Clock Enable (SCKE). This active-high output is registered to route directly to the CKE (clock enable) signal of external DRAMs when the MCF5307 SDRAM controller is operating in synchronous mode. The CKE signal enables or disables the clock internal to the memory chips. When CKE is low, the memory can go into a power-down mode. Operations can be suspended, or the memories can enter self-refresh mode.

Clock Output (called BCLKO on the MCF5307) connects to the CLK input on SDRAMs. BCLKO represents the bus clock, and as such is not unique to the SDRAM controller but can be used for other purposes throughout the system as well.

Another signal included in the SDRAM controller is the EDGESEL, which can provide extra hold time for the signals to the memory. This signal can monitor the clock at the input to the SDRAM, and cause data, address, and

control outputs to remain active for an additional time after BCLKO transitions. A more detailed explanation is provided in the *MCF5307 User's Manual*.

Additionally, the $\overline{CAS}[3:0]$ signals serve as output qualifiers or masks to select specific bytes. These are referred to on the SDRAM as “mask qualifiers,” or \overline{DQM} signals. The timing for these is fixed by the design of industry-standard SDRAMS and is not programmable. When reading from SDRAM, the \overline{DQM} lines must be valid two clocks prior to the availability of the data to which they apply. When writing to SDRAM, the \overline{DQM} signals will be valid coincidentally with the data being written. $\overline{CAS0}$ affects the least significant byte while $\overline{CAS3}$ operates on the most significant byte.

Finally, $\overline{RAS}[1:0]$ on the MCF5307 are used to enable either of the two SDRAM banks that the controller can support. They are typically connected to chip-select pins on the SDRAM.

GENERAL OPERATION

The controller on the MCF5307 manages the interface to the SDRAM subsystem through the control signals \overline{RAS} , \overline{CAS} , and \overline{DRAMW} as well as multiplexing the address signals. The controller also provides termination of the access cycle. The exact operation of these signals is set by the configuration of the on-chip control registers and is explained in the user's manual, so it will not be repeated here. However, the physical connection from the MCF5307 to a particular SDRAM chip will vary depending on the exact memory device chosen, and the first order of business is to determine how the address signals should be routed to the memory.

This Application Note includes two examples; however, first it is worthwhile to examine the generic address connection scheme used in the SDRAMC. The following table shows the physical connections needed to operate 8-, 16-, and 32-bit-wide memory systems. Note that this

table is described as the “generic” connection scheme. That is because it is completely applicable only for symmetrical memory devices. For memory chips that have unequal numbers of row and column addresses some adjustments are needed. Both of the examples included herein will further illustrate this statement. Additional information is presented in the Special Considerations section at the end of this document.

GENERIC ADDRESS CONNECTION SCHEME

MCF5307	SDRAM ROW	SDRAM COLUMN	NOTES RELATING TO PORT SIZES
17	17	0	8-bit port only
16	16	1	8- and 16-bit ports
15	15	2	
14	14	3	
13	13	4	
12	12	5	
11	11	6	
10	10	7	
9	9	8	
17	17	16	32-bit port only*
18	18	17	16-bit port only*
19	19	18	
20	20	19	
21	21	20	
22	22	21	
23	23	22	
24	24	23	
25	25	24	

*See *Asymmetrical Memory Devices* in the Special Considerations section at the end of this document.

This table details the row and column address signals driven by the physical address pins on

the MCF5307. Some differences exist for each of the three possible port sizes. Note that only 8-bit ports use an A0 address from the MCF5307. Because 16- and 32-bit ports will issue either words or longwords when accessed, they do not use the MCF5307 A0 signal. Likewise, the configuration for 32-bit ports uses neither A0 nor A1. This presents a slight problem as SDRAM address signal A0 is issued on physical pin A17 of the MCF5307 along with SDRAM address signal A17. While A0 is not used for the larger ports, A17 is still needed. The MCF5307 SDRAM controller provides for this by changing the column address that appears on physical pin A17 of the processor whenever an 8-bit port is not selected. This is determined by the settings of the Port Size bits (bits 4 and 5) in the MCF5307 SDRAMC DACRx registers. For 8-bit ports, MCF5307 physical pin A17 will drive logical address A0 during the $\overline{\text{CAS}}$ cycle. When 16- or 32-bit ports sizes are programmed, the $\overline{\text{CAS}}$ cycle of pin A17 will drive logical address A16, as indicated in the generic address connection scheme table identify which physical pins of the MCF5307 are used for various port sizes.

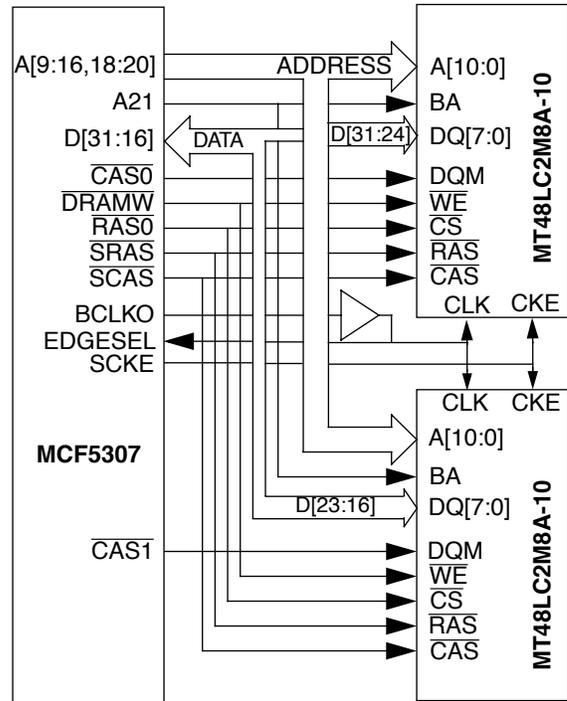
While the Generic Address Connection Scheme table only lists physical MCF5307 pins from 17 to 25, in fact SDRAM row addresses will appear on pins all the way up to pin A31 on the MCF5307. Column addresses however, are limited to the pins shown (A17 to A25). This permits the use of larger memories in the future.

EXAMPLE 1:

**MICRON TECHNOLOGY
MT48LC2M8A-10**

This part is rated for bus speeds of up to 66 MHz. The CAS latency is 2 clocks (9 ns) with 3 ns setup and 1 ns hold times. It is organized as 1 MByte X 8-bits X 2 banks. For this example, assume a 16-bit- wide port using two memory chips. This will give 2 megawords of SDRAM.

Complete data sheets for this and other Micron memory devices can be found at <http://www.micron.com/mti/msp/html/datasheet.html>



MCF5307 Bank 0 configured as 2M Words X 16 bits

Connecting the physical address lines.

To create a 16-bit port with a depth of 2 megawords, 21 address signals are needed. That is, the address range would be from zero to 0x1FFFFFF. These are made up of 11 row addresses, 9 column addresses, and one bank select line. Because the access width is 16 bits, A0 is not used (bytes are not individually accessed via the address lines). Starting with A1, which is physically on pin A16 of the MCF5307, the combined number of address lines needed to access 2 megawords is 21. The row/column muxing by the MCF5307 SDRAMC would therefore look like this:

EXAMPLE 1: ADDRESS PIN CONNECTIONS .

SDRAM	MCF5307	SDRAM ROW	SDRAM COLUMN
A0	A16	A16	A01

SDRAM	MCF5307	SDRAM ROW	SDRAM COLUMN
A1	A15	A15	A02
A2	A14	A14	A03
A3	A13	A13	A04
A4	A12	A12	A05
A5	A11	A11	A06
A6	A10	A10	A07
A7	A09	A09	A08
A8	A18	A18	A17
A9	A19	A19	
A10	A20	A20	
BA	A21	BA	

This row/column muxing provides the necessary 21 address signals (21:01) to access the 16-bit-wide port. As mentioned earlier, address signal A0 is not used. Notice that MCF5307 address signal A17 was skipped. The generic connection table identifies this as used only for 8- or 32-bit ports. When the SDRAMC is configured for 8-bit ports, pin A17 drives row address A17 and column address A0. For 32-bit ports pin A17 on the MCF5307 drives row address A17 and column address A16. Because this example is based on a 16-bit port, MCF5307 physical address pin A16 is used to supply address signal A16 as a column address, along with row address A1. The MCF5307 pin A17 is therefore not used in favor of the next pin, which is A18. This pin (A18) supplies the missing address signal A17 as a row address, and also continues the addressing sequence by providing SDRAM address A18. Because all SDRAM column addresses have now been accounted for, the final task is to connect additional pins to provide the remaining row addresses. The MCF5307 address pins A19 and A20 are used for this task, along with A21 as the SDRAM Bank Select signal.

SDRAM INITIALIZATION

The physical connections between the processor and the SDRAM are established. Before the memory can be used however, it must be initialized. After power is applied to the memory and the clock is running and stable, a 100 μsec delay is required before the SDRAM accepts commands. During this time, the MCF5307 DCR, DACRx, and DCMRx registers can be initialized (but do not enable refresh at this time).

The DRAM Control Register (DCR) in this example should be loaded with the value 0x822B. This value sets the controller to synchronous operation, enables address multiplexing, and programs the SCKE pin to be clock enable. This value also doesn't initiate refresh. Refresh timing (required delay following the issue of a refresh command before an activate command can be given) is set for 6 bus clocks. This is determined by the t_{RC} spec of the SDRAM. Finally, the Refresh Count (RC) field is loaded with the value 0x2B (decimal 43). This value programs the frequency of refresh operations. To determine the correct RC field value, divide the number of bus clocks allowed between refreshes by 16. This result minus one gives the number to load into the RC field. The Micron SDRAM spec states a maximum time period for refresh commands of 15.5 μsec. This equates to 697.5 bus clocks at 45 MHz. To convert this to a RC field value, perform these calculations:

$$\begin{aligned} \# \text{ of bus clocks} &= (\text{RC Field} + 1) * 16 \\ 697.5 \text{ bus clocks} &= (\text{RC Field} + 1) * 16 \\ 697.5/16 &= (\text{RC Field} + 1) \\ (697.5/16) - 1 &= \text{RC Field} \\ 42.6 &= \text{RC Field} \end{aligned}$$

This result indicates the maximum delay between refreshes. A value of 42 decimal should be used (2A hexadecimal).

Before issuing any commands to the SDRAM, load appropriate values into the DACRx and DCMRx registers to establish the preferred location in the system memory map for the SDRAM. Again, do not initiate refresh yet.

After this step and the necessary 100 μ sec delay has been completed, issue a “precharge all” (PALL) command by setting the IP bit (bit 3) in the DACRx register to a one, and then accessing any memory location in the associated SDRAM. Next, enable refresh by setting the RE bit in the MCF5307 DACRx register (bit 15) to a one. The Micron Technology data sheet specifies a 30 ns delay following the PALL command to allow the banks to precharge. This operation places the SDRAM in the idle state. After observing the appropriate delay (this is a good time to set up other peripherals on the MCF5307) to allow the memory to enter the idle state, issue two AUTO REFRESH commands. After these commands are finished, you can program the SDRAM mode register, and normal memory operation can begin.

WRITE BURST MODE							BURST TYPE				
BA	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
11	10	9	8	7	6	5	4	3	2	1	0
RESRV		WB	OP MODE		CAS LATENCY			BT	BURST LENGTH		

MT48LC2M8A1TG-10 Mode Register

Issuing commands to SDRAM involves a little bit of planning. Because commands are issued via the address lines, commands are dispatched simply by accessing a specific address in the SDRAM address range that corresponds to the desired bit pattern for the command being given. For instance, to set the mode register in the Micron Technology MT48LC2M8A-10 SDRAM memory chip, the first order of business is to determine what information to send. The mode register on the SDRAM has 12 bits. Bits 0-2 determine the burst length. Bit 3 identifies the burst type. Bits 4-6 set the CAS

latency, while bits 7-8 define the mode of operation. Bit 9 establishes the write burst mode, while bits 10-11 are reserved and should be programmed with zeroes. A mode register setting of (binary) 0010 0010 0000 (hex equivalent 0x220) causes the SDRAM to operate in the following manner:

- Burst Length = 1
- Burst Type = Sequential
- CAS Latency = 2 Clocks
- Operating Mode = Standard Operation
- Write Burst Mode = Single Location Access

Before the SDRAM mode register can be programmed, we must first go back and examine the physical pin connections. The SDRAM will take the values presented to its’ address lines during the mode register load and transfer them into the mode register. The MCF5307 user’s manual states that the address lines are not multiplexed during this operation. Furthermore, because the port size is 16 bits in this example some physical pins are not used on the MCF5307. This must also be taken into consideration. To program the SDRAM mode register with a hex value of 0x220, look at these connections to determine how the individual bits must be routed to the SDRAM. Because the SDRAM controller does not multiplex the address lines while loading the SDRAM mode register, the individual bits must be placed appropriately. To write a value of 0x220 to the SDRAM address lines, a logic one must be presented to SDRAM pins A5 and A9 while the other pins are held at logic zero. Therefore the MCF5307 should access location 0xnn08 0800. This causes MCF5307 address pins A11 and A19 to be high. These are physically connected to SDRAM pins A5 and A9, which correspond to the bits in the SDRAM mode register we wish to set. The data driven will be ignored.

To program this information into the SDRAM mode register, set the IMRS bit (bit 6) to a “1” in the DRAM Address and Control register of the MCF5307 SDRAMC, and immediately issue a

write to address 0xnn08 0800 where the upper address bits “nn” are selected to force the access to occur in SDRAM space (as previously established by initializing the DACRx and DCMRx registers). The lower portion of the address is the value selected to cause proper programming of the SDRAM mode register. The MCF5307 SDRAMC will then run a command cycle and load the SDRAM mode register with the proper pattern.

In some instances the address used to program the SDRAM mode register may fall outside of the memory map for the SDRAM. When this happens, the write cycle to program the mode register will not cause an SDRAM access to occur, and the register will not be programmed. In this case the base address of the SDRAM must be temporarily changed via the DACRx and DMRx registers to force the required address to hit in the SDRAM space. After the mode register is successfully programmed, the base address may be set to its desired value.

EXAMPLE 2

TEXAS INSTRUMENTS TMS664814-10

The TI part can also operate on a 66 MHz bus, so it will easily satisfy the 45 MHz bus timing requirements of the MCF5307. It is organized as 2 MBytes X 8-bits in each of four banks. Fourteen address pins (named A13-A0)—nine of which are multiplexed with column addresses—provide the addressing capability. Address pins A12 and A13 are used as the bank-select pins. For this example, assume a 32-bit-wide port using four memory chips. This will give 8M longwords of SDRAM, or 32 MBytes. It is an important concept to distinguish between the two physical banks supported by the MCF5307 SDRAM controller and the multiple banks that can exist on SDRAM chips. The two banks allowed by the SDRAMC permit the use of different speeds and/or port sizes in the overall memory system.

The interface from the MCF5307 to the SDRAM uses 14 pins as mentioned previously. Because the port size is 32 bits wide, the starting address pin on the MCF5307 is A15. The combined number of address signals is 23 (14 row plus 9 column).

EXAMPLE 2: ADDRESS PIN CONNECTIONS.

SDRAM	MCF5307	SDRAM ROW	SDRAM COLUMN
A0	A15	A15	A02
A1	A14	A14	A03
A2	A13	A13	A04
A3	A12	A12	A05
A4	A11	A11	A06
A5	A10	A10	A07
A6	A09	A09	A08
A7	A17	A17	A16
A8	A19	A19	A18
A9	A20	A20	
A10	A21	A21	
A11	A22	A22	
A12	A23	BS1	
A13	A24	BS0	

Notice that address signals A0 and A1 do not appear in the row/column address tables. Bytes and words are not directly accessible via the address signals. This level of granularity is controlled by the SDRAM DQM signals. Initialization of the SDRAM will be similar to what was described in the first example. There are two Bank Select signals because the Texas Instruments device has four banks on each SDRAM chip. The TI naming convention for these is BS0 and BS1. These perform in the same fashion as the BA signal on the Micron Technologies part. The Micron device had just two banks per chip and therefore required only a single signal for bank selection.

SPECIAL CONSIDERATIONS

It is important to be aware of the design assumptions that are built in to the controller. As part of the design process, certain parameters must be constrained in order to produce an efficient and reliable controller. These determine how the controller will operate in specific circumstances. Some of these conditions are listed below:

RESET State - Following a reset of the MCF5307 processor the SDRAMC is disabled. It must be initialized before operation can begin.

Fixed Page Size - The controller on the MCF5307 is hard-configured for a 512-byte page (column) size. Should memories with larger page sizes be used, the controller will treat any access outside of a 512-byte boundary as a new page. As such, it will “close” the current page and issue a new row address for the new page.

No Mixed Memory Types - The default (out of RESET) mode of operation for the MCF5307 assumes asynchronous DRAMs. This default can be changed by setting the SO bit (bit 15) to a “1” in the DRAM Control Register on the MCF5307. Once synchronous operation is set, it cannot be reversed except by resetting the MCF5307. Both banks will operate in the selected mode. Mixing asynchronous and synchronous DRAMs is not allowed. Each bank can contain a unique configuration of SDRAM. That is, the speeds, port widths, etc. may be different in each of the two banks.

External Master Multiplexing - While the MCF5307 SDRAMC will respond to SDRAM accesses by alternate bus masters, it will not drive the address lines to provide address multiplexing when this occurs. The controller will drive the appropriate control signals only. Addresses must, in this case, be externally multiplexed if required.

Bursting - Many SDRAMs can burst data in various amounts; however, the controller on the MCF5307 does not support this feature. The controller will instead conduct all accesses by directly controlling the address lines. Therefore, if variable-length bursting is available on the chosen SDRAM, the burst option must not be enabled, or the burst length must be set to one. This was done in the setting of the Mode Register in the first example.

EDGESEL - The synchronous edge-select input pin on the MCF5307 can provide additional output hold time for the SDRAM control signals. The usual mode of operation is to use a buffer that slightly delays the BCLKO signal. This delayed signal is then routed to the SDRAM and back to the EDGESEL pin on the MCF5307. This will have the effect of holding the signals to the SDRAM by the amount of buffer and line delay, which helps to ensure that data are held beyond the falling edge of the SDRAM clock input signal. This is a useful feature with regard to meeting memory system timing requirements on high-frequency buses.

Asymmetrical Memory Devices - When asymmetrical memory devices are used (i.e. the memory chips have more row addresses than column addresses), the additional row addresses will be connected by using sequential MCF5307 pins until done. That is, physical pins will not be skipped. Additionally, for 32 bit ports with only eight column addresses, or 8-bit ports with just nine columns, MCF5307 pin A18 can be used to provide SDRAM row address 18 even though it is noted for 16-bit port use only. Likewise for 16-bit ports with eight column address signals, MCF5307 address pin 17 may be used to provide SDRAM row address 17.

Revision History:

Rev. 1.0 - Initial Release

Rev 2.0 - Corrected maximum size of accessible memory. Moved note, in expanded form, from the bottom of the Generic Address Connection Scheme table on page three to text in the Special Considerations section. Corrected calculation of RC Field value in SDRAM Initialization section. Heavily revised description of mode register load procedure to correct errors in rev 1.0. Fixed miscellaneous typos.

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