Application Note

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Minimum MPC8260 PowerQUICC II™ System Configuration

The MPC8260 PowerQUICC II™ is the next generation of highly integrated communications processors from Motorola. The MPC8260 is a versatile communications processor that integrates on one-chip a high performance processor that implements the PowerPC™ architecture, a very flexible system integration unit, and a communications processor module that can be used in a variety of applications, particularly in communications and networking systems.

This application note describes the basic minimum system configuration for the MPC8260. It discusses the basic hardware requirements and register settings for configuring the MPC8260 to support a basic system configuration. A discussion of complexity in setting up various communications protocols is not part of this application note.

1 Introduction

The hardware requirements for a MPC8260 minimum system configuration are as follows:

- MPC8260 PowerQUICC II communications processor module (CPM)
- Power, clocks, reset
- Serial RS232 link
- COP/JTAG interface
- Flash and SDRAM memory on the 60x bus
- SDRAM on the local bus

Figure 1 shows a typical MPC8260 minimum system configuration.

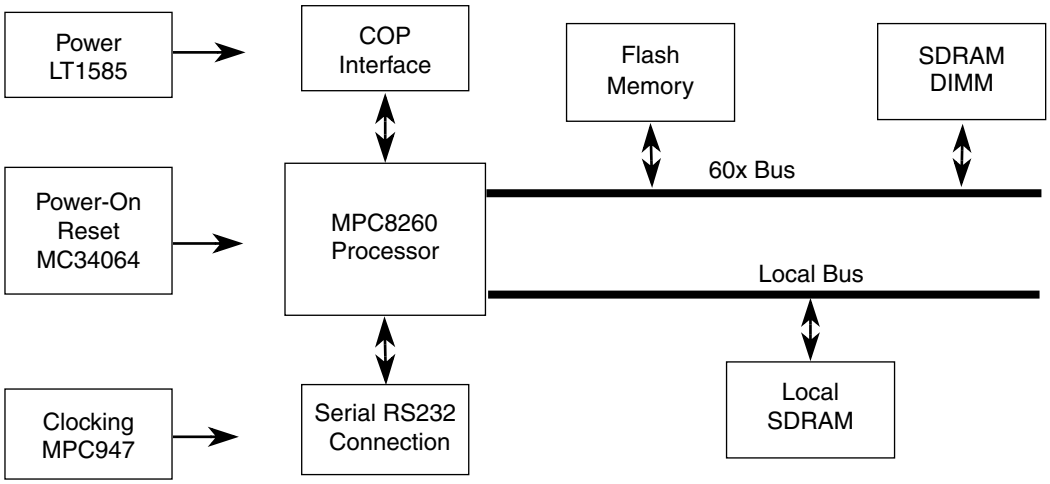


Figure 1. Typical Minimum MPC8260 System Configuration

This configuration includes the following assumptions:

- Single MPC8260 device configured from 4-Mbytes of 32-bit wide Flash memory
- Single MPC8260 bus mode
- Data on the 60x bus is 64 bits wide
- Data on the local bus is 32 bits wide
- 16-Mbyte, 64-bit SDRAM DIMM on the 60x bus
- 4-Mbyte, 32-bit SDRAM memory on the local bus
- The MODCK[1:3] signals determine the PLL multiplication factors, and therefore, the CPM and core frequencies

2 Hardware Requirements

The following sections describe hardware requirements for a minimum MPC8260 system.

2.1 60x Bus Interface

In this configuration, the MPC8260 is configured in single bus mode. It does not support other bus masters or L2 cache controllers, and external pins on the MPC8260 memory controller control external memory and peripheral devices. Figure 2 shows the MPC8260 in single bus mode.

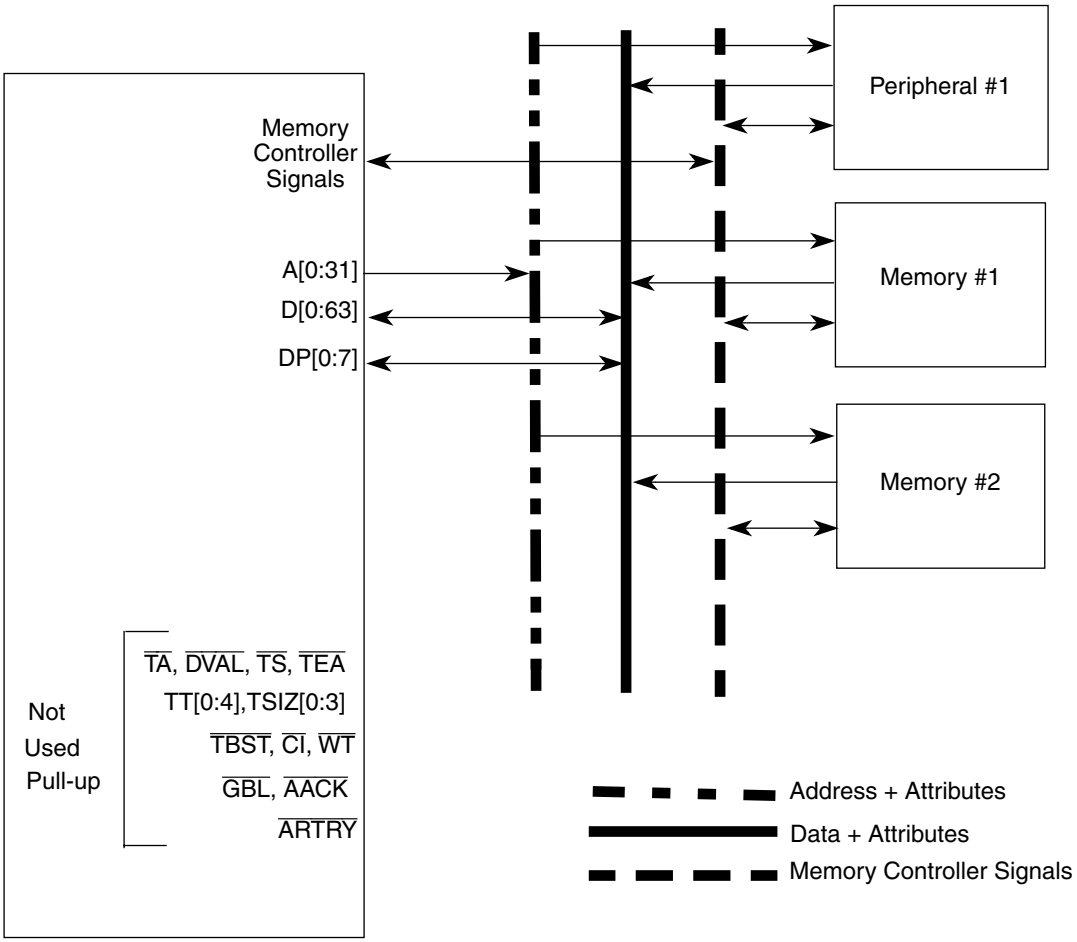


Figure 2. MPC8260 in Single Bus Mode

Single bus mode has only one bus master. Many external signals on the 60x bus can be ignored or wired to the desired state. A number of signals are on the 60x bus, and are multiplexed with other signals, The register setting in the system interface unit (SIU) configuration register (SIUMCR) determines their function. Table 1 shows the recommended terminations for this configuration. For a more complete table on the signal states during HRESET and the recommended terminations, refer to the *MPC8260 Board/System Design Checklist*.

Table 1. External Pins on 60x Bus and Recommendations

External Signal	Comments/Recommended Termination
CPU_BR	Unused. Leave unconnected.
BR, TSIZ[1:3], TT[1:3], ABB, TS, TBST, AACK, ARTRY, DBB, TA, PSDVAL, TEA, GBL/IRQ1, CPU_DBG, BG, DBG	Unused. Pull-up via a resistor to +3.3V (V_{DDH}).

Table 1. External Pins on 60x Bus and Recommendations (continued)

External Signal	Comments/Recommended Termination
TSIZ[0], TT[0]	Unused. Pull-down via resistor to GND.
A[0:31], D[0:63]	Connect to memory devices or peripherals as required.
The following signals are multiplexed. Their function is determined by SIUMCR	
DP[0]/$\overline{\text{RSRV}}$/$\overline{\text{EXT\_BR2}}$	SIUMCR[DPPC] = 00 as default, hence these signals default to interrupts. Unused. Pull-up via a resistor to +3.3V (V_{DDH}).
$\overline{\text{IRQ1}}$/DP[1]/$\overline{\text{EXT\_BG2}}$	
$\overline{\text{IRQ2}}$/DP[2]/$\overline{\text{TLBISYNC}}$/$\overline{\text{EXT\_DBG2}}$	
$\overline{\text{IRQ3}}$/DP[3]/$\overline{\text{CKSTP\_OUT}}$/$\overline{\text{EXT\_BR3}}$	
$\overline{\text{IRQ4}}$/DP[4]/$\overline{\text{CORE\_SRESET}}$/$\overline{\text{EXT\_BG3}}$	
$\overline{\text{IRQ5}}$/DP[5]/TBEN/$\overline{\text{EXT\_DBG3}}$	
$\overline{\text{IRQ6}}$/DP[6]/CSE[0]	
$\overline{\text{IRQ7}}$/DP[7]/CSE[1]	
$\overline{\text{CI}}$/BADDR29/$\overline{\text{IRQ2}}$	Unused. Pull-up via a resistor to +3.3V (V_{DDH})
$\overline{\text{WT}}$/BADDR30/$\overline{\text{IRQ3}}$	
L2_$\overline{\text{HIT}}$/$\overline{\text{IRQ4}}$	
$\overline{\text{CPU\_BG}}$/BADDR31/$\overline{\text{IRQ5}}$	

In single bus mode, the buffer control output signals, $\overline{\text{BCTL}}$[0:1], can still be used to control buffers on the 60x data bus, and furthermore, BADDR[27:31] are not required because A[27:31] performs their function.

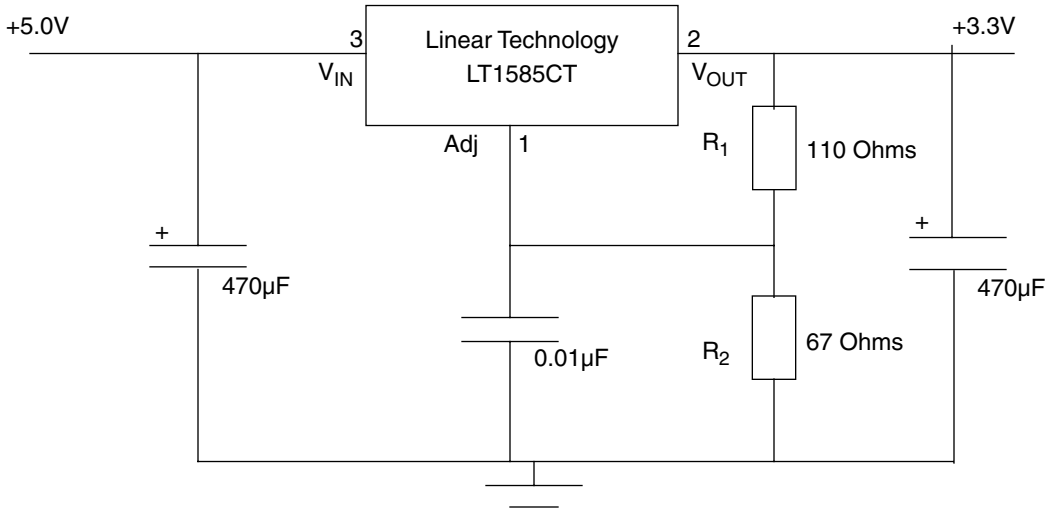
NOTE

The recommended pull-up value is 4.7K to 3.3V (V_{DDH}) and the recommended pull-down value is 10K to GND, unless otherwise noted.

2.2 Power

The MPC8260 has a core voltage V_{DD} that operates at a lower voltage than the I/O voltage V_{DDH}. The MPC826*x* (HiP3) family supports a core voltage V_{DDL} of 2.5V. The MPC826*x*A (HiP4) family supports a core voltage of V_{DDL} of 1.8V. Therefore, Motorola recommends using a variable power supply or regulator to supply the V_{DD} core voltage to maintain future compatibility. For external devices, the I/O voltage, V_{DDH}, remains at 3.3V, which increases the complexity of the system because multiple voltage supplies are required. The tolerance on the core and I/O voltages is ±5%. External signals on the MPC8260 are not 5-V tolerant. All the input signals should meet the V_{IN} DC spec (–0.3V–3.3V).

One of the more popular ways to derive power is to use a simple linear regulator, as shown in Figure 3. Modifying the values of R_2, for example, with R_1 = 110R and R_2 = 67R to adjust V_{OUT} generates an output voltage of 3.3V using the formula for V_{OUT} that Figure 3 shows.



Note: $V_{OUT} = V_{REF}(1 + R_1/R_2) + I_{REF}(R_2)$, where V_{REF} = 1.25V and I_{REF} = 55µA

Figure 3. Power Supply Using Linear Regulator

The MPC8260 has two PLLs that are fed from dedicated voltage supplies to achieve a highly stable output frequency: V_{CCSYN} for the main PLL and V_{CCSYN1} for the core PLL. The V_{CCSYN}/V_{CCSYN1} pins can be tied together. To ensure internal clock stability, these supply signals should be connected to a filtered voltage source by means of a low-impedance path to the V_{DD} power rail only, as Figure 4 shows.

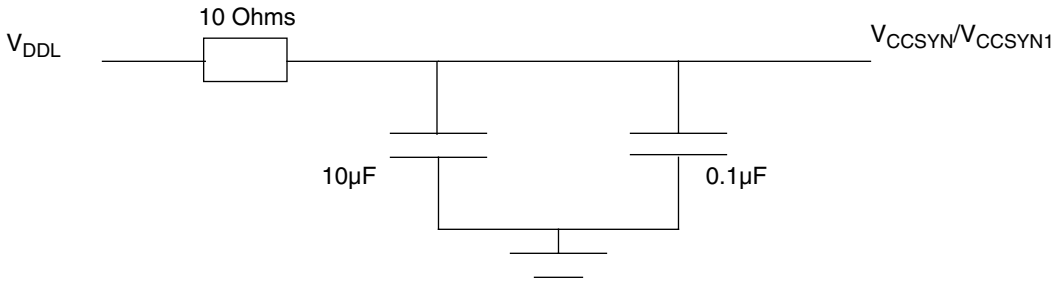


Figure 4. External Components Required for PLLs

GNDSYN should be connected directly to the ground plane.

An external filter capacitor for the main PLL should be connected between the external signal XFC and V_{DDSYN} on the MPC8260. Refer to Section 2.3, “Clocking,” for more information.

2.2.1 Power Sequencing

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates depending upon the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The following restrictions apply to the MPC8260:

- V_{IN} must not exceed the V_{DDH} by more than 2.5V at any time, including during power-on reset.
- V_{DDH} must not exceed V_{DD}/V_{CCSYN} by more than 1.6V at any time, including during power-on reset.
- V_{DD}/V_{CCSYN} must not exceed V_{DDH} by more than 0.4V at any time, including during power-on reset.

NOTE

Internal diodes are connected serially between V_{DDH} and $V_{DD,}$ and vice versa for ESD protection. If one of the voltages (V_{DD} or V_{DDH}) is applied and the other power pins are not driven, the internal diodes pull it up these pins. However, a problem could occur if one of the voltages (V_{DD} or V_{DDH}) is applied and the other voltage is forced to GND. In this case, the ESD diodes might be destroyed.

2.2.2 Decoupling

The core voltage V_{DD} and the I/O voltage V_{DDH} should be decoupled for switching noise. Standard capacitor values of approximately 0.1 µF and 10µF should be used. Motorola recommends using one high frequency decoupling capacitor for every two voltage pins. Following this guideline, use approximately twenty-three 0.1µF and two 10µF capacitors on the V_{DDH} I/O voltage supply, and place as near as possible to the MPC8260. Use approximately nine 0.1µF and one 10µF capacitors on the V_{DD} core voltage supply, place as near as possible to the MPC8260.

2.3 Clocking

In this configuration, the MPC8260 processor and the memory devices all need separate clock signals. The MPC8260 requires a single clock source via the external CLKIN input signal. All bus timings on the MPC8260 are referenced to this clock source. The 60x and local bus frequencies for the MPC8260 are determined from this clock source (refer to the *MPC8260 (HiP3) Hardware Specifications* (Document ID: MPC8260EC/D) or the *MPC826xA (HiP4) Family Hardware Specifications* (Document ID: MPC8260AEC/D), which are available at www.motorola.com/semiconductors).

To achieve clocking in this configuration, an external clock oscillator must be used as the clock source. This clock source must have a very low output impedance in order to drive multiple loads, which in this configuration would include MPC8260 and the memory devices, but could include other processors, peripherals, ASICs, and L2 cache in a more complex system configuration. The simplest way to achieve clocking in an MPC8260 system configuration is to use an inexpensive low-skew clock distribution device such as the MPC947 that Figure 5 shows.

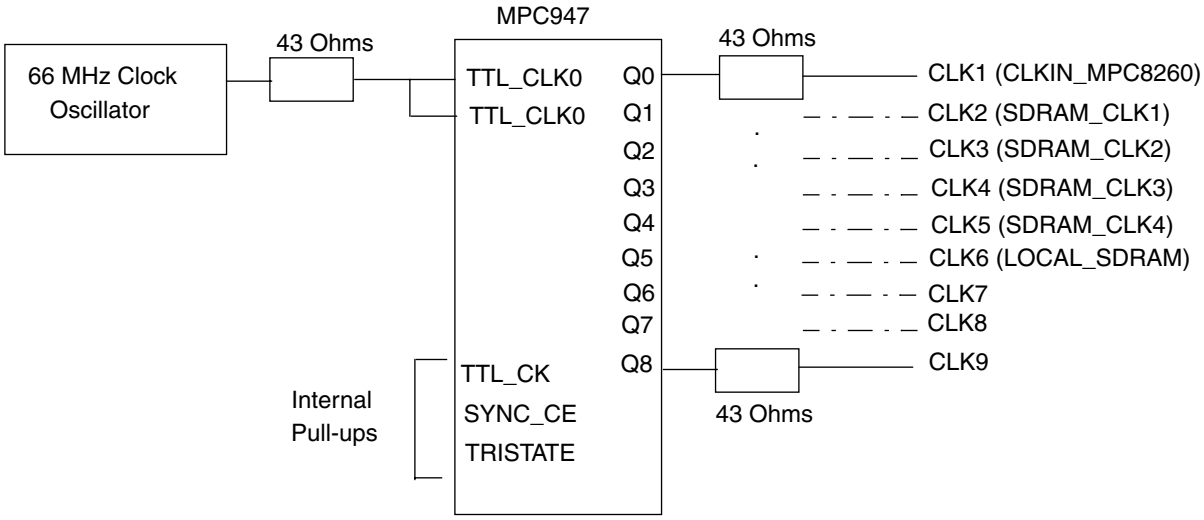


Figure 5. Clock Distribution Using the MPC947

The MPC947 is a 1:9 low-skew clock distribution device that can provide a dedicated clock signal for up to nine devices or system components. A 66.66-MHz clock signal on the input clock signal, CLKIN, of the MPC8260 determines the external bus operating frequencies, but the MPC8260 has two PLLs, which determine the core and CPM operating frequencies. The main PLL can multiply the input clock frequency to determine the CPM frequency. Similarly, the core PLL can multiply the input clock frequency to determine the core frequency.

The seven mode clock bits determine PLL multiplication factors. Three of these bits, MODCK[1:3], are dedicated external signals. The other four bits, MODCK[4:7], are part of the hard reset configuration word (HRCW). These bits select one of several clock options, but this configuration assumes that the MODCK[4:7] bits in the HRCW are zero. Only the eight default clock modes discussed in “Clocks and Power Control,” in the *MPC8260 PowerQUICC II Users Manual* are available. One of these eight default clock modes is selected by the MODCK[1:3] signals, sampled during the assertion of $\overline{\text{HRESET}}$ and $\overline{\text{RSTCONF}}$.

The MODCK[1:3] pins are multiplexed with the following signals.

- MODCK1—AP1/TC0/BNKSEL0
- MODCK2—AP2/TC1/BNKSEL1
- MODCK3—AP3/TC2/BNKSEL2

During the reset configuration sequence, which is executed for 1024 clock cycles, the MODCK[1:3] pins are inputs and are in a high-impedance state. After the reset configuration sequence the values on the MODCK[1:3] pins are sampled once, before the $\overline{\text{HRESET}}$ signal is negated. Hence, the MODCK pins have sufficient time to stabilize before they are sampled. Refer to Section 2.4, “Reset,” for more details. The MODCK[1:3] pins can be configured using just pull-up/pull-down resistors or with active logic.

An external filter capacitor for the main PLL should be connected between the external signal XFC and V_{DDSYN} on the MPC8260. The value of this capacitor is determined by the main PLL multiplication factor shown in Table 2 (if using HiP4 silicon, refer to the *Errata to the MPC8260 PowerQUICC II User's Manual* in addition to the *MPC826xA (HiP4) Family Hardware Specification*).

Table 2. External Filter Capacitor Values

XFC — External filter capacitor—Connects to the off-chip capacitor for the main PLL filter. One terminal of the capacitor is connected to XFC while the other terminal is connected to VCCSYN. 30 MΩ is the minimum parasitic resistance value that ensures proper PLL operation when connected in parallel with the XFC capacitor. XFC capacitor values are shown in the tables below; a definition of the multiplication factor follows:

HiP3 Silicon: Revisions A.1 and B.x

Multiplication Factor	Maximum Allowed Capacitance	Minimum Allowed Capacitance	Unit
MF ≤ 4 [1]	MF x 840 - 90	MF x 750 - 90	pF
MF > 4	MF x 1220	MF x 1100	pF

[1] When MF is 2.5, 3.5, or >4 the internal PLL does not lock reliably; this results in erratic behavior.

HiP3 Silicon: Revision C.2 and Future Revisions

Maximum Allowed Capacitance	Minimum Allowed Capacitance	Unit
MF x 840 - 90	MF x 750 - 90	pF

HiP4 Silicon

Recommended Capacitance	Maximum Allowed Capacitance	Minimum Allowed Capacitance	Unit
MF x 680 - 120	MF x 780 - 140	MF x 580 -100	pF

Definition of Multiplication Factor (MF)

If the ratio of CPM_CLK/CLKIN is an integer (A), MF = A. If CPM_CLK/CLKIN is A.5, MF = 2 x A.5. For example, if CPM_CLK/CLKIN is 166.66 MHz/ 66.66 MHz = 2.5, then MF = 5. The relevant factors are as follows:

CPM_CLK/CLKIN = 2 MF = 2
CPM_CLK/CLKIN = 2.5 MF = 5
CPM_CLK/CLKIN = 3 MF = 3
CPM_CLK/CLKIN = 3.5 MF = 7
CPM_CLK/CLKIN = 4 MF = 4
CPM_CLK/CLKIN = 5 MF = 5
CPM_CLK/CLKIN = 6 MF = 6

2.4 Reset

The following sections describe the various reset facilities recommended for configuring an MPC8260 minimal system.

2.4.1 Power-on Reset

The power-on reset signal ($\overline{\text{PORESET}}$) initiates the power-on reset flow and must be asserted for at least 16 clock cycles whenever the system is initially powered up or when the external power supply falls below 3.3V ± 5%. The MPC8260 has no power-up detection. The simplest way to drive the $\overline{\text{PORESET}}$ signal for the appropriate length is to use an external reset controller such as the MC34064 shown in Figure 6.

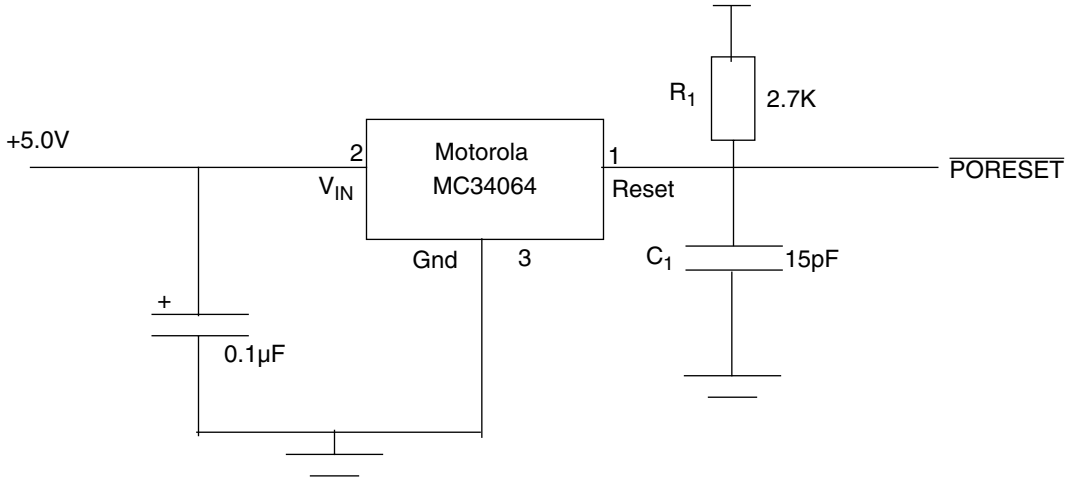


Figure 6. Power-on Reset Controller

The MC34064 is an under-voltage sensing circuit that is typically a reset controller in processor based systems. It offers an economical solution for low-voltage detection with a single external resistor, R_1. A time delayed reset is accomplished with the addition of C_1. Refer to the MC34064 data sheet for more information.

The value driven on the $\overline{\text{RSTCONF}}$ signal while $\overline{\text{PORESET}}$ changes from assertion to negation determines the chip configuration. If $\overline{\text{RSTCONF}}$ is negated (driven high) when $\overline{\text{PORESET}}$ changes, the MPC8260 acts as a configuration slave. If $\overline{\text{RSTCONF}}$ is asserted (driven low) when $\overline{\text{PORESET}}$ changes, the MPC8260 acts as a configuration master. In a minimal system configuration, the MPC8260 device is the configuration master; therefore, $\overline{\text{RSTCONF}}$ is tied to GND.

After $\overline{\text{PORESET}}$ is negated and the $\overline{\text{RSTCONF}}$ signal is sampled, the MPC8260 starts the configuration process. $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ remain asserted throughout the power-on reset process. The reset configuration sequence (which is designed to support up to eight MPC8260 devices, each configured differently) is executed in 1,024 clock cycles, after which time the MODCK[1:3] pins are sampled. The PLL locks according to the mode clock bits sampled on the MODCK[1:3] pins and in the hard reset configuration word. After the PLL lock interval, which can be up to 200µS, $\overline{\text{HRESET}}$ remains asserted for another 512 clocks before being released. $\overline{\text{SRESET}}$ is released three clocks later.

2.4.2 Hardware/Software Reset

$\overline{\text{HRESET}}$ is an open-drain bi-directional signal that can be driven internally when $\overline{\text{PORESET}}$ is asserted or externally to initiate hard reset flow. In both cases, the MPC8260 continues to assert $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$. During the hard reset flow, the hard reset configuration word is re-sampled and executed in 1,024 clock cycles before $\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ are released. All the registers in the MPC8260 are reset including the memory controller registers. However, a hard reset does not affect PLL operation.

$\overline{\text{SRESET}}$ is an open-drain bi-directional signal that can be driven internally when $\overline{\text{PORESET}}$ is asserted or externally to initiate a soft reset flow. In both cases, the MPC8260 asserts $\overline{\text{SRESET}}$ for 512 clock cycles

before the SRESET signal is released. Internal logic and the core are reset, but the hard reset configuration word remains unchanged after a soft reset.

An external pull-up resistor should be added to negate the HRESET and SRESET signals. After the negation of HRESET and SRESET is detected, a 16-clock cycle period is undertaken before the MPC8260 tests for the presence of a hard/soft reset.

To generate an external hard or soft reset, HRESET and SRESET can be asserted manually using a push-button switch.

2.4.3 Hard Reset Configuration Word

The simplest way to configure the MPC8260, if default values in the hard reset configuration word are desirable, is to tie RSTCONF to V_{DDH} or +3.3V. This configuration is applicable only for systems that require single MPC8260 bus mode. The MPC8260 does not try to access any boot PROM during hard reset and it is assumed that the default hard reset configuration word is used upon exiting the hard reset flow. Therefore, bringing up a board with a blank EPROM/Flash device requires a switch or another method to force RSTCONF to a logic '1' to bring up the MPC8260 in the default state.

More typically it is desirable to change the default hard reset configuration word, and in this configuration a single MPC8260 device would be configured from a boot EPROM or flash memory on CS0 as shown in Figure 7.

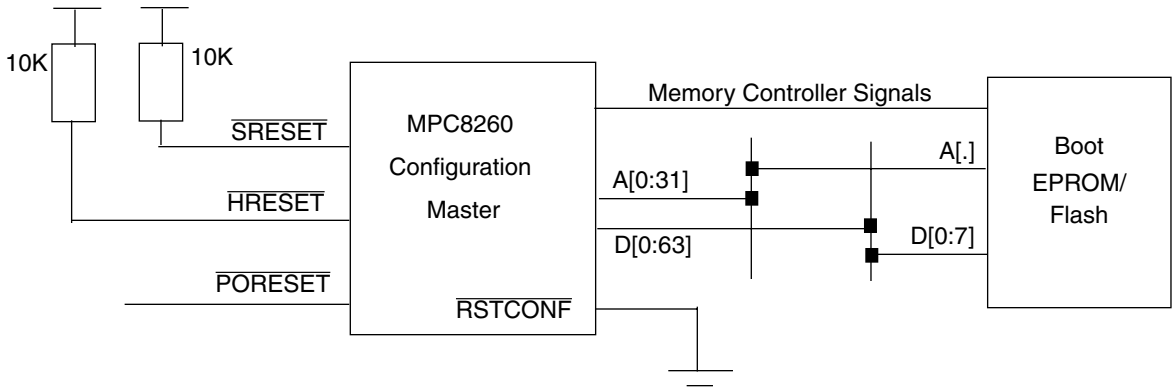


Figure 7. Configuration of a Single MPC8260 Device from a Boot EPROM or Flash Memory

During the hard reset sequence, the configuration master reads the EPROM or Flash at address 0x00, 0x08, 0x10 and 0x18 one byte at a time to assemble the 32-bit hard reset configuration word. Refer to Section 2.5.1, "Memory Map," for the configuration setup for Flash memory.

A total of 32 bytes of data is read from D[0:7] one byte at a time to acquire eight 32-bit configuration words for a system configuration that may have as many as eight MPC8260 devices. In this configuration, only a single MPC8260 is used. Therefore, the configuration word for this device is stored in Flash memory at address 0xFE00_0000 while the other seven configuration words are not initialized.

The hard reset configuration word is provided on D[0:7] and is used during hard reset for initialization/configuration of the MPC8260. The hard reset configuration word and the settings used in this configuration are shown in Table 3.

Table 3. Hard Reset Configuration Word

Bits	Name	Settings	Description—Comments
0	EARB	0	Bus arbitration—Internal bus arbitration is assumed
1	EXMC	0	Memory controller—Internal memory controller is assumed
2	CDIS	0	Core—The core is enabled
3	EBM	0	External bus mode—Single MPC8260 bus mode is assumed
4–5	BPS	11	Boot port size—32-bit boot port size
6	CIP	0	Core initial prefix default
7	ISPS	0	Internal space port size—Defined as 64 bits
8–9	L2CPC	10	L2 cache configuration—For burst address pins
10–11	DPPC	00	Data parity pin configuration—Default used
12	—	0	Reserved
13–15	ISB	010	Initial address of internal RAM space—0x0F00_0000
16	BMS	0	Boot memory space—0xFE00_0000–0xFFFF_FFFF
17	BBD	0	Bus busy—Enable/disable—Defaults used
18–19	MMR	00	Memory mask requests—No masking
20–21	LBPC	00	Local bus pin configuration—Default used
22–23	APPC	00	Address parity pin configuration—Default used
24–25	CS10PS	00	CS10 pin configuration—Default used
26–27	—	0	Reserved
28–31	MODCK_H	0000	MODCK[4:7]

2.5 Memory

The MPC8260 has a flexible memory controller capable of controlling up to 12 memory banks that can be dynamically allocated between the 60x bus and the local bus. The memory controller has three types of machines to interface gluelessly to different types of memory as follows:

- Two general-purpose chip-select machines (GPCM)—These machines provide a glueless interface for simpler, low performance memory devices. Because they do not support bursting, GPCM memory controlled banks are primarily used during booting and access to low performance memory mapped peripherals such as EPROM, Flash, and SRAM.
- Three user-programmable machines (UPM)—These machines support the address multiplexing of external bus, refresh timers and generation of programmable control signals for row address and column address strobes. For this reason UPM memory controlled banks provide a glueless interface to DRAM, burstable SRAM and other types of peripherals.
- Two SDRAM machines—These machines provide a glueless interface to SDRAM memory devices including JEDEC standard SDRAM DIMMs.

The following sections describe the memory map and memory interfaces used in this configuration and the register settings required.

2.5.1 Memory Map

Table 4 shows the memory map that is established for this configuration. This memory map includes 4 Mbytes of buffered Flash memory and 16 Mbytes of SDRAM on the 60x bus. A 4-Mbyte SDRAM on the local bus can be used for connection tables and general data buffer storage for communication protocols.

Table 4. Memory Map Definition

Address Range	Description	Port Size
FE000000—FE3FFFF	4 Mbytes of buffered Flash memory on the 60x bus for boot code.	32 bit
00000000—00FFFFFF	16 Mbyte SDRAM DIMM on the 60x bus with page-based interleaving.	64 bit
04000000—043FFFFF	4 Mbytes of SDRAM memory on the local bus with bank-based interleaving.	32 bit

The MPC8260 supports two methods of internal bank interleaving:

- Page-based interleaving—This method uses the low address bits as the bank_select for SDRAM, allowing interleaving on every page boundary.
- Bank-based interleaving—This method uses the most significant address bits as the bank select for SDRAM, allowing interleaving only on bank boundaries.

Page-based interleaving is the preferred method for connecting to SDRAM, because it provides higher performance and is typically used on larger SDRAM memory devices. However, bank-based interleaving is still required for compatibility with existing designs. In this configuration, to illustrate the use of these two methods for internal bank interleaving, page-based interleaving is used on the 60x bus for the 16-Mbyte SDRAM DIMM, and bank-based interleaving is used on the local bus for the 4-Mbyte SDRAM memory.

2.5.2 Flash

In this configuration, 4 Mbytes of 32-bit wide Flash memory is supported on the 60x bus. The 4 Mbytes of Flash memory uses two AM29LV160B Flash memory devices from AMD that are two Mbytes each. The MPC8260 controls this memory bank using one of the GPCM and the global chip-select line, $\overline{CS0}$, for booting purposes. Figure 8 shows the interface between this 4-Mbyte Flash memory and the MPC8260, including the memory controller signals.

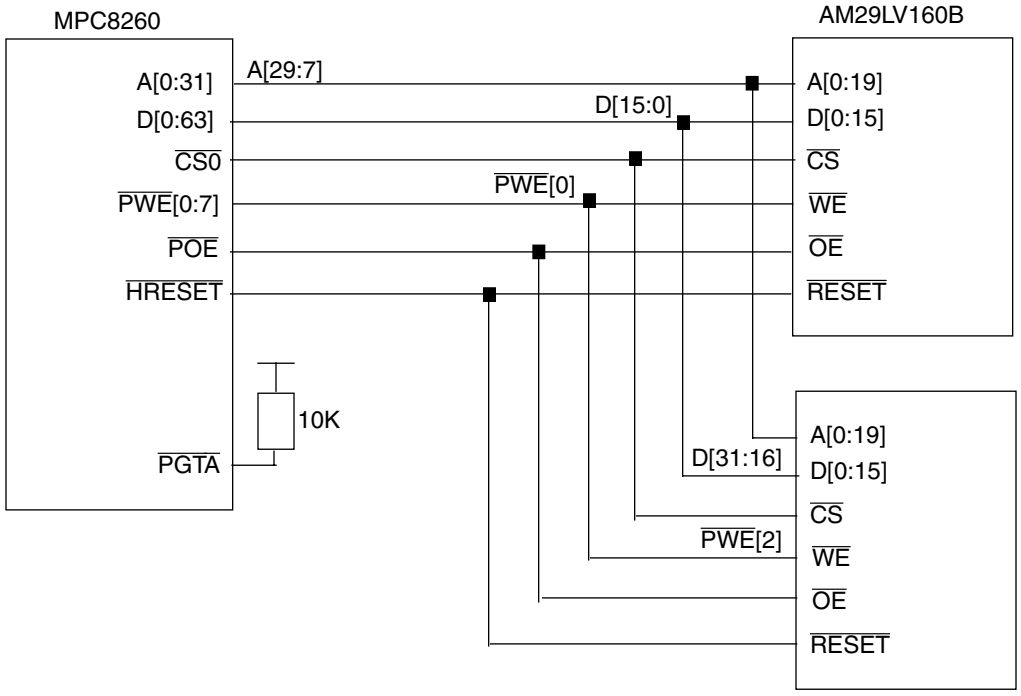


Figure 8. Glueless Interface to 4 Mbytes of Flash Memory on the 60x Bus

Refer to the AMD AM29LV160B data sheet for more information.

The data lines of most Flash devices are connected to the MPC8260 with the byte lanes reversed for programming algorithm purposes as shown in Figure 9.

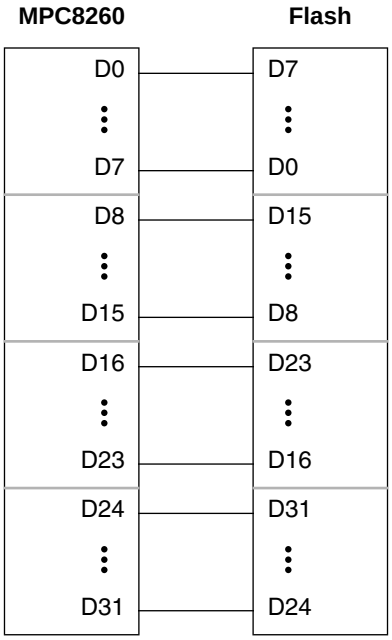


Figure 9. MPC8260 to Flash Byte Lane Reversal

The GPCM on the 60x bus uses the following register settings in this configuration to control the 4-Mbyte Flash memory:

- Base Register $\overline{CS0}$ (BR0) = FE001801
  - BA = 11111110000000000 'Locates Flash at base address FE000000'
  - PS = 11 '32-bit port size'
  - DECC = 00 'Data error checking disabled'
  - WP = 0 'Read and write accesses are allowed'
  - MS = 000 'Selects GPCM on the 60x bus'
  - EMEC = 0 'Accesses are handled by the memory controller according to machine select'
  - ATOM = 00 'The address spaced controlled by this memory bank is not used for atomic operations'
  - DR = 0 'No data pipelining is done'
  - V = 1 'This bank is valid'
- Options Register $\overline{CS0}$ (OR0) = FFC00866
  - AM = 1111111111000 'Address mask corresponding to BA bits in BR0 determines 4 Mbyte block'
  - BCTLD = 0 'BCTLx is asserted upon access to current memory bank'
  - CSNT = 1 '$\overline{CS}$/$\overline{WE}$ are negated a quarter clock earlier'
  - ACS = 00 '$\overline{CS}$ is output at the same time as the address lines'
  - SCY = 0110 'Determines the number of wait states inserted in the cycle (in this case 6 wait states)'
  - SETA = 0 'PSDVAL is generated internally by the memory controller'

— TRLX = 1 'Relaxed timing is generated by the GPCM for accesses initiated to this memory bank'

— EHTR = 10 'Four idle clock cycles are inserted'

2.5.3 60x SDRAM DIMM

In this configuration, a 16-Mbyte, 64-bit wide SDRAM DIMM is supported on the 60x bus. The 16-Mbyte SDRAM DIMM used is supplied by Fujitsu SDC2UL6484-84-T-S and conforms to the JEDEC standard. The MPC8260 controls this SDRAM memory bank using the SDRAM machine on the 60x bus and one chip-select line ($\overline{CS2}$), This SDRAM DIMM has only two memory banks, and a 256-byte serial EPROM on the SDRAM DIMM contains the DIMM configuration information. The SDRAM DIMM has dedicated control signals—serial data input/output (SDA), serial clock (SCL), and decode inputs (SA0–SA2)—to determine the control information in the serial EPROM.

The I^2C controller on the MPC8260 is used in this configuration to control the serial EPROM on the SDRAM DIMM and switch settings provide the slave address for the serial EPROM. The clock input signals for the SDRAM DIMM, are provided from the MPC947 clock distribution chip. The interface between this 16-Mbyte SDRAM DIMM and the MPC8260, including the memory controller signals, is shown in Figure 10.

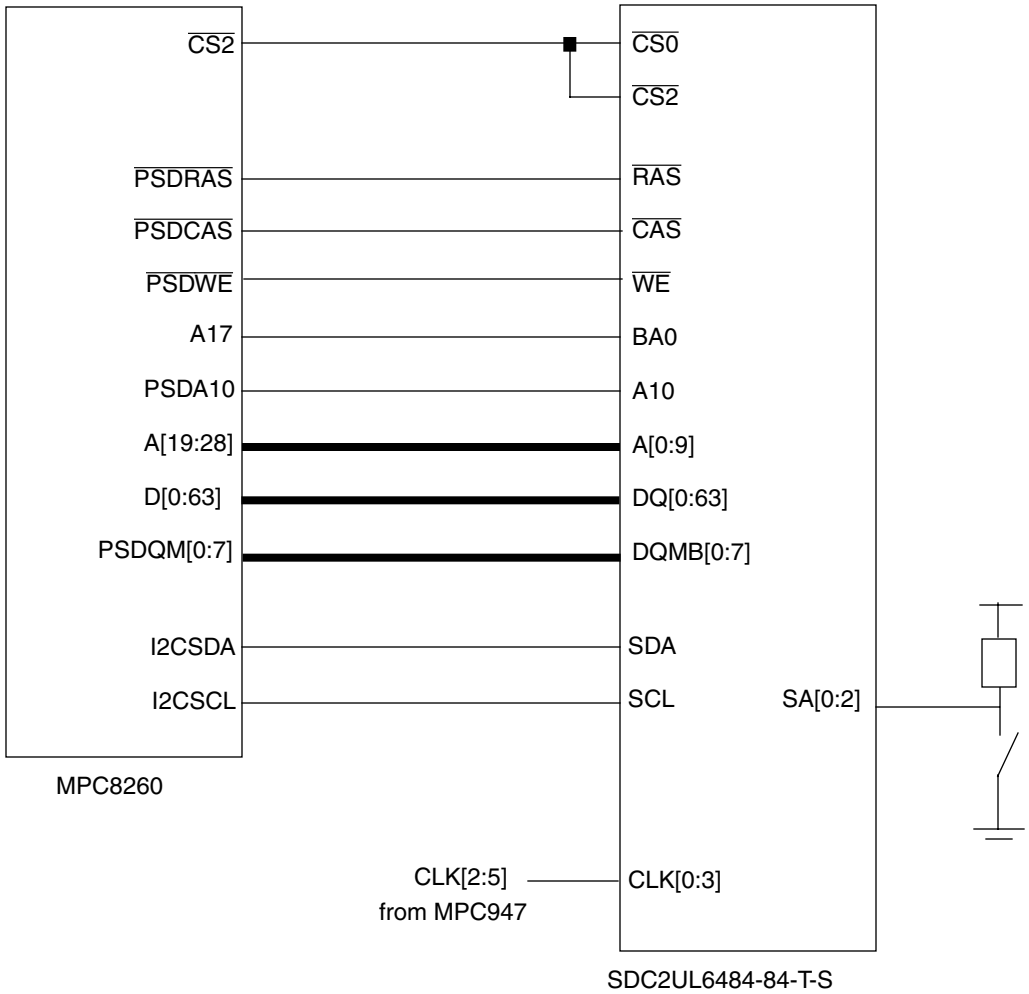


Figure 10. Glueless Interface to 16 Mbytes SDRAM DIMM

Refer to the Fujitsu SDC2UL6484-84-T-S data sheet for more information.

The following register settings were used in this configuration by the SDRAM machine on the 60x bus to control the 16-Mbyte SDRAM DIMM:

- Base Register $\overline{CS2}$ (BR2) = 00000041
  - BA = 0000000000000000 'Locates SDRAM DIMM at base address 00000000'
  - PS = 00 '64-bit port size'
  - DECC = 00 'Data error checking disabled'
  - WP = 0 'Read and write accesses are allowed'
  - MS = 010 'SDRAM machine on 60x bus'
  - EMEC = 0 'Accesses are handled by the memory controller according to MS'
  - ATOM = 00 'The address spaced controlled by this memory bank is not used for atomic operations'
  - DR = 0 'No data pipelining is done'
  - V = 1 'This bank is valid'
- Options Register $\overline{CS2}$ (OR2) = FF001280
  - SDAM/LSDAM = 11111 1110000 0000 = 'SDRAM address mask determines 16-Mbyte block size'
  - BPD = 00 '2 internal banks per device'
  - ROWST = 1001 'Defines A9 as row start address bit for page-based interleaving'
  - NUMR = 010 '11 row address lines'
  - PMSEL = 0 'Back-to-back page mode/normal operation'
  - IBID = 0 'Internal bank interleaving within same device not disabled'
- 60x SDRAM mode register (PSDMR) = C166B452
  - PBI = 01'Page-based interleaving'
  - RFEN = 1 'Refresh services enabled'
  - OP = 000 'Normal operation'
  - SDAM = 001 'Address line A19 multiplexed out on external address line A28'
  - BSMA = 011 'Bank select [0:2] multiplexed on address lines A15–A17'
  - SDA10 = 001 'Determines address line A9 is output and A10 is control for page-based interleaving'
  - RFRC = 101 'Determines 7 clocks for refresh recovery'
  - PRETOACT = 011 'Determines 3 clock cycle wait states for precharge to activate interval'
  - ACTTORW= 010 'Determines 2 clock cycle wait states for activate to read/write interval'
  - BL= 0 'Burst length is 4'
  - LDOTOPRE = 01 = 'Determines 1 clock cycle for last data out to precharge'
  - WRC = 01 = 'Determines 1 clock cycle for write recovery time'
  - EAMUX = 0 = 'No external address multiplexing'
  - BUFCMD = 0 = 'Normal timing for control lines'
  - CL = 10 = 'Defines CAS latency as 2"
- Memory refresh timer prescaler register (MPTPR) = 2000
  - PTP = 00100000 = 'Defines a refresh timer prescaler of 32'

- 60x bus-assigned SDRAM refresh timer (PSRT) = 1C 'Determines the timer refresh period as follows:
  - Timer Period = (PSRT/(System Bus Frequency/MPPR) = 28/(66 MHz/32) ~ 13.6µS'

2.5.4 Local SDRAM

In this configuration, 4-Mbytes of SDRAM memory (32 bits wide) is supported on the local bus. The 4 Mbytes of SDRAM memory uses two MB811171622A-84 SDRAM memory devices from Fujitsu that are 2 Mbytes each. The MPC8260 controls this SDRAM memory bank using the SDRAM machine on the local bus and chip-select line $\overline{CS4}$. The interface between 4 Mbytes of SDRAM memory and the MPC8260, including the memory controller signals, is shown in Figure 11.

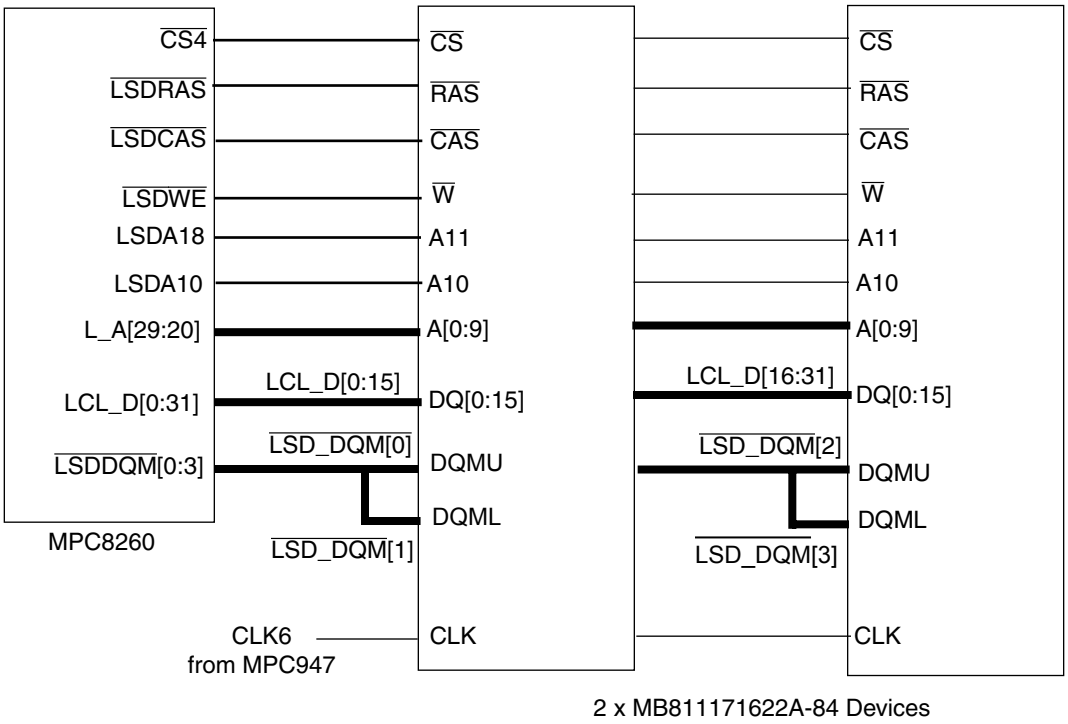


Figure 11. Glueless Interface to 4-Mbytes of SDRAM on the Local Bus

Refer to the Fujitsu MB81171622-84 data sheet for more information. The following register setting were used in this configuration by the SDRAM machine on the local bus to control 4 Mbytes of SDRAM memory:

- Base register $\overline{CS4}$ (BR4) = 04001861
  - BA = 00000100000000000 'Locates SDRAM Memory at Base Address 04000000'
  - PS = 11'32-bit port size'
  - DECC = 00 'Data error checking disabled'
  - WP = 0 'Read and write accesses are allowed'
  - MS = 011 'SDRAM machine on local bus'
  - EMEC = 0 'Accesses are handled by the memory controller according to MS'
  - ATOM = 00 'The address spaced controlled by this memory bank is not used for atomic operations'

  - DR = 0 'No data pipelining is done'
  - V = 1 'This bank is valid'
- Options register $\overline{CS4}$ (OR4) = FFC01480
  - SDAM/LSDAM = 11111 1111100 0000 = 'SDRAM address mask determines the 4-Mbyte block size'
  - BPD = 00 '2 internal banks per device'
  - ROWST = 1010 'Defines A11 as row address start bit'
  - NUMR = 010 '11 row address lines'
  - PMSEL = 0 'Back-to-back page mode/normal operation'
  - IBID = 0 "Internal bank interleaving within same device not disabled'
- Local bus SDRAM mode register (LSDMR) = 4086B552
  - PBI = 0 'Bank-based interleaving'
  - RFEN = 1 'Refresh services enabled'
  - OP = 000 'Normal operation'
  - SDAM = 000 'Address line A23 multiplexed out on external address line A31'
  - BSMA = 100 'Bank select [0:2] multiplexed on address lines A16–A18'
  - SDA10 = 001 'Determines address line A11 is output and A10 is control'
  - RFRC = 101 'Determines 7 clocks for refresh recovery'
  - PRETOACT = 011 'Determines 3 clock cycle wait states for precharge to activate interval'
  - ACTTORW= 010 'Determines 2 clock cycle wait states for activate to read/write interval'
  - BL= 1'Burst length is 8'
  - LDOTOPRE = 01 = 'Determines 1 clock cycle for last data out to precharge'
  - WRC = 01= 'Determines 1 clock cycle for write recovery time'
  - EAMUX = 0 = 'No external address multiplexing'
  - BUFCMD = 0 = 'Normal timing for control lines'
  - CL = 10 = 'Defines CAS latency as 2'
- Memory refresh timer prescaler register (MPTPR) = 2000
  - PTP = 00100000 = 'Defines a refresh timer prescaler of 32'
- Local bus-assigned SDRAM refresh timer (LSRT) = 1C—Determines the timer refresh period as follows:
  - Timer period = (LSRT/(System Bus Frequency/MPPR) = 28/(66 MHz/32) ~ 13.6µS'

2.5.5 Connecting Data Buffers

In this configuration, the memory devices on the 60x bus and the local bus are not buffered. However, in most system configurations, Flash memory is buffered. The memory controller on the MPC8260 supports this requirement by providing two data buffer control signals for the 60x bus—$\overline{BCTL0}$ and $\overline{BCTL1}$. These control signals are activated when a GPCM or UPM controlled memory bank is selected and can be disabled by setting ORx[BCTLD]. The polarity of these control signals is determined by the register setting SIUMCR[BCTLC].

Figure 12 shows how one of the buffer control signals ($\overline{\text{BCTL0}}$) could be used to control two MC74LVT16245 low-voltage, 16-bit transceivers for buffering the data bus between the MPC8260 and the 4 Mbytes of Flash memory.

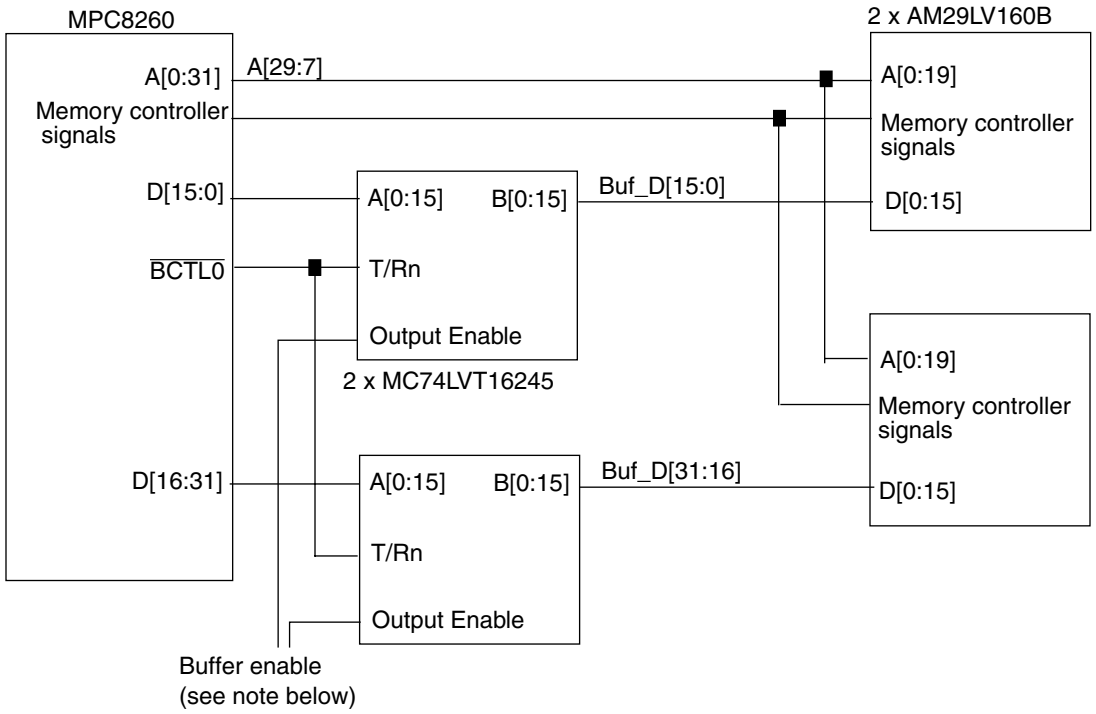


Figure 12. Buffered Flash Memory using the $\overline{\text{BCTL0}}$ Control Signal

NOTE

Depends on which peripheral/memory devices in the configuration require data be buffered. The buffer enable signal should be generated using programmable control logic for these devices. Refer to the *MPC8260 Power QUICC II Application Development Board User's Manual* for more information.

2.5.6 Future Compatibility

In system configurations where the MPC8260 is used in 60x bus compatible mode and the internal memory controller is used, the BADDR [27:31] pins must be connected to the least-significant address lines of the memory device or the peripheral being accessed for burst accesses and not the standard address (A[27:31]) pins. For SDRAM, the BADDR pins are only required for 16 bit and 8 bit port sizes. Refer to the "Address Incrementing for External Bursting Masters," section in "Memory Controller," in the *MPC8260 PowerQUICC II User's Manual*.

Example Setup:

- For 8-bit wide memory interfaces (including SDRAM), connect the BADDR pins 31, 30, 29, 28, and 27 to A0, A1, A2, A3 and A4 of the memory interface.
- For 16-bit wide memory interfaces (including SDRAM), connect the BADDR pins 30, 29, 28, and 27 to A0, A1, A2 and A3 of the memory interface.
- For 32-bit wide memory interfaces (not SDRAM), connect the BADDR pins 29, 28, and 27 to A0, A1, and A2 of the memory interface.

NOTE

The BADDR[31:29] pins are multiplexed with L2 cache control pins $\overline{\text{CPU\_BG}}$, $\overline{\text{WT}}$ and $\overline{\text{CI}}$. In system configurations where an 8-bit or 16-bit Flash interface and external L2 cache control is required, only use one set of functionality on these pins at any one time. In these configurations, power the MPC8260 with the BADDR functionality enabled and copy the code from Flash to SDRAM. Then reconfigure these pins for L2 cache operation and run the code from SDRAM.

Use the BNKSEL[0:2] pins instead of the bank select signals on the multiplexed address lines to allow SDRAM bank interleaving and to facilitate compatibility with SDRAM memory devices with different numbers of row and column address lines.

2.6 COP/JTAG Interface

The MPC8260 implements a common on-chip processor function (COP) function, a feature common to all Motorola processors that implement the PowerPC architecture except the MPC8xx family. This feature allows internal access to scan chains for debug purposes and is also used as a serial connection to the core for emulator support. Adding a COP connection adds little or no cost to the system, but adds significant advantages during early system development. The COP interface is implemented using a standard 16-pin header with the pinout, as shown below in Figure 13.

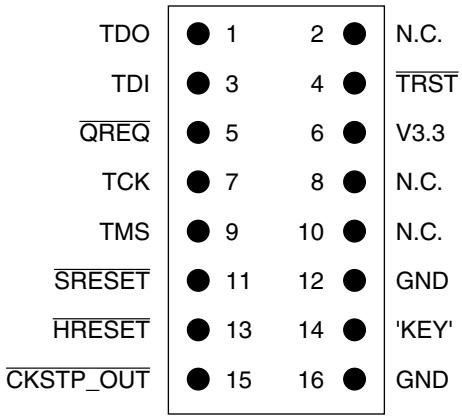


Figure 13. 16-Pin Header for COP/JTAG Interface

The COP interface connects through the JTAG port on the MPC8260, with some additional status monitoring signals. Table 5 shows the pin definitions and recommendations.

Table 5. COP/JTAG Interface Pin Definitions

Pins	Connection	Description	Recommendations
1	TDO	Test Data Out	—
2,8,10	N.C.	No Connect	Leave not connected
3	TDI	Test Data In	—
4	TRST	Test Reset	Connect to MPC8260 $\overline{\text{TRST}}$ signal, but add 1K pull-down to ground
5	QREQ	Quiescent Request	Connect to MPC8260 $\overline{\text{QREQ}}$ signal

Table 5. COP/JTAG Interface Pin Definitions (continued)

Pins	Connection	Description	Recommendations
6	V3.3	I/O Power Supply	Connect to MPC8260 I/O Voltage
7	TCK	Test Clock	—
9	TMS	Test Mode Select	—
11	SRESET	Soft Reset	Connect to the $\overline{\text{SRESET}}$ and $\overline{\text{HRESET}}$ signals on the MPC8260 using open circuit gates. Refer to section 2.6.1
13	HRESET	Hard Reset	
14	'KEY'	Mechanical Keying	Pin should be removed.
15	CKSTP_OUT	Check Stop Output	Add 10K pull-up to VCC = 3.3V
12, 16	GND	System Ground Plane	Connect to digital ground

2.6.1 Merging Reset Signals

The COP interface requires the ability to assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ independently to control the processor. If the target system has multiple independent reset sources, such as voltage monitors, watchdog timers, low voltage detectors or manual push-button switches that can cause a system reset, the reset signals on the COP header must be merged into these signals with logic. These reset signals cannot be simply wired together; damage to the COP or target system occurs.

The arrangement shown in Figure 14 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring the target system can drive $\overline{\text{HRESET}}$ as well. The Pull-down resistor on $\overline{\text{TRST}}$ ensures that the JTAG scan chain is initialized properly during power-on if COP is not attached. If COP is attached, it is responsible for driving $\overline{\text{TRST}}$ when needed.

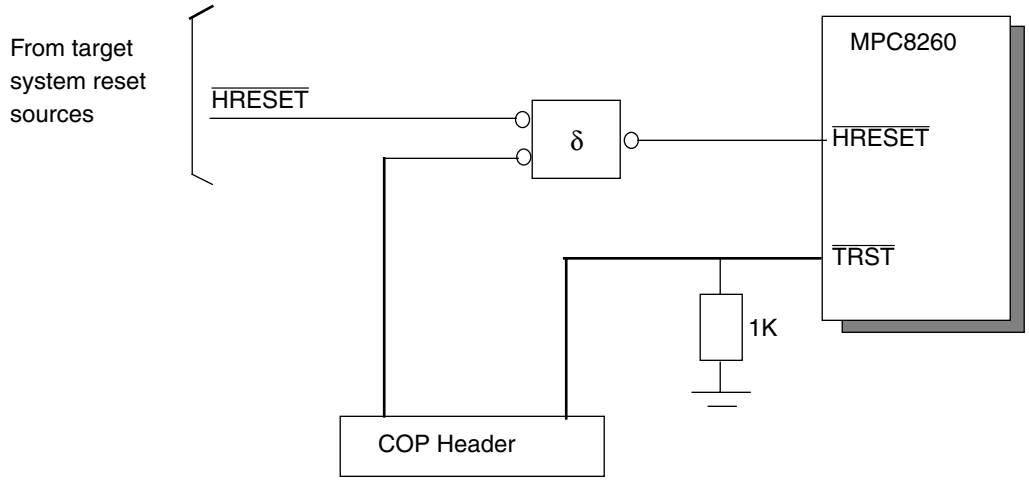


Figure 14. COP Merging Reset Signals

2.6.2 Nonscan Chain Operation

In nonscan chain operation, the TCK input does not include an internal pull-up resistor. A10K pull-up resistor to +3.3V or V_{DDH} should be connected to TCK.

To ensure that the scan chain test logic is kept transparent to the system logic, the TAP controller should be forced into a test-logic-reset state. This step is done automatically within the MPC8260 because $\overline{\text{TRST}}$ and $\overline{\text{PORESET}}$ are connected together internally.

A 10K pull-up resistor to 3.3V or V_{DDH} should be connected to TMS, and it should not change state. This ensures that the TAP controller does not leave the test-logic-reset state.

2.7 Serial RS232 Connection

The MPC8260 has four serial communications controllers (SCCs) that support transmit (TXD, TCLK), receive (RXD, RCLK) and flow control ($\overline{\text{CTS}}$, $\overline{\text{CD}}$, $\overline{\text{RTS}}$) signals. All four SCCs are capable of implementing the UART protocol. The MPC8260 can implement an RS232 serial connection required to communicate with a HOST PC for debug using one of its SCCs. In this configuration, SCC4 has been chosen, and only transmit and receive functionality is used. Four SCC4 port pins PD21 and PD22 are used for TXD4 and RXD4, respectively. Figure 15 illustrates the serial RS232 connection, using a Maxim 3.3 volt RS232 driver to interface to a 9-way D type connector. This serial connection is able to run at 115.2Kbps when communicating with the host PC.

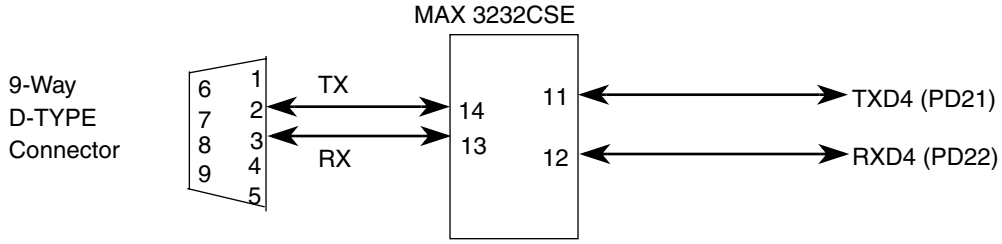


Figure 15. Serial RS232 connection using Maxim RS232 driver (Max 3232)

The following register setting were used in this configuration to set-up Port D as required above:

- PODRD = 0x0000_0000
- PDATD = 0x0000_0000
- PDIRD = 0x0000_ 0400
- PPARD = 0x0000_0600
- PSORD = 0x0000_0000

2.8 Parallel I/O Ports

The CPM of the MPC8260 supports four general purpose parallel I/O ports as follows:

- Port A—32 Bits
- Port B—28 Bits
- Port C—32 Bits
- Port D—28 Bits

Each pin in the I/O ports can be configured as a general-purpose I/O signal or as a dedicated peripheral interface signal. Port C is unique in that 16 of its pins have external interrupt capability.

The default configuration for these I/O ports is inputs, and these port pins do not have internal pull-up or pull-down resistors. Unused parallel I/O port pins may be configured as outputs after reset and left

unconnected. However, unused parallel I/O port pins configured as inputs should be tied high or low but not left unconnected.

2.9 Layout Practices

Careful consideration must be given to component placement and layout, keeping components as near as possible to the chip and keeping all trace lengths to a minimum.

Each voltage supply pin Core (V_{DD}) and I/O (V_{DDH}) on the MPC8260 should be provided with a low-impedance path to the board's power supplies. Likewise each ground pin should be provided with a low-impedance path to ground. It is recommended to use one ground plane, one power plane for the I/O voltage (V_{DDH}). It is also recommended to use either a full power plane or a split power plane for the core voltage (V_{DD}). Four signal planes are normally used to ensure routing to/from the MPC8260.

Decoupling capacitors (Refer to section 2.2.2) should be located as close as possible to the four sides of the device package. The capacitor leads and associated printed circuit traces connecting the voltage supplies and ground should be kept to less than half an inch per capacitor lead.

All output pins on the MPC8260 have fast rises and fall times. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections that these fast output switching times cause. This recommendation particularly applies to address and data buses. Maximum PC trace lengths of six inches are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitance due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the voltage supply and GND circuits. Pull-up all unused inputs or signals that will be inputs during reset. Special care should be taken to minimize the noise levels on the PLL supply pins.

3 Conclusion

This document design allows users to understand the hardware requirements for a simple system design using the MPC8260 without requiring a detailed knowledge of the device. It can be implemented with a small amount of hardware by following the examples listed in this document, which have been proven on the following reference designs:

- MPC8260 Application Development System Board (ADS)
- MPC8260/MPC750 (Scout) reference design

Furthermore, the simple MPC8260 configuration described in this paper can be enhanced to include the following features and communication interfaces found on the above reference designs and on the MPC8260 T1/E1 communication board.

- 60x Bus Compatible Mode with support for multiple bus masters including L2 Cache
- 10/100Mbps Ethernet Ports
- Up to 155Mbps SAR ATM Ports
- Multiple T1/E1 Interfaces

For software developers, a number of features on the MPC8260 must be initialized properly out of reset. An initialization code example is available for the MPC8260, which sets up these features. Example software drivers are also available for the integrated communication features of the MPC8260. All of this information is available on the web: www.motorola.com/semiconductors.

4 References

It is important that users familiarize themselves with the following references for a better understanding of the terminology and general MPC8260 programming model.

- *MPC8260 PowerQUICC II User's Manual* (MPC8260UM/D Rev.0)
- *MPC8260 PowerQUICC II User's Manual Errata* (MPC8260UMAD/D)
- *MPC8260 (HiP3) Hardware Specification* (MPC8260EC/D)
- *MPC8260A (HiP4) Family Hardware Specification* (MPC8260AEC/D)
- *MPC8260 PowerQUICC II Board/System Design Checklist*
- *MPC8260 PowerQUICC II Application Development Board User's Manual* (MPC8260ADSUM)
- *MPC8260 PowerQUICC II Application Development Board User's Schematics* (MPC8260ADSCH1)
- *MPC8260 PowerQUICC II TCOM User's Manual* (MPC8260TCOMUM)
- *MPC8260/MP750 (Scout) Reference Designs Specification* (MPC8260RD4)
- *MPC8260/MP750 (Scout) Reference Designs Schematics* (MPC8260SCH2)
- *MPC603e RISC Microprocessor User's Manual* (MPC603EUM/AD Rev. 3)
- *Programming Environments Manual for 32-Bit Implementations of PowerPC Architecture* (MPCFPE32B/AD Rev.2)

These references are available on the web at www.motorola.com/semiconductors

5 Document Revision History

Table 6 shows changes made to this document.

Table 6. Document Revision History

Revision	Changes
0	Initial release of document
0.1	Nontechnical editorial changes
0.2	Update to XFC calculation in Table 2
0.3	Nontechnical reformatting

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