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Functional Pin Differences Between the MSC8101 and MPC8260 Communications Processor Modules

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The MSC8101 processor consists of three internal modules: the communications processor module (CPM), the system interface unit (SIU), and the extended core (which includes the StarCore™ SC140 core). This application note focuses on the CPM. The MSC8101 CPM is based on the MPC8260 CPM. This application note compares the functional pin differences between the MSC8101 and the MPC8260 CPMs.

This document starts with a high-level overview of the CPM and then lists the functionality on each parallel I/O (PIO) pin for the MSC8101 and the MPC8260 CPMs. Figures and tables identify the following:

- Overview of MSC8101 versus MPC8260 CPM
- CPM block diagram
- MSC8101 versus MPC8260 PIO ports
- MSC8101 versus MPC8260 serial channels
- MSC8101 CPM multiplexing logic block diagram
- Interrupt lines
- MSC8101 versus MPC8260 Port A–D pins

For more information on the MSC8101 and MPC8260 processors, refer to the following manuals:

- *MSC8101 Reference Manual*
- MPC8260 PowerQUICC II™ User's Manual

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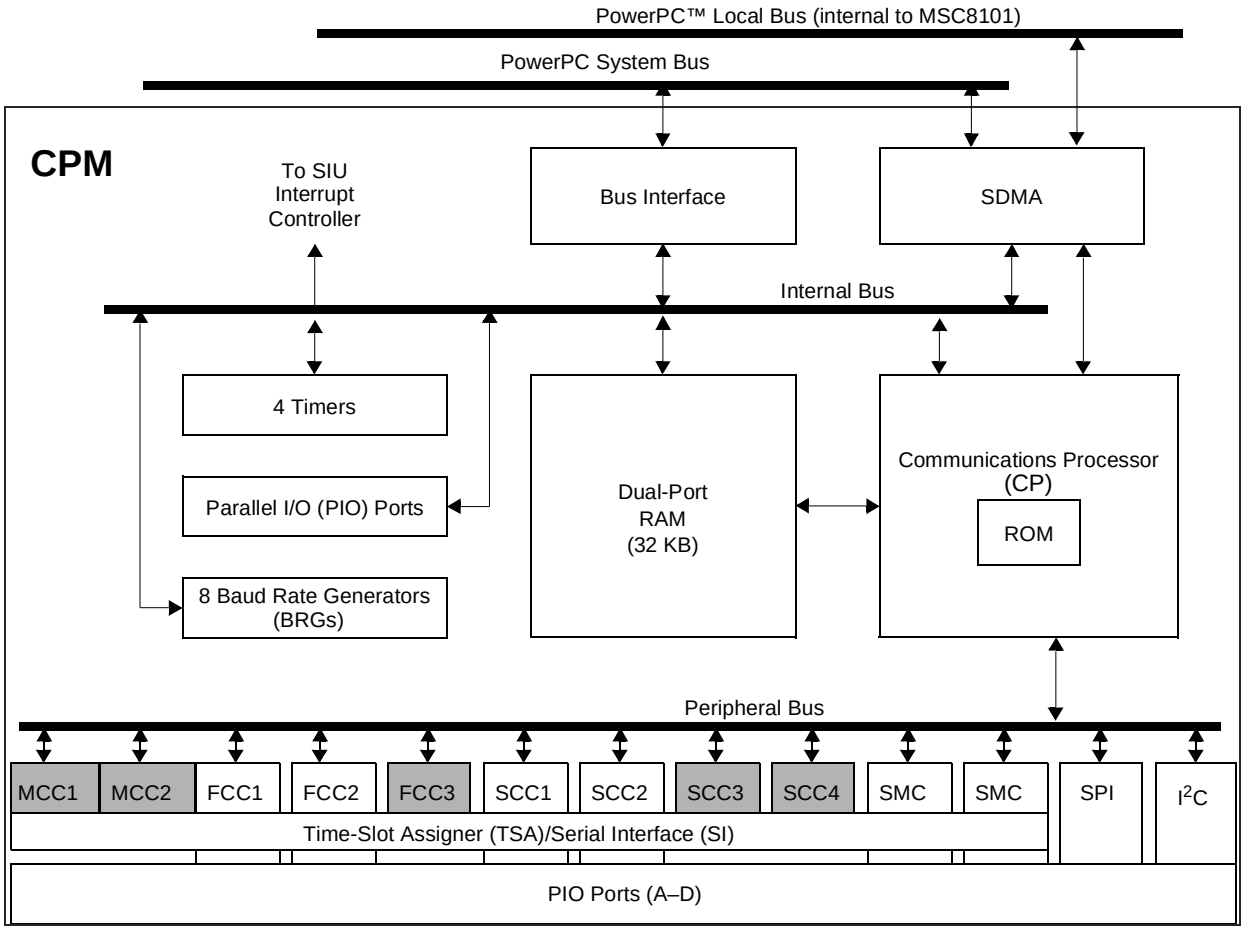
1 Overview

The MSC8101 is a highly integrated StarCore™-based DSP for use in third-generation wireless infrastructure systems and wireline multichannel applications that require networking support (Ethernet, asynchronous transfer mode (ATM), and so on).

The MPC8260 is a highly integrated fourth generation (MC68302, MC68360, MPC860, and MPC8260) microprocessor for use in multi-channel applications that require networking support (Ethernet, ATM, and so on). The MSC8101 CPM is based on the MPC8260 CPM. **Figure 1** depicts the general CPM block diagram for both the MSC8101 and the MPC8260.



Note: Shaded areas available only through one of four common TDM interfaces. TDM buses are part of the PIO ports.

Figure 1. CPM Block Diagram

Table 1 shows the major differences between the MSC8101 and MPC8260 CPMs.

Table 1. Overview of MSC8101 Versus MPC8260 CPMs

MSC8101	MPC8260
66 I/O ports	120 I/O ports
4 time-division multiplexors (TDMs)	8 TDMs
10 CPM clock inputs	20 CPM clock inputs

Table 1. Overview of MSC8101 Versus MPC8260 CPMs (Continued)

MSC8101	MPC8260
8 general-purpose I/O lines with interrupt capability	16 general-purpose I/O lines with interrupt capability
FCC1 does not support 16-bit UTOPIA 16	FCC1 support for 16-bit UTOPIA 16 (ATM)
FCC2 does not support UTOPIA 8	FCC2 support for UTOPIA 8 (ATM)
FCC3 works only in TDM mode	FCC3 available to external pins (NMSI)
SCC3/SCC4 work only in TDM mode	SCC3/SCC4 available to external pins (NMSI)
No support for $\overline{\text{L1RQ}}$ and L1CLK0 pins	Support for $\overline{\text{L1RQ}}$ and L1CLK0 pins (TDM)
No support for $\overline{\text{REJECT}}$ AND $\overline{\text{RSTRT}}$ pins from SCC1/SCC2 (Ethernet mode)	Support for $\overline{\text{REJECT}}$ AND $\overline{\text{RSTRT}}$ pins (SCC1/SCC2: Ethernet mode)

2 PIO Ports

Table 2 lists the number of PIO port pins available on the MSC8101 and the MPC8260, the general-purpose I/O (GPIO) ports common to both processors, and the I/O ports not present in the MSC8101. The MSC8101 supports 66 PIO ports versus 120 for the MPC8260.

Note: Use caution when comparing the MSC8101 and MPC8260 PIO pins since not all common pins share the same communication peripherals.

Table 2. MSC8101 Versus MPC8260 PIO Ports

Port	Number of MSC8101 Pins	Number of MPC8260 Pins	Common General-Purpose I/O Ports	I/O Ports Not Present on the MSC8101
Port A	26	32	PA[31–6]	PA[5–0]
Port B	14	28	PB[31–18]	PB[17–4]
Port C	18	32	PC[31–22] PC[15–12] PC[7–4]	PC[21–16], PC[11–8], PC[3–0
Port D	8	28	PD[31–29] PD[19–16] PD7	PD[28–20], PD[15–8], PD[6–4]
Total PIO Pins	66	120		

Both processors use similar die (internal logic) for the CPM, but not all of the MPC8260 port I/O pins are present on the MSC8101. For example, both the MSC8101 and the MPC8260 support four Serial Communications Controllers (SCCs) and three Fast Communication Controllers (FCCs), but the MSC8101 has dedicated pins only for SCC1/SCC2 and FCC1/FCC2. On the MSC8101, the functionality of SCC3, SCC4, and FCC3 is accessible only through the Time-Slot Assigner (TSA) block and time-division multiplexed (TDM) pins (refer to **Section 3**, *CPM Multiplexing Logic*). **Table 3** lists the number of communication controllers available on the MSC8101 and MPC8260 CPMs.

Table 3. MSC8101 Versus MPC8260 Communication Controllers

Communication Controller	MSC8101	MPC8260
FCC	3[1]	3
SCC	4[1]	4

Table 3. MSC8101 Versus MPC8260 Communication Controllers

Communication Controller	MSC8101	MPC8260
SMC	2	2
SPI	1	1
I^2C	1	1
MCC[2]	2	2

Notes: **1.** One FCC and two SCCs are only available through the TDM ports.
2. MCC is available through the TDM ports.

3 CPM Multiplexing Logic

Figure 2 depicts the MSC8101 CPM multiplexing logic. Notice that SCC3, SCC4, and FCC3 work only with the TSA and no dedicated pins are available on the non-multiplexed serial interface (NMSI). The MPC8260 supports SCC3, SCC4, and FCC3 through multiplexors to the NMSI pins. The MPC8260 also has more TDMs and TDM signals, as explained in **Section 4**, *Time-Division Multiplexing*.

4 Time-Division Multiplexing

The MSC8101 has four TDM interfaces as compared to eight on the MPC8260:

- MSC8101: **TDMA1**, **TDMB2**, **TDMC2**, **TDMD2**
- MPC8260: **TDMA1**, TDMB1, TDMC1, TDMD1, TDMA2, **TDMB2**, **TDMC2**, **TDMD2**

The “1” or “2” at the end of the TDM interface names indicates the serial interface (SI) to which it belongs: SI1 or SI2. TDMA1 and TDMA2 are special in that they support both bit and nibble modes. All of the other TDM ports support only bit mode. Since the MSC8101 has TDMA1, it can support both bit and nibble modes. The MSC8101 does not support TDMA2. TDMA1 was chosen over TDMA2 for performance reasons. This allows one TDM interface for SI1 and three TDM interfaces for SI2.

The MSC8101 does not support the $\overline{\text{L1RQ}}$ and L1CLK0 pins on the TDMs. The $\overline{\text{L1RQ}}$ output pin is used to support Interchip Digital Link (IDL), which is asserted when there is data to transmit on the ISDN D channel. The L1CLK0 output pin clocks devices that do not interface directly to the general circuit interface (GCI) in ISDN applications.

5 $\overline{\text{REJECT}}$ and $\overline{\text{RSTRT}}$ Pins

The MSC8101 does not support the $\overline{\text{REJECT}}$ and $\overline{\text{RSTRT}}$ pins on SCC1 and SCC2. On the MPC8260, these pins support an external Ethernet Content-Addressable Memory (CAM). The MPC8260 outputs a receive start ($\overline{\text{RSTRT}}$) signal when the start frame delimiter is recognized. The receive $\overline{\text{REJECT}}$ signal from the CAM tells the MPC8260 to reject the current receive frame, due to a possible collision.

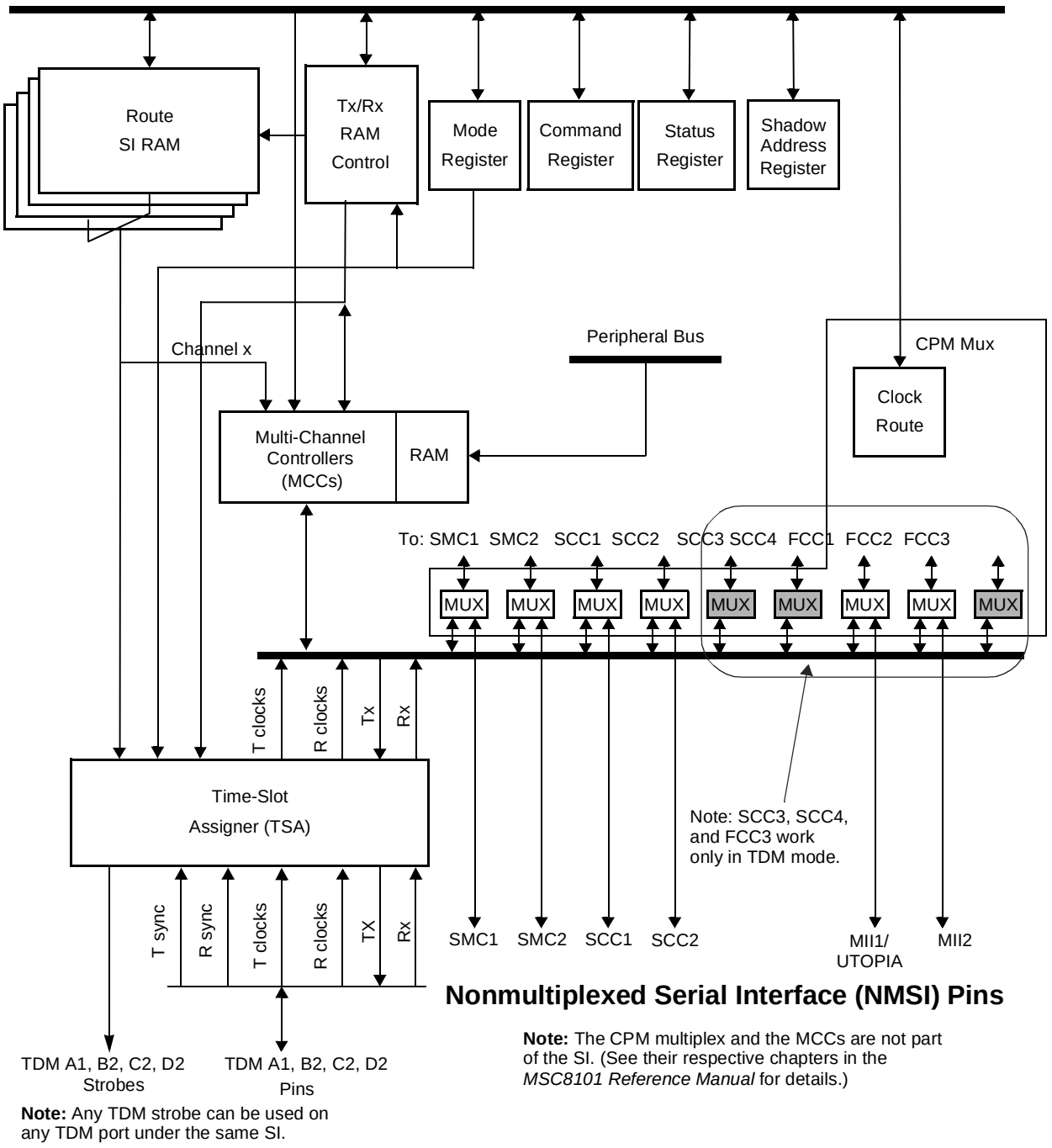


Figure 2. MSC8101 CPM Multiplexing Logic Block Diagram

6 Interrupts

The MSC8101 supports eight GPIO lines with interrupt capability as compared to 16 for the MPC8260. In addition, the MSC8101 supports seven IRQs as compared to eight for the MPC8260. The IRQs are supported by the SIU module, not the CPM, and hence are not categorized as a PIO port. **Table 4** shows the pin names for the PIO with interrupt capability and the IRQ lines.

Table 4. Interrupt Lines

Description	MSC8101	MPC8260
PIO with interrupt capability	PC[4–7], PC[12–15]	PC[0–15]
IRQs	$\overline{\text{IRQ}}$[1–7]	$\overline{\text{IRQ}}$[0–7]

7 External Pins

Table 5 through **Table 8** list and contrast the functionality of the CPM external pins (Ports A–D) on the MSC8101 and MPC8260. For details on the MSC8101 and MPC8260 pins, refer to the "External Signals" chapter in the *MSC8101 Reference Manual* and *MPC8260 User's Manual*, respectively.

Note: If the functionality on an MSC8101 pin is the same as on the MPC8260 pin, the programming may still be different. Refer to the *Dedicated Pin Assignment* tables in the "Parallel I/O Ports" chapter in the *MSC8101 Reference Manual* and *MPC8260 User's Manual*.

Table 5. MSC8101 Versus MPC8260 Port A Pins[1]

Pin Number	MSC8101 Pin Functions	MPC8260 Pin Functions
PA31	FCC1: UTOPIA 8 $\overline{\text{TXENB}}$ (m/s)[2], MII COL	FCC1: UTOPIA[3] $\overline{\text{TxENB}}$ (m/s), MII COL
PA30	FCC1: UTOPIA 8 TXCLAV (m/s), $\overline{\text{RTS}}$, MII CRS	FCC1: UTOPIA TxClav (m/s), $\overline{\text{RTS}}$, MII CRS
PA29	FCC1: UTOPIA 8 TXSOC (m/s), MII TX_ER	FCC1: UTOPIA TxSOC (m/s), MII TX_ER
PA28	FCC1: UTOPIA 8 $\overline{\text{RXENB}}$ (m/s), MII TX_EN	FCC1: UTOPIA $\overline{\text{RxEnb}}$ (m/s), MII TX_EN
PA27	FCC1: UTOPIA 8 RXSOC (m/s), MII RX_DV	FCC1: UTOPIA RxSOC (m/s), MII RX_DV
PA26	FCC1: UTOPIA 8 RXCLAV (m/s), RXCLAV0[4], MII RX_ER	FCC1: UTOPIA RxClav (m/s), RxClav[0], MII RX_ER
PA25	FCC1: UTOPIA 8 TXD0 MSNUM0	FCC1: UTOPIA 8 TxD[0], MSNUM[0] FCC1: UTOPIA 16 TxD[8]
PA24	FCC1: UTOPIA 8 TXD1 MSNUM1	FCC1: UTOPIA 8 TxD[1] MSNUM[1] FCC1: UTOPIA 16 TxD[9]
PA23	FCC1: UTOPIA 8 TXD2	FCC1: UTOPIA 8 TxD[2] FCC1: UTOPIA 16 TxD[10]
PA22	FCC1: UTOPIA 8 TXD3	FCC1: UTOPIA 8 TxD[3] FCC1: UTOPIA 16 TxD[11]
PA21	FCC1: UTOPIA 8 TXD4 FCC1: MII/HDLC nibble TXD3	FCC1: UTOPIA 8 TxD[4] FCC1: MII/HDLC nibble TxD[3] FCC1: UTOPIA 16 TxD[12]
PA20	FCC1: UTOPIA 8 TXD5 FCC1: MII/HDLC nibble TXD2	FCC1: UTOPIA 8 TxD[5] FCC1: MII/HDLC nibble TxD[2] FCC1: UTOPIA 16 TxD[13]

Table 5. MSC8101 Versus MPC8260 Port A Pins[1] (Continued)

Pin Number	MSC8101 Pin Functions	MPC8260 Pin Functions
PA19	FCC1: UTOPIA 8 TXD6 FCC1: MII/HDLC nibble TXD1	FCC1: UTOPIA 8 TxD[6] FCC1: MII/HDLC nibble TxD[1] FCC1: UTOPIA 16 TxD[14]
PA18	FCC1: UTOPIA 8 TXD7 FCC1: MII/HDLC nibble TXD0 FCC1: HDLC serial/transp TXD	FCC1: UTOPIA 8 TxD[7] FCC1: MII/HDLC nibble TxD[0], HDLC serial/transp TxD FCC1: UTOPIA 16 TxD[15]
PA17	FCC1: UTOPIA 8 RXD7 FCC1: MII/HDLC nibble RXD0 FCC1: HDLC serial/transp RXD	FCC1: UTOPIA 8 RxD[7] FCC1: MII/HDLC nibble RxD[0], HDLC serial/transp RxD FCC1: UTOPIA 16 RxD[15]
PA16	FCC1: UTOPIA 8 RXD6 FCC1: MII/HDLC nibble RXD1	FCC1: UTOPIA 8 RxD[6] FCC1: MII/HDLC nibble RxD[1] FCC1: UTOPIA 16 RxD[14]
PA15	FCC1: UTOPIA 8 RXD5 FCC1: MII/HDLC nibble RXD2	FCC1: UTOPIA 8 RxD[5] FCC1: MII/HDLC nibble RxD[2] FCC1: UTOPIA 16 RxD[13]
PA14	FCC1: UTOPIA 8 RXD4 FCC1: MII/HDLC nibble RXD3	FCC1: UTOPIA 8 RxD[4] FCC1: MII/HDLC nibble RxD[3] FCC1: UTOPIA 16 RxD[12]
PA13	FCC1: UTOPIA 8 RXD3 MSNUM2	FCC1: UTOPIA 8 RxD[3] MSNUM[2] FCC1: UTOPIA 16 RxD[11]
PA12	FCC1: UTOPIA 8 RXD2 MSNUM3	FCC1: UTOPIA 8 RxD[2] MSNUM[3] FCC1: UTOPIA 16 RxD[10]
PA11	FCC1: UTOPIA 8 RXD1 MSNUM4	FCC1: UTOPIA 8 RxD[1] MSNUM[4] FCC1: UTOPIA 16 RxD[9]
PA10	FCC1: UTOPIA 8 RXD0 MSNUM5	FCC1: UTOPIA 8 RxD[0] MSNUM[5] FCC1: UTOPIA 16 RxD[8]
PA9	SMC2: SMTXD TDMA1:L1TXD0	SMC2: SMTXD TDMA1:L1TxD[0]
PA8	SMC2: SMRXD TDMA1: L1RXD0, L1RXD	SMC2: SMRXD TDMA1: L1RxD[0], L1RxD
PA7	SMC2: $\overline{\text{SMSYN}}$ TDMA1: L1TSYNC/GRANT	SMC2: $\overline{\text{SMSYN}}$ TDMA1: L1TSYNC/GRANT
PA6	TDMA1: L1RSYNC	TDMA1: L1RSYNC
PA5	No pin	SCC2:RSTRT FCC2: MPHY RxAddr[2] IDMA4:DREQ
PA4	No pin	FCC2: MPHY RxAddr[1] SCC2: REJECT IDMA4: DONE
PA3	No pin	FCC2: MPHY RxAddr[0] CLK19 IDMA4: DACK TDMA2: L1RXD[1]
PA2	No pin	FCC2: MPHY TxAddr[0] CLK20 IDMA3: DACK

Table 5. MSC8101 Versus MPC8260 Port A Pins[1] (Continued)

Pin Number	MSC8101 Pin Functions	MPC8260 Pin Functions
PA1	No pin	FCC2: MPHY TxAddr[1] SCC1: REJECT IDMA3:DONE
PA0	No pin	SCC1:RSTRT FCC2:MPHY TxAddr[2] IDMA3:DREQ

Notes:
1. Signal name differences in this table represent differences in signal name conventions in MSC8101 and MPC8260 documentation and do not represent any functional differences.
2. m/s = master/slave.
3. UTOPIA by itself refers to both UTOPIA 8 and UTOPIA 16; the MSC8101 does not support UTOPIA 16.
4. If a master or slave is not specified, assume a master.

Table 6. MSC8101 Versus MPC8260 Port B Pins

Pin Number	MSC8101 Pin Functions	MPC8260 Pin Functions
PB31	FCC2:MII TX_ER SCC2:RXD TDMB2:L1TXD	FCC2:MII TX_ER TDMB2:L1TXD FCC2: UTOPIA RxSOC
PB30	SCC2: TXD FCC2: RX_DV TDMB2: L1RXD	FCC2: MII RX_DV TDMB2: L1RXD FCC2: UTOPIA TxSOC
PB29	FCC2: MII TX_EN TDMB2: L1RSYNC	FCC2: UTOPIA RxClav (m/s) FCC2: MII TX_EN TDMB2: L1RSYNC
PB28	FCC2: $\overline{\text{RTS}}$, MII RX_ER SCC2: $\overline{\text{RTS}}$ (TENA) TDMB2:L1TSYNC/GRANT	FCC2: $\overline{\text{RTS}}$, MII RX_ER SCC1: TXD TDMB2:L1TSYNC/GRANT
PB27	FCC2: MII COL TDMC2:L1TXD	FCC2: UTOPIA 8 TxD[0] FCC2: MII COL TDMC2:L1TXD
PB26	FCC2: MII CRS TDMC2: L1RXD	FCC2: UTOPIA 8 TxD[1] FCC2: MII CRS TDMC2: L1RXD
PB25	FCC2: MII/HDLC nibble TXD3 TDMA2: L1TXD3 TDMC2: L1TSYNC/GRANT	FCC2: UTOPIA 8 TxD[4] FCC2: MII/HDLC nibble TxD[3] TDMA1: L1TXD[3] TDMC2: L1TSYNC/GRANT
PB24	FCC2: MII/HDLC nibble TXD2 TDMA1: L1RXD3 TDMC2: L1RSYNC	FCC2: UTOPIA 8 TxD[5] FCC2: MII/HDLC nibble TxD[2] TDMA1: L1RXD[3] TDMC2: L1RSYNC
PB23	FCC2: MII/HDLC nibble TXD1 TDMA1: L1RXD2 TDMD2: L1TXD	FCC2: UTOPIA 8 TxD[6] FCC2: MII/HDLC nibble TxD[1] TDMA1:L1RXD[2] TDMD2:L1TXD

Table 6. MSC8101 Versus MPC8260 Port B Pins (Continued)

Pin Number	MSC8101 Pin Functions	MPC8260 Pin Functions
PB22	FCC2: MII/HDLC nibble TXD0 FCC2: HDLC serial/transp TXD TDMA1: L1RXD1 TDMD2: L1RXD	FCC2: UTOPIA 8 TxD[7] FCC2: MII/HDLC nibble TxD[0] FCC2: HDLC serial/transp TxD TDMA1:L1RXD[1] TDMD2: L1RXD
PB21	FCC2: MII/HDLC nibble RXD0 FCC2: HDLC/transp RXD TDMA1: L1TXD2 TDMD2: L1TSYNC/GRANT	FCC2: UTOPIA 8 RxD[7] FCC2: MII/HDLC nibble RxD[0] FCC2: HDLC/transp RxD TDMA1:L1TXD[2] TDMD2: L1TSYNC/GRANT
PB20	FCC2: MII/HDLC nibble RXD1 TDMA1: L1TXD1 TDMD2: L1RSYNC	FCC2: UTOPIA 8 RxD[6] FCC2: MII/HDLC nibble RxD[1] TDMA1:L1TXD[1] TDMD2:L1RSYNC
PB19	FCC2: MII/HDLC nibble RXD2 I^2C: SDA	FCC2: UTOPIA 8 RxD[5] FCC2: MII/HDLC nibble RxD[2] TDMD2: L1RQ TDMA2: L1RXD[3]
PB18	FCC2: MII/HDLC nibble RXD3 I^2C: SCL	FCC2: UTOPIA 8 RxD[4] FCC2: MII/HDLC nibble RxD[3] TDMD2:L1CLK0 TDMA2: L1RXD[2]
PB17	No pin	TDMA1: L1RQ FCC3: MII RX_DV CLK17
PB16	No pin	TDMA1:L1CLK0 FCC3: MII RX_ER CLK18
PB15	No pin	FCC3: MII TX_ER SCC2: RXD TDMC1: L1TXD
PB14	No pin	FCC3: TX_EN SCC3: RXD TDMC1: L1RXD
PB13	No pin	TDMB1: L1RQ FCC3: MII COL TDMA2: L1TXD[1] TDMC1: L1TSYNC
PB12	No pin	TDMB1: L1CLK0 FCC3: MII CRS SCC2: TXD TDMC1: L1RSYNC
PB11	No pin	FCC2: UTOPIA 8 TxD[0] FCC3: MII/HDLC nibble RxD[3] TDMD1: L1TXD
PB10	No pin	FCC2: UTOPIA 8 TxD[1] FCC3: MII/HDLC nibble RxD[2 TDMD1: L1RXD

Table 6. MSC8101 Versus MPC8260 Port B Pins (Continued)

Pin Number	MSC8101 Pin Functions	MPC8260 Pin Functions
PB9	No pin	FCC2: UTOPIA 8 TxD[2] FCC3: MII/HDLC nibble RxD[1] TDMA2: L1TXD[2] TDMD1: L1TSYNC
PB8	No pin	FCC2: UTOPIA 8 TxD[3] FCC3: MII/HDLC nibble RxD[0] FCC3: HDLC/transp RxD SCC3: TXD TDMD1: L1RSYNC
PB7	No pin	FCC3: MII/HDLC nibble TXD[0] FCC3: HDLC/transp TXD FCC2: UTOPIA 8 RxD[3] TDMA2: L1TXD[0], L1TXD
PB6	No pin	FCC3: MII/HDLC nibble TXD[1] FCC2: UTOPIA 8 RxD[2] TDMA2: L1RXD, L1RXD[0]
PB5	No pin	FCC3: MII/HDLC nibble TXD[2] FCC2: UTOPIA 8 RxD[1] TDMA2: L1TSYNC
PB4	No pin	FCC3: MII/HDLC nibble TXD[3] FCC2: UTOPIA 8 RxD[0] FCC3: RTS TDMA2: L1RSYNC

Notes: **1.** UTOPIA by itself refers to both UTOPIA 8 and UTOPIA 16.
2. m/s: master/slave.
3. If a master or slave is not specified, assume a master.

Table 7. MSC8101 Versus MPC8260 Port C Pins

Pin Number	MSC8101 Pin Functions	MPC8260 Pin Functions
PC31	BRG10 CLK1 Timer1/2: $\overline{\text{TGATE1}}$	BRG10 CLK1
PC30	BRG20 CLK2 Timer1: $\overline{\text{TOUT1}}$ EXT1	FCC2: UTOPIA 8 TxD[3] CLK2 Timer1: $\overline{\text{TOUT1}}$
PC29	BRG30 CLK3/$\overline{\text{TIN2}}$ SCC1: $\overline{\text{CTS}}$ (CLSN)	BRG20 CLK3/$\overline{\text{TIN2}}$ SCC1: $\overline{\text{CTS}}$ (CLSN)
PC28	BRG40 CLK4/$\overline{\text{TIN1}}$ Timer2:$\overline{\text{TOUT2}}$ SCC2: $\overline{\text{CTS}}$ (CLSN)	Timer2: $\overline{\text{TOUT2}}$ CLK4/$\overline{\text{TIN1}}$ SCC2: $\overline{\text{CTS}}$ (CLSN)
PC27	BRG50 CLK5 Timer3/4: $\overline{\text{TGATE2}}$	FCC3: HDLC serial/transp TxD FCC3: MII/HDLC nibble TxD[0] CLK5 BRG30

Table 7. MSC8101 Versus MPC8260 Port C Pins (Continued)

Pin Number	MSC8101 Pin Functions	MPC8260 Pin Functions
PC26	BRG60 CLK6 Timer3: TOUT3 TMCLK	Timer3: TOUT3 CLK6 TMCLK
PC25	BRG70 CLK7/TIN4 DMA2: DACK2	FCC2: UTOPIA 8 TxD[2] CLK7 BRG40
PC24	BRG80 CLK8/TIN3 Timer4: TOUT4 DMA2: DREQ2	FCC2: UTOPIA 8 TxD[3] CLK8 Timer4:TOUT4
PC23	CLK9 DMA1: DACK1 EXT2	BRG50 CLK9 IDMA1: DACK1
PC22	SI1:L1ST1 CLK10 DMA1:DREQ1	CLK10 IDMA1: DONE1
PC21	No pin	BRG60 CLK11
PC20	No pin	CLK12 timer 1/2: TGATE1
PC19	No pin	BRG70 CLK13
PC18	No pin	CLK14 timer 3/4: TGATE2
PC17	No pin	BRG80 CLK15/TIN4
PC16	No pin	CLK16/TIN3
PC15	SMC2:SMTXD SCC1: CTS (CLSN) FCC1: MPHY TXADDR0 (m/s)	SMC2:SMTXD SCC1: CTS (CLSN) FCC1: MPHY TxAddr[0] (m/s) FCC2: MPHY TxAddr[4] slave
PC14	SI1:L1ST2 SCC1: CD (RENA) FCC1: MPHY RXADDR0 (m/s)	SCC1: CD (RENA) FCC1: MPHY RxAddr[0] (m/s) FCC2: MPHY RxAddr[4] (slave)
PC13	SI1:L1ST4 SCC2:CTS (CLSN) FCC1: MPHY TXADDR1 (m/s)	TDMD1: L1RQ SCC2: CTS (CLSN) FCC1: MPHY TxAddr[1] (m/s) FCC2: MPHY TxAddr[3] (slave)
PC12	S1:L1ST3 SCC2: CD (RENA) FCC1: MPHY RXADDR1 (m/s)	SI1: L1ST3 SCC2: CD (RENA) FCC1: MPHY RxAddr[1] (m/s) FCC2: MPHY RxAddr[3] (slave)
PC11	No pin	TDMD1: L1CLK0 SCC3: CTS (CLSN) TDMA2: L1TXD[3] FCC2: UTOPIA 8 RxD[2]

Table 7. MSC8101 Versus MPC8260 Port C Pins (Continued)

Pin Number	MSC8101 Pin Functions	MPC8260 Pin Functions
PC10	No pin	FCC1: UTOPIA 16 TxD[2] SCC3: CD (RENA) SI1: L1ST4 FCC2: UTOPIA 8 RxD[3]
PC9	No pin	FCC1: UTOPIA 16 TxD[1] SCC4: CTS (CLSN) SI2: L1ST1 TDMA2: L1TSYNC
PC8	No pin	FCC1: UTOPIA 16 TxD[0] SCC4: CD (RENA) SI2: L1ST2 SCC3: CTS
PC7	SI2:L1ST1 FCC1: CTS FCC1: MPHY TXADDR2 (m/s) FCC1: TxClav1	TDMC1: L1RQ FCC1: CTS FCC1: MPHY TxAddr[2] (m/s) FCC1: MPHY TxClav1 FCC2: MPHY TxAddr[2] (slave)
PC6	SI2:L1ST2 FCC1: CD FCC1: MPHY RXADDR2 (m/s) FCC1: MPHY RXCLAV1	TDMC1: L1CLK0 FCC1: CD FCC1: MPHY RxAddr[2] (m/s) FCC1: MPHY RXcLAV1 FCC2: MPHY RxAddr[2] slave
PC5	SMC1: SMTXD SI2: L1ST3 FCC2: CTS	FCC2: TxClav UTOPIA (m/s) SI2: L1ST3 FCC2: CTS
PC4	SMC1: SMRXD SI2: L1ST4 FCC2: CD	FCC2: UTOPIA RxEnb (m/s) SI2: L1ST4 FCC2: CD
PC3	No pin	FCC2: UTOPIA 8 TxD[2] FCC3: CTS IDMA2: DACK2 SCC4: CTS
PC2	No pin	FCC2: UTOPIA 8 TxD[3] FCC3: CD IDMA2: DONE2
PC1	No pin	BRG60 IDMA2: DREQ TDMA2: L1RQ
PC0	No pin	BRG70 IDMA1: DREQ TDMA2: L1CLK0 SMC2: SMSYN

Notes:
1. UTOPIA by itself refers to both UTOPIA 8 and UTOPIA 16.
2. m/s: master/slave.
3. If a master or slave is not specified, assume a master.
4. BRGx0: Baud-Rate Generator x Output.

Table 8. MSC8101 Versus MPC8260 Port D Pins

Pin Number	MSC8101 Pin Functions	MPC8260 Pin Functions
PD31	SCC1: RXD DMA1: DRACK1 DMA1: DONE1	SCC1: RXD
PD30	SCC1: TXD DMA2: DRACK2 DMA2: DONE2	FCC2: UTOPIA TxEnb (m/s) SCC1: TXD
PD29	SCC1: RTS (TENA) FCC1: MPHY RXADDR3 (m/s) FCC1: MPHY RXCLAV2	SCC1: RTS (TENA) FCC1: MPHY RxAddr[3] (m/s) FCC1: MPHY RxClav2 FCC2: MPHY RxAddr[4] FCC2: MPHY RxAddr[1] slave
PD28	No pin	FCC1: UTOPIA 16 TxD[7] SCC2: RXD TDMC1: L1TXD
PD27	No pin	SCC2: TXD FCC1 UTOPIA 16 RxD[7] TDMC1: L1RXD
PD26	No pin	SCC2: RTS (TENA) FCC1: UTOPIA 16 RxD[6] TDMC1: L1RSYNC3
PD25	No pin	FCC1: UTOPIA 16 TxD[6] SCC3: RXD TDMD1:L1TXD
PD24	No pin	SCC3: TXD FCC1: UTOPIA 16 RxD[5] TDMD1: L1RXD
PD23	No pin	SCC3: RTS (TENA) FCC1: UTOPIA 16 RxD[4] TDMD1: L1RSYNC
PD22	No pin	FCC1: UTOPIA 16 TxD[5] SCC4: RXD TDMA2: L1TXD[0], L1TXD
PD21	No pin	SCC4: TXD FCC1: UTOPIA 16 RxD[3] TDMA2: L1RXD, L1RXD[0]
PD20	No pin	SCC4: RTS (TENA) FCC1: UTOPIA 16 RxD[2] TDMA2: L1RSYNC
PD19	FCC1: MPHY TXADDR4 (m/s) FCC1: MPHY TXCLAV3 BRG10 SPI: SPISEL	FCC1: MPHY TxAddr[4] (m/s) FCC2: MPHY TxAddr[3] FCC1: MPHY TxClav3 FC C2: MPHY TxAddr[0] slave BRG10 SPI:SPISEL
PD18	FCC1: RXADDR4 (m/s) FCC1: MPHY RXCLAV3 SPI: SPICLK	FCC1: MPHY RxAddr[4] (m/s) FCC2: MPHY RxAddr[3] FCC1: MPHY RxClav3 FCC2: MPHY RxAddr[0] slave SPI: SPICLK

Table 8. MSC8101 Versus MPC8260 Port D Pins (Continued)

Pin Number	MSC8101 Pin Functions	MPC8260 Pin Functions
PD17	BRG20 FCC1: UTOPIA RXPRTY SPI: SPIMOSI	BRG20 FCC1 UTOPIA RxPrty SPI: SPIMOSI
PD16	FCC1: UTOPIA TXPRTY SPI: SPIMISO	FCC1: UTOPIA TxPrty TDMC1:L1TSYNC SPI: SPIMISO
PD15	No pin	TDMC2: L1RQ FCC1: UTOPIA 16 RxD[1] I2C: I2CSDA
PD14	No pin	TDMC2: L1CLK0 FCC1 UTOPIA 16 RxD[0] I2C: I2CSCL
PD13	No pin	SI1: L1ST1 TDMB1: L1TXD
PD12	No pin	SI1: L1ST2 TDMB1: L1RXD
PD11	No pin	TDMB2: L1RQ FCC2: UTOPIA 8 RxD[0] TDMB1: L1TSYNC
PD10	No pin	TDMB2: L1CLK0 FCC2: UTOPIA 8 RxD[1] BRG40 TDMB1: L1RSYNC
PD9	No pin	SMC1: SMTXD BRG30 FCC2: UTOPIA RxPrty
PD8	No pin	FCC2: UTOPIA TxPrty SMC1: SMRXD BRG50
PD7	SMC1: $\overline{\text{SMSYN}}$ FCC1: MPHY TXADDR3 (m/s) FCC1: MPHY TXCLAV2	SMC1: $\overline{\text{SMSYN}}$ FCC1: MPHY TxAddr[3] (m/s) FCC2: MPHY TxAddr[4] FCC1: MPHY TxClav2 FCC2: MPHY TxAddr[1] slave
PD6	No pin	FCC1: UTOPIA 16 TxD[4] IDMA1: DACK
PD5	No pin	FCC1: UTOPIA 16 TxD[3] IDMA1: DONE
PD4	No pin	BRG80 TDMD1: L1TSYNC FCC3: RTS SMC2: SMRXD

Notes:
1. **Notes**: 1) UTOPIA by itself refers to both UTOPIA 8 and UTOPIA 16.
2. m/s: master/slave.
3. If a master or slave is not specified, assume a master.
4. BRGxO: Baud-Rate Generator x Output.

8 Channels

Table 9 shows the number of pins required and supported for each MSC8101 and MPC8260 channel. If a pin within a channel is supported on more than one pin, then the number of external pins may be higher than the required number of pins. The pin counts in **Table 9** do not include clocks.

Table 9. Number of Channel Pins Required and Supported

Channel	MSC8101 External Pins	MPC8260 External Pins	MSC8101 Required Pins	MPC8260 Required Pins
FCC1	34	50	34	50
FCC2	16	52	14	50
FCC3	0	18	0	14
SCC1	6	9	5	7
SCC2	6	10	5	7
SCC3	0	8	0	7
SCC4	0	6	0	7
SPI	4	4	4	4
I^2C	2	2	2	2
SMC1	3	3	3	3
SMC2	4	6	3	3
TDMA	10	12	10	12
TDMB	4	6	4	6
TDMC	4	6	4	6
TDMD	4	6	4	6

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