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CDMA Upmixer Design Considerations Using The MRFIC1854

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INTRODUCTION

This note focuses on designing Motorola's MRFIC1854 with Qualcomm's MSM3000 based CDMA platform. In order to achieve an excellent performance in the transmitter (Tx) chain as well as a very good production yield, a few points are strongly recommended.

DESIGN CONSIDERATIONS

In order to understand the necessity of keeping our recommendations in a successful design, let's review a typical architecture, as shown in Figure 1, of the Tx chain using in the CDMA mobile system (MS). The baseband signal from MSM3000 is first modulated into a 130 MHz IF signal by IFT3000 (Qualcomm). This modulated signal must then be band limited before up–converting to the RF transmitting frequency by the upmixer. The exciter and the power amplifier (PA) further amplify the RF signal.

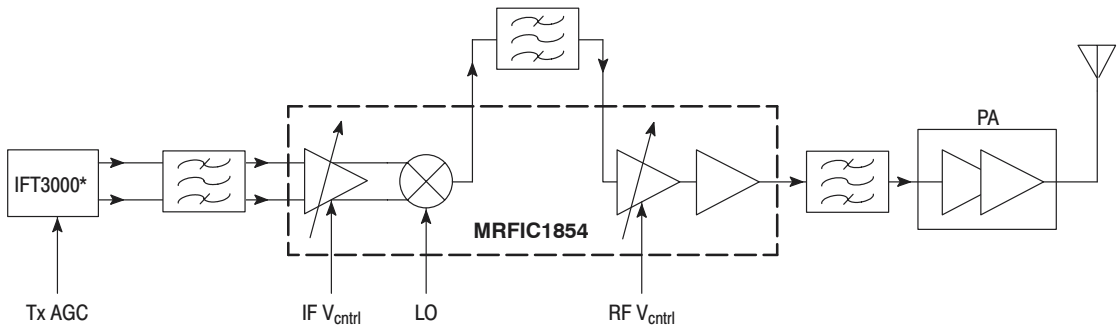
In the MS, a dynamic range (DR) as much as 85 dB must be implemented in the Tx chain in order to meet the system power control requirement. This large DR is provided by three automatic gain control (AGC) amplifiers in the Tx chain. The IFT3000 has a DR of about 84 dB which corresponds to a control voltage ranging from 0.2 to 2.3 V. The two AGC amplifiers in MRFIC1854 have a total DR of about 65 dB with a control voltage ranging from 0.1 to 1.7 V. Based on the power control algorithm (both open and closed loops), the MSM3000 outputs a pulse density modulation (PDM) control signal to adjust the Tx gain.

In order to get the best performance, the total Tx gain must be distributed properly among these three AGC amplifiers. Too much gain in the IFT3000 results in low adjacent channel power rejection (ACPR) problem whereas too little gain results in excess noise issue. To improve the noise performance, it is also recommended to insert an IF SAW filter prior to the upmixer.

To achieve better signal–to–noise ratio (SNR) and ACPR, the IFT3000 is usually operated in the high output power region of its DR because both SNR and ACPR increase with the output power. To prevent the IF AGC amplifier and the upmixer in MRFIC1854 from saturation, an IF attenuator prior to the upmixer must be used if more attenuation is required.

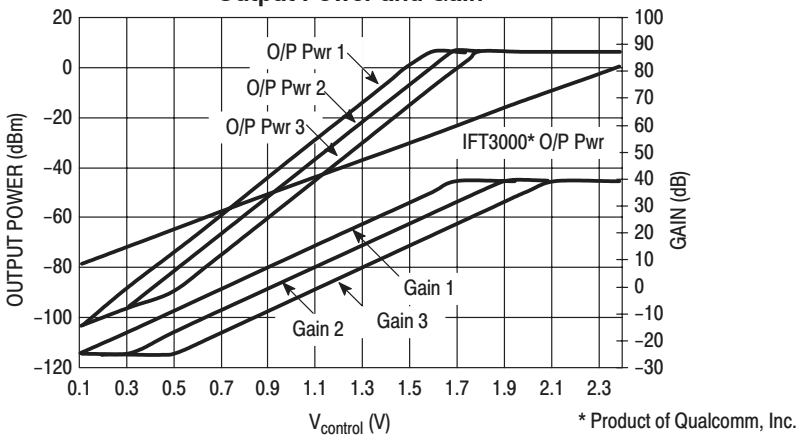
However, the gain control issue is complicated by the following facts. Firstly, there is normally only one AGC control pin available from the MSM3000 baseband processor. Secondly, the AGC characteristics of IFT3000 and MRFIC1854 have different gain slopes. These two points imply that three AGC amplifiers cannot be controlled independently even though level shifters are used to provide adequate control voltage ranges for different AGC amplifiers. In other words, the three AGC voltages are one to one mapped to each other. As a result, any gain tolerance in any AGC amplifier may adversely affect the pre–designed Tx gain budget. For example, the IFT3000 needs to drive harder in case of a low gain upmixer, which in turn, causes ACPR problem due to overdriving the upmixer. The attenuation network must therefore be designed with enough margins.

Figure 1. System Block Diagram of the Tx Chain in a CDMA MS



* Product of Qualcomm, Inc.

Figure 2. IFT3000 & MRFIC1854 Output Power and Gain



* Product of Qualcomm, Inc.

Thirdly, MRFIC1854 is designed to be used over its entire dynamic range, limiting the device to operate in the linear portion of the AGC curve can result in higher overall Tx gain variation. Figure 2 shows the typical AGC curves of MRFIC1854. It is apparent that there is about +8.0 dB gain variation in the middle of the AGC curve compared to about +1.0 dB gain variation at two ends. This suggests that the whole DR of MRFIC1854 must be utilized to allow the AGC loop to adjust the total Tx gain by itself dynamically. Limiting the usable AGC range of MRFIC1854 can result in lack of output power and/or amplifier saturation in case of low gain devices. The level shifting circuits for MRFIC1854 must be designed in such a way to cover entire AGC range, i.e. from 0.1 to 1.7 V. It is not recommended to apply a fixed control voltage in the transition region of any AGC amplifier neither. This can enlarge the effect of gain variation.

Lastly, the Tx AGC nonlinearity compensation algorithm adopted by MSM3000 places another constraint upon the Tx AGC design. In this platform, the TX AGC curve is piece–wisely linearized into 16 linear segments with each segment representing by a linear equation in the form of y = mx + c where m is the slope and c is the offset of each segment, as depicted in Figure 3. The values of m (7 bits) and c (9 bits) are found in the Tx power calibration and are stored in the sixteen 16–bit words in RAS_RAM of MSM3000. With a six–bit input x ranging from 0/64 to 63/64, the resulting AGC control (TX_AGC_ADJ) is a 9–bit PDM signal. This suggests there is at most 512 gain steps in the entire AGC DR. The gain slope must be carefully chosen. These 16 linearized line segments compensate any nonlinearity in the AGC characteristics to produce a net linear AGC amplifier gain curve.

The effect of device gain variation in any block in the Tx chain causes the open loop gain characteristics shifting in the x–direction, for example, any low gain device results in the entire open loop gain curve shifting to the right side. As a consequence, a larger PDM output value must be generated in order to produce the same output power level. In practice, as long as the gains at two ends of the open loop AGC curve remain unchanged, any gain variation in the transition part of any AGC amplifier can be cancelled out after calibration. However, it is to remind that the Tx gain budget will be adversely affected as explained before. In case, only part of the AGC curve of MRFIC1854 is covered, there may be chance that some low gain devices cannot produce the maximum output power even though the maximum PDM code is input.

Figure 3. Linearized PDM Output

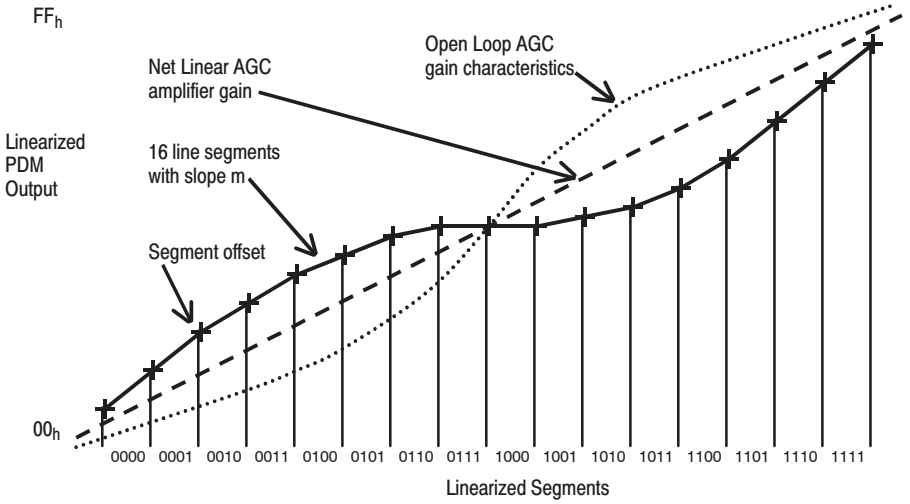
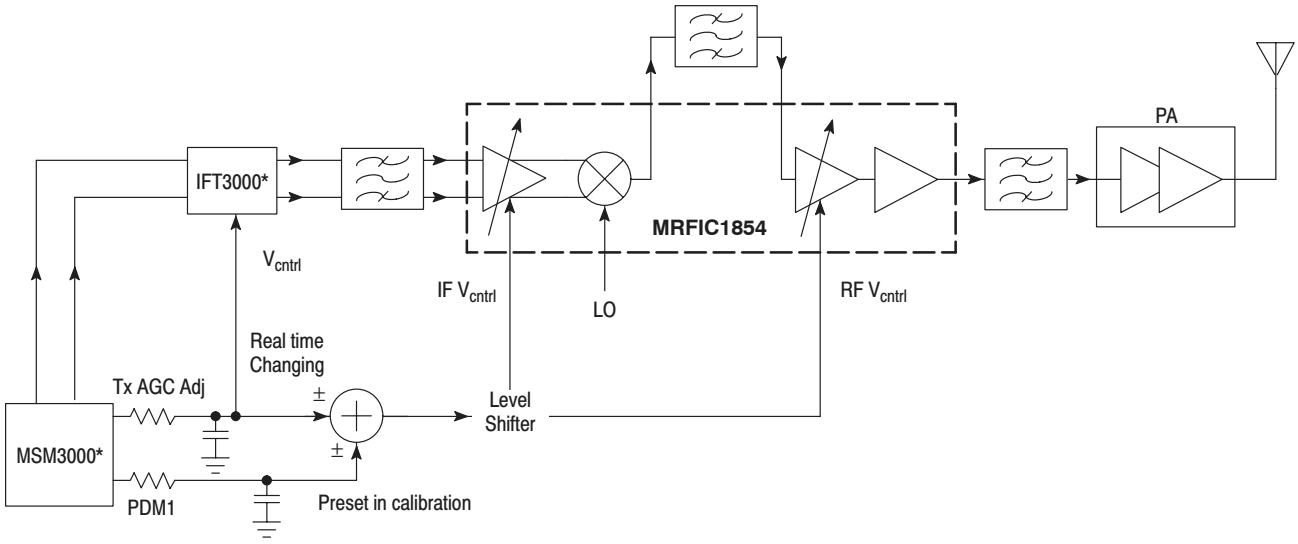


Figure 4. Improved System Block Diagram of the Tx Chain in a CDMA MS



To handle this issue, one of the solutions is to add one more control signal in the Tx AGC scheme, as described in Figure 4. An additional PDM output (“PDM1” or “PDM2”) is used for providing a DC signal to the AGC amplifiers, say MRFIC1854, to trim the Tx AGC curve back to the preset position by simply adding this PDM voltage with the TX_AGC_ADJ output. This trimming voltage is found in the Tx power calibration, which is then converted back to the PDM output signal. The corresponding PDM output value is stored in MSM3000 permanently. This method has the advantages of reducing the harmful effect of gain variation of individual device, less disturbance to the Tx gain budget and more accurate Tx power calibration. On the other hand, those advantages are at the expense of MSM3000 control software modification, calibration program modification as well as a little longer calibration time. Additional components may or may not be required because most of the current designs have incorporated an OPAMP for level shifting already. To save the calibration time, the additional PDM output can be normally set to zero. Additional calibration is only done for those failure MS.

No matter using the suggested Tx AGC scheme or not, in designing the level shifting networks, data should collected in the gain characteristics of both IFT3000 and MRFIC1854, as well as the gain variation in the PA. The gain variation data can provide a big picture of how the gains vary from device to device basis. With the consideration of the tolerance data, proper level shifting circuits can be designed with enough margins to cover the gain variation of the AGC amplifiers and to minimize the impact of gain tolerance to the production yield.

REFERENCE

MRFIC1854A Data Sheet: 1.9 GHz CDMA Upmixer/Exciter

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