



How to Configure a MPC860 System (1 of 4)

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	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	LITCLKB TOUT4* CLK8 PA0	TIN4 BRGO4 CLK7 PA1	LIRCLKB TOUT3* CLK6 PA2	TIN3 BRGO3 CLK5 PA3	TOUT2* CLK4 PA4	TIN2 LITCLKA BRGO2 CLK3 PA5	TOUT1* CLK2 PA6	TIN1 LIRCLKA BRGO1 CLK1 PA7	LIRXDA PA8	LITXDA PA9	LIRXDB PA10	LITXDB PA11	TXD2 PA12	RXD2 PA13	TXD1 PA14	RXD1 PA15
SCC1																
NMSI																
SCC2																
NMSI																
SCC3																
NMSI																
SCC4																
NMSI																
TDMa																
TDMb																
SMC1																
SMC2																
SPI																
Ethnet																
CAM																
Timer																
1																
Timer																
2																
Timer																
3																
Timer																
4																
IDMA																
1																
IDMA																
2																
I2C																
PIP																

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PADAT																
PAODR	0	0	0	0	0	0	0	0	0		0			0		0
PADIR																
PAPAR																

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14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

	STRBI RSTR1* PB14	STRBO BRGO3 PB15	LIST4 LIRQA* PB16	LIST3 LIRQB* PB17	LIST2 RTS2* PB18	LIST1 RTS1* PB19	LJCLK0A SMRXD2 PB20	LJCLK0B SMTXD2 PB21	SDACK2* SMSYN2* PB22	SDACK1* SMSYN1* PB23	SMRXD1 PB24	SMTXD1 PB25	I2CSCL BRGO2 PB26	I2CSDA BRGO1 PB27	BRGO4 SPIMISO PB28	SPIMOSI PB29	SPICLK PB30	RRJCT1* SPISEL* PB31
SCC1 NMSI		/			/													
SCC2 NMSI		/			/													
SCC3 NMSI		/																
SCC4 NMSI		/																
TDMa		/	/	/	/													
TDMb		/	/	/	/													
SMC1																		
SMC2																		
SPI																		
Ethnet CAM																		
Timer 1																		
Timer 2																		
Timer 3																		
Timer 4																		
IDMA 1																		
IDMA 2																		
I2C																		
PIP																		

14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31

PBDAT																		
PBODR																		
PBDIR																		
PBPAR																		

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	4	5	6	7	8	9	10	11	12	13	14	15
	L1RSYNCA* CD4* PC4	SDACK1* L1TSYNCA* CTS4* PC5	L1RSYNCB* CD3* PC6	SDACK2* L1TSYNCB* CTS3* PC7	TGATE2* CD2* PC8	CTS2* PC9	TGATE1* CD1* PC10	CTS1* PC11	L1ST4 L1RQA* PC12	L1ST3 L1ROB* PC13	L1ST2 RTS2* DREQ2 PC1	L1ST1 RTS1* DREQ1 PC0
SCC1												
NMSI												
SCC2												
NMSI												
SCC3												
NMSI												
SCC4												
NMSI												
TDMa												
TDMb												
SMC1												
SMC2												
SPI												
Ethnet												
CAM												
Timer												
1												
Timer												
2												
Timer												
3												
Timer												
4												
IDMA												
1												
IDMA												
2												
I2C												
PIP												

	4	5	6	7	8	9	10	11	12	13	14	15
PCDAT												
PCDIR												
PCPAR												
PCSO												
PCINT												

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	3	4	5	6	7	8	9	10	11	12	13	14	15
	RRJCT4 SDACK2 PD3	RRJCT3 SDACK1 PD4	RRJCT2 PD5	RTS4* PD6	RTS3* PD7	TXD4 PD8	RXD4 PD9	TXD3 PD10	RXD3 PD11	LIRSYNCB PD12	LITSYNCB PD13	LIRSYNCA PD14	LITSYNCA PD15
SCC1 NMSI													
SCC2 NMSI													
SCC3 NMSI													
SCC4 NMSI													
TDMa													
TDMb													
SMC1													
SMC2													
SPI													
Ethnet CAM													
Timer 1													
Timer 2													
Timer 3													
Timer 4													
IDMA 1													
IDMA 2													
I2C													
PIP													

	3	4	5	6	7	8	9	10	11	12	13	14	15
PDDAT													
PDDIR*													
PDPAR													

* PDDIR, bits 0 & 1, can be used to make PD8 and/or PD10 open drain.

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