

# PowerPC™

## *Application Note*

# DEVELOPMENT INFORMATION REGARDING MIGRATION TO SILICON REVISION B.3 OF THE MPC8260 PowerQUICC II

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## INTRODUCTION

This document highlights information which may impact customer designs that are migrating to revision B.3 silicon from previous revisions of the MPC8260. Please be aware that this is considered a “living” document and may be updated as is necessary. Customers are encouraged to take note of new editions of this document.

## ERRATA

Note that a number of device errata have been eliminated with the latest revision of silicon. This may allow the removal of workarounds in future design work with the new silicon revision. Also note that since the release of new silicon, new errata have been discovered and investigated. Customers are highly encouraged to regularly review the MPC8260 device errata document in detail to determine if or how these fixes impact their design work.

The MPC8260 device errata documentation can be located on the World Wide Web at the bottom of the following web page:

<http://www.mot.com/SPS/RISC/netcomm/support/index.html>



## RAM MICROCODES

Note the following updates regarding appropriate usage of microcode packages in relation to certain microcode revisions. Updated RAM microcodes that patch device errata are also available in the MPC8260 table located on the web at:

<http://www.mot.com/SPS/RISC/netcomm/support/index.html>

Updates of microcode packages for sale should be obtained through your usual Motorola sales contact.

- A different AAL2 microcode package is required for revision B.3 than is used on B.2.
- A different IMA microcode package is required for revision B.3 than those used in previous revisions.
- Note that when using ATM AAL1 in rev B.x devices, it is recommended that users program the RCT and TCT's AAL\_TYPE field to AAL1\_CES (b101) instead of the old regular AAL1 setting (b001) and then enable CES functionality if needed by setting the CESM field. Please see the "MPC8260 Revision B ROM Microcode Changes" document for further detail.
- Revision B.2 requires a microcode patch for ATM internal rate operation. This patch is not required for revision B.3.
- Different SS7 microcode patches are required for revision A.1 and revision B.x devices.




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