

Semiconductor Products Sector
Application Note

AN2189

Using the Clock Generation Module on the HC12 'D' Family

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1 Introduction

The M68HC912D Family of microcontrollers incorporate clock generation circuitry comprising of a low power oscillator and a phase-locked loop (PLL). For enhanced operational capability under adverse conditions there is also a clock monitor circuit, a computer operating properly (COP) watchdog and in addition, the PLL features an emergency operating mode called Limp-home mode (LHM).

The purpose of this document is to present the most commonly used configurations of the clock control registers and to outline the behaviour of the clock generation circuit in low power modes and under adverse conditions. This document should be used in conjunction with the relevant microcontroller Technical Manual.

2 Oscillator

The internal Colpitts oscillator requires external components in order to generate a clock signal. Commonly, a quartz crystal or a ceramic resonator may be used, together with a pair of load capacitors. A quartz crystal will realise a precise and stable clock frequency and for this reason they are the preferred component when the clock will be used as a base for a high frequency communications bus such as the controller area network (CAN). On the other hand, ceramic resonators are lower

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cost, and a side effect of the lower Q is that the start-up time for the oscillator is significantly shorter than for quartz crystals. Ceramic resonators are also available with integrated load capacitors which can give this component a size advantage over quartz crystals. Resonators with tight accuracy and stability are increasingly becoming available. In all cases it is highly recommended that the correct value for the load capacitors is obtained directly from the crystal/resonator manufacturer. Note that the arrangement of the external components is different from the standard Pierce circuit used on other HC12 microcontrollers. Note also that the V_{SSPLL} pin is the ground connection for the oscillator as well as the PLL and that this pin must always be connected to ground.

The common node of the crystal/resonator and capacitor should be connected directly to the V_{SSPLL} pin. In order to minimise power consumption, the oscillator contains an amplitude limitation control loop. This limits the peak-to-peak amplitude on the EXTAL pin.

The oscillator continues to run in Wait mode. In Stop mode, the oscillator is completely stopped if the PSTP bit in the PLLCR register is clear. If the PSTP bit in the PLLCR register is set, the microcontroller enters Pseudo-stop mode when the 'stop' instruction is executed. In Pseudo-stop mode all internal clocks are stopped but the oscillator continues to run. Exit from Stop mode is subject to a delay whilst the oscillator is restarted, this delay is minimised if Pseudo-stop mode is used. Although current consumption in Pseudo-stop mode is higher than Stop mode, mechanical stress and ageing of the crystal/resonator is reduced in Pseudo-stop mode.

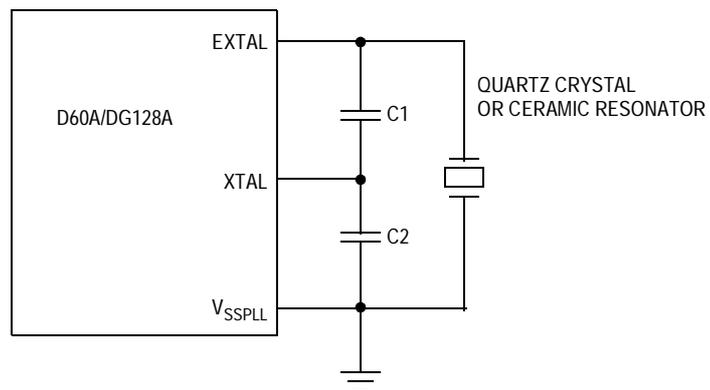


Figure 1 Oscillator Circuit

For optimum performance, the physical layout of the oscillator circuit should occupy a small area. Signal traces should be kept as short as possible. No other traces should cross below or between the oscillator components. The crystal or resonator and load capacitors should be on the same side of the board as the microcontroller to minimise the use of vias. High stability load capacitors are recommended such as multilayer ceramic with NPO or COG temperature coefficient.

3 Phase-Locked Loop

The internal PLL may be used to generate a higher clock frequency than the crystal oscillator for the microcontroller system clock. It is not allowed to generate a PCLK frequency which is lower than the crystal oscillator frequency as the operation of some internal synchronizers would be jeopardized. The V_{DDPLL} pin must be connected to V_{DD} for PLL operation. With the V_{DDPLL} pin connected to V_{DD} , the PLL is enabled at reset, but not selected as the source for SYSCLK and the PLL may be disabled/enabled under software control. The PLL is always disabled when the V_{DDPLL} pin is connected to V_{SS} . The V_{DDPLL} pin must not be left floating. The V_{SSPLL} pin must always be connected to ground as this is the ground connection for the oscillator as well as the PLL. If the PLL is to be used (V_{DDPLL} connected to V_{DD}) then external components in a second order low-pass filter configuration must be connected to the XFC pin. If the PLL is not used (V_{DDPLL} connected to V_{SS}) then the XFC pin may be left floating or connected to V_{SS} (but **not** V_{DD}). Advantages of using the PLL include:

- Increased flexibility for low power consumption strategies
 - PLL can be switched off under software control to give a lower clock frequency and lower power consumption.
- Reduced susceptibility to electromagnetic interference
 - Acts as a filter to electromagnetic interference on the oscillator.
- Reduced electromagnetic emissions
 - Short term frequency drift reduces emissions peak.
- Emergency Limp-home mode
 - Microcontroller can continue to operate even if crystal/resonator fails.

The PLL has two operating modes:

1. Acquisition Mode – In this mode a higher value of the charge pump current (approximately 40 μA) allows large corrections to the voltage controlled oscillator (VCO) frequency. This mode is used at PLL start-up when the VCO frequency is far off the target frequency.
2. Tracking Mode – In this mode the charge pump current is reduced to approximately 3 μA and only small corrections can be made to the VCO frequency.

The normal configuration for the PLL is the 'automatic bandwidth selection' which is obtained by having the AUTO bit set in the PLLCR register. In this configuration the PLL is automatically switched from acquisition mode to tracking mode as the VCO frequency approaches the target frequency. If the current leakage at the XFC pin is excessive, due to adverse environmental conditions for example, then the PLL may repetitively switch between acquisition and tracking modes. In these circumstances it is advisable to run the PLL in the manual acquisition configuration by clearing both the AUTO and ACQ bits in the PLLCR register. Doing this will maintain the higher charge pump current level constantly which will overcome higher levels of leakage on the XFC pin. The LOCK bit in the PLLFLG register is set when the VCO frequency is within tolerance of the target frequency and is an indication that the PLLCLK is safe to use as the microcontroller system clock, SYSCLK. The VCO output frequency is multiplied by 2 to create the PLLCLK frequency, so the ECLK frequency (f_{BUS}) is equal to the VCO frequency when the PLLCLK is selected for SYSCLK (BCSP bit set).

The PLL is unaffected by Wait mode, although power consumption may be reduced by switching the PLL off under software control before entering Wait mode. PLL operation is suspended in Stop and Pseudo-stop modes.

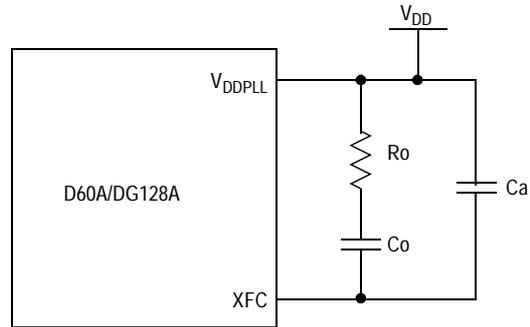


Figure 2 PLL Filter Circuit

Table 1 Suggested PLL Filter Components for Tracking/Auto Mode

f_{REF} [MHz] (Note 1)	f_{Bus} [MHz]	SYNR	Co [nF]	Ro [kΩ]	Ca [nF]	Loop Bandwidth [kHz]
1	8	\$07	10	11	1.0	4.6
1	8	\$07	2.2	24	0.22	10.0
1	8	\$07	1.0	36	0.1	15.1
1	8	\$07	0.47	51	0.047	21.4
2	8	\$03	4.7	11	0.47	9.2
2	8	\$03	1.0	24	0.1	20.1
2	8	\$03	0.47	36	0.047	30.1
2	8	\$03	0.22	51	0.022	42.7
4	8	\$01	2.2	12	0.22	20.1
4	8	\$01	0.47	24	0.047	40.2
4	8	\$01	0.22	36	0.022	60.3
4	8	\$01	0.1	56	0.01	93.8

Note 1: $f_{REF} = f_{osc} / (REFDV + 1)$

Table 2 Suggested PLL Filter Components for Acquisition/Manual Mode

f_{REF} [MHz] (Note 1)	f_{Bus} [MHz]	SYNR	Co [nF]	Ro [kΩ]	Ca [nF]	Loop Bandwidth [kHz]
1	8	\$07	100	1.1	10	5.1
1	8	\$07	22	2.2	2.2	10.1
1	8	\$07	10	3.3	1.0	15.2
1	8	\$07	4.7	4.7	0.47	21.6
2	8	\$03	47	1.1	4.7	10.1
2	8	\$03	10	2.4	1.0	22.1
2	8	\$03	4.7	3.3	0.47	30.4
2	8	\$03	2.2	5.1	0.22	46.9
4	8	\$01	22	1.1	2.2	20.2
4	8	\$01	4.7	2.4	0.47	44.1
4	8	\$01	2.2	3.6	0.22	66.2
4	8	\$01	1.0	5.1	0.1	93.8

Note 1: $f_{REF} = f_{osc} / (REFDV + 1)$

$$f_{PLLCLK} = \frac{2 f_{XTAL} [SYNR + 1]}{[REFDV + 1]}$$

Equation 1 PLLCLK Frequency when PLL Locked

4 Clock Monitor

The clock monitor circuit is based on an internal resistor-capacitor (RC) time delay. If no oscillator (EXTALi) clock edges are detected within this delay time, the clock monitor can generate a microcontroller reset. Alternatively, if the V_{DDPLL} pin is connected to V_{DD} , the clock monitor can cause the PLL to enter the emergency Limp-home mode. If V_{DDPLL} is connected to V_{DD} , the clock monitor is enabled at reset, but may be disabled/enabled under software control by means of the CME and FCME bits in the COPCTL register. If V_{DDPLL} is connected to V_{SS} , the

clock monitor is disabled at reset but may be enabled/disabled under software control by means of the CME and FCME bits in the COPCTL register. Note that the FCME bit is write once after reset (in 'normal' modes).

There is a short delay from the point when the oscillator clock fails and its detection by the clock monitor circuit. If the microcontroller is clocked directly from the oscillator clock, there is a risk of spurious clock signals disrupting normal operation of the microcontroller during this time. This risk is eliminated if the microcontroller system clock is derived from the PLL. Once the oscillator clock has failed, the application software should take action to ensure that the microcontroller remains in a safe state, especially in the case of an intermittent failure.

The clock monitor must be disabled in order for the microcontroller to enter Stop or Pseudo-stop mode because the EXTALi clock is stopped in these modes.

5 Limp-home Mode

The emergency Limp-home mode allows the microcontroller to continue operation at a frequency f_{VCOMIN} in the event of a crystal/resonator oscillator failure or long oscillator startup time. This mode is available only if the V_{DDPLL} pin is connected to V_{DD} . In Limp-home mode, the PLLCLK frequency drops to the minimum frequency of the VCO. The PLLCLK drives ECLK, PCLK, MCLK, XCLK and BCLK at a frequency f_{VCOMIN} . Limp-home mode may be disabled under software control by means of the NOLHM bit in the PLLCR register. This bit is write once after reset (in 'normal' modes). The LHOME bit in the PLLFLG register is set when the microcontroller is in Limp-home mode and cleared when not in Limp-home mode. The LHIE bit in the PLLCR register enables the limp-home interrupt when set.

Exit from Limp-home mode occurs when the clock monitor circuit has detected EXTALi clock edges. However, although the clock monitor circuit can detect clock edges, it does not detect if the oscillator clock signal has a valid duty cycle or frequency.

It is recommended to shut down the microcontroller by executing the 'stop' instruction when Limp-home mode is entered.

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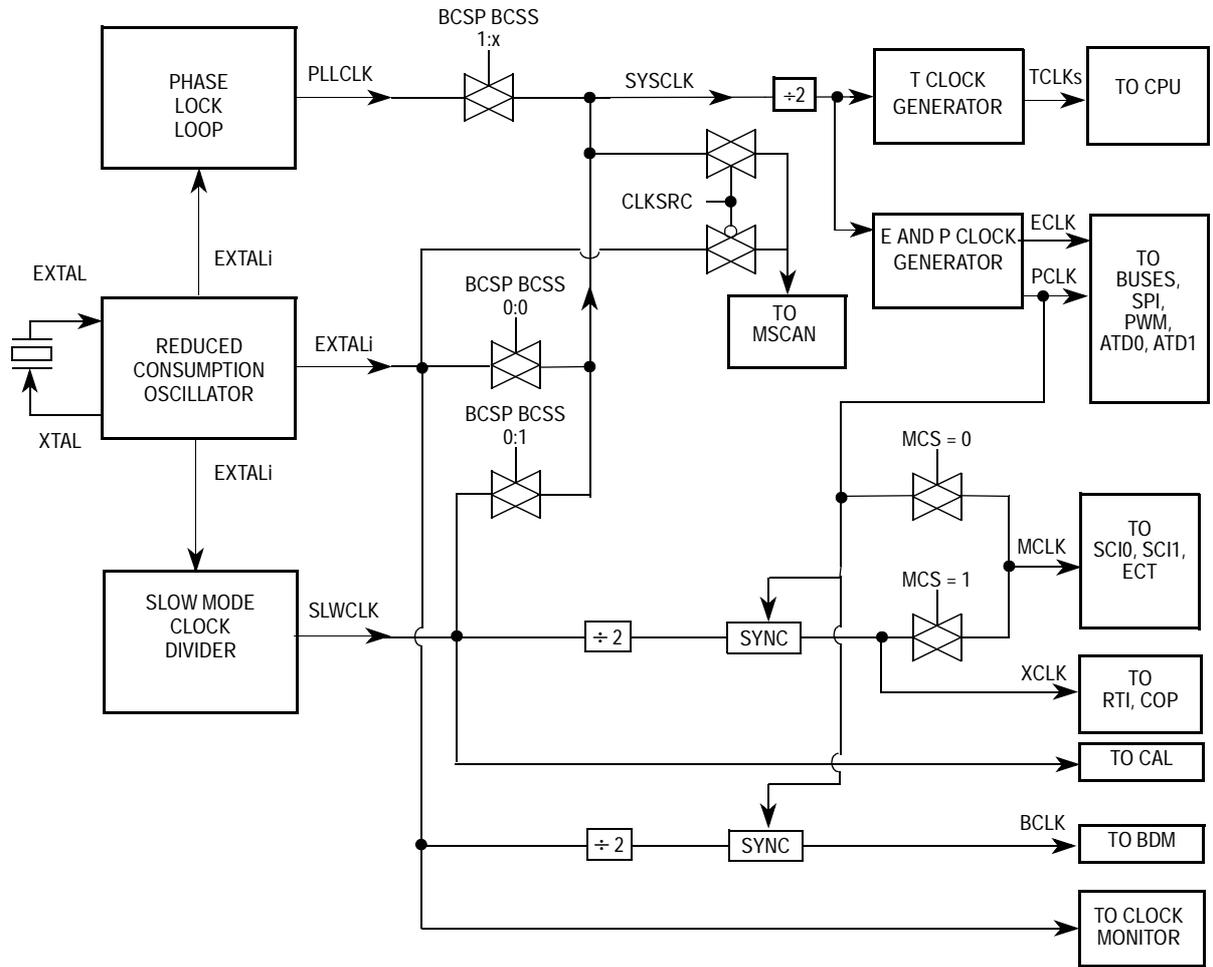


Figure 3 Clock Generation Chain

6 Effects of Oscillator Failure

The effect of an oscillator failure can be categorised according to the conditions under which the event occurs. The three situations are:

- At power-on reset
- During normal operation
- At exit from Stop or Pseudo-stop mode

The response to the oscillator clock failure depends on the state of the V_{DDPLL} pin and the clock configuration bits. The response to an oscillator failure in the three situations are described for different clock configurations in the sections below.

7 Clock Behaviour with PLL Disabled

V_{DDPLL} pin = V_{SS} level
XFC pin = floating or V_{SS} level

Connecting the V_{DDPLL} pin to V_{SS} disables the PLL and Limp-home mode. The clock monitor is disabled out of reset. ECLK is half the oscillator clock frequency. It is not possible to enable the PLL or to select the PLLCLK when the V_{DDPLL} pin is at V_{SS} level.

7.1 Power-on Reset

The microcontroller begins operation when the oscillator starts. Code execution begins after count of 4096 XCLK cycles (8192 EXTALi cycles). In order to prevent code execution beginning before the oscillator has stabilised, the RESET pin should be held low (V_{SS} level) for sufficient time to allow the oscillator to stabilise. If the oscillator fails before or during Power-on reset, the microcontroller stops operating.

7.2 Normal Operation

Oscillator failure during normal operation could result in improper operation of the microcontroller due to an unstable oscillator clock signal as the oscillator fails. To reduce this risk, the clock monitor and the COP watchdog should be enabled by software. The clock monitor is enabled by setting either the CME bit or the FCME bit in the COPCTL register (note FCME is write once after reset). Once enabled, the clock monitor will cause a reset if the oscillator clock should fail. The COP watchdog is enabled by writing a value other than '0' to the CR2...CR0 bits in the COPCTL register. Once enabled, software must prevent a COP reset by periodically writing \$55 followed by \$AA to the COPRST register.

Note that the microcontroller distinguishes between an internal reset (COP or clock monitor) and external reset by sampling the level on the reset pin about 24 ECLK cycles after it is driven low. If the level on the

reset pin is still low when it is sampled, an external reset is assumed. Thus, if external circuitry on the reset pin prevents the reset pin from rising within this time, the COP reset vector and the clock monitor reset vector will never be taken.

7.3 Stop Mode

In order to enter Stop mode, the clock monitor must be disabled: the CME and FCME bits in the COPCTL register must both be clear to disable the clock monitor. Also, the S bit in the condition codes register must be cleared to enable the 'stop' instruction. When the 'stop' instruction is executed all clocks to the microcontroller are stopped. If the PSTP bit in the PLLCR register is set then Pseudo-stop mode is entered and the oscillator continues to run.

Stop mode and Pseudo-stop mode is exited by means of an interrupt or an external reset. Only specific interrupts can cause exit from Stop and Pseudo-stop modes, these are IRQ, XIRQ, key wakeup, and MSCAN wakeup. The DLY bit in the INTCR register must always be set before entering Stop mode when using the internal oscillator. This ensures that a delay of 4096 XCLK cycles occurs before code is allowed to execute, this is to give sufficient time for the oscillator to stabilise after restarting. The microcontroller will resume operation more quickly if the PSTP bit is set before entering Pseudo-stop mode as the oscillator does not have to be restarted, but it is still recommended to set the DLY bit in the INTCR register.

If the oscillator fails during Stop or Pseudo-stop modes the microcontroller will not restart operation. If the oscillator partially fails, or does not stabilise during the 4096 XCLK delay time, there is a risk of improper operation of the microcontroller.

8 Clock Behaviour with PLL Enabled

V_{DDPLL} pin = V_{DD} level.
 XFC pin connected to 2nd order low-pass filter.

Connecting the V_{DDPLL} pin to V_{DD} enables the PLL, the clock monitor and Limp-home mode out of reset.

8.1 Power-on Reset

With the V_{DDPLL} pin at V_{DD} level, the PLL, clock monitor and Limp-home mode are enabled. The microcontroller (when configured for 'normal', as opposed to 'special', modes) starts up in Limp-home mode and the 4096 XCLK cycle count is started at the limp-home clock frequency, f_{VCOMIN} . If EXTALi clock edges are detected by the clock monitor circuit during the 4096 XCLK cycle count the Limp-home mode is exited immediately and the 4096 XCLK cycle count continues using the EXTALi clock instead of the PLLCLK. At the end of the 4096 XCLK cycle count reset is released and code execution begins with EXTALi selected for SYSCLK.

Note however, that although the clock monitor circuit can detect clock edges, it does not detect if the oscillator clock signal has a valid duty cycle or frequency. Therefore it is possible that with a slow starting oscillator the microcontroller may begin executing code from an oscillator clock which has not yet stabilised and improper operation may result. To avoid this issue, it may be necessary to hold the reset pin low with an external circuit for an extended period of time to allow the oscillator clock to stabilise – see errata AR627 in the latest Mask Set Errata for the appropriate microcontroller for more details.

If the oscillator has failed to start and the clock monitor has detected no edges at the end of the 4096 XCLK cycle count, the microcontroller remains in Limp-home mode and code execution begins at f_{VCOMIN} with the LHOME bit set. The clock monitor output is checked after another 4096 XCLK cycles and then again every 8192 XCLK cycles thereafter. If any oscillator clock edges are detected, Limp-home mode will be exited at the check point, clearing the LHOME bit and generating an interrupt if enabled by the LHIE bit.

It is recommended to check the status of the LHOME bit in the PLLCR register immediately at the start of code execution to determine if the oscillator has started. If the microcontroller is operating in Limp-home mode it must be decided whether it is safe to allow the microcontroller to continue operating, or to shut it down. It is recommended to shut down the microcontroller by enabling the stop instruction (clear the S bit in the condition codes register) and executing the 'stop' instruction. Refer to [8.3 Stop Mode](#) for different Stop mode scenarios.

There is a risk associated with allowing operation to continue in Limp-home mode due to the possibility of partial oscillator recovery leading improper operation.

8.2 Normal Operation

The response of the microcontroller to an oscillator failure during normal operation depends on the state of the NOLHM, CME and FCME bits.

8.2.1 Clock Monitor Disabled

CME and FCME = 0

This mode is not recommended as a normal operating mode and is included only for completeness. If the oscillator fails, the PLL no longer has a reference clock and the PLLCLK frequency will drop to the minimum VCO frequency. The LOCK bit in the PLLFLG register will be cleared and an interrupt generated if enabled by the LHIE bit. If the SYSCLK is derived from PLLCLK (BCSP = 1), the microcontroller will continue to operate at a frequency of $f_{VCO\text{MIN}}$. If, however, SYSCLK is derived from EXTALi (BCSP = 0), the microcontroller will stop operating. In both cases peripheral modules which require a clock derived from EXTALi will not operate. If the oscillator clock recovers, the PLLCLK will gradually recover to its target frequency.

8.2.2 Limp-home Mode Disabled, Clock Monitor Enabled

NOLHM = 1, CME or FCME = 1

If the oscillator fails, the clock monitor will generate a clock monitor reset and the microcontroller will be forced to the reset state. There may be a short delay from the point at which the oscillator fails to its detection by the clock monitor. Peripheral modules which require a clock derived from EXTALi may be affected during this time. The status of the NOLHM signal is latched throughout the clock monitor reset so the microcontroller does not start up in Limp-home mode. Reset clears the BCSP bit, i.e. EXTALi is selected for SYSCLK so the microcontroller will only restart if and when the oscillator clock recovers. An external reset will enable the microcontroller to restart in Limp-home mode. There is a risk of improper operation due to an unstable oscillator clock if the oscillator clock recovers.

8.2.3 Limp-home Mode Enabled, Clock Monitor Enabled

NOLHM = 0, CME or FCME = 1

Limp-home mode is entered if the oscillator fails and the microcontroller continues operation at $f_{V_{COMIN}}$, regardless of the state of the PLLON bit in the PLLCR register, the BCSP and MCS bits in the CLKSEL register, and the value of the SLOW register. The LHOME bit in the PLLFLG register is set to indicate operation in Limp-home mode. The clock monitor output is checked every 8192 XCLK cycles thereafter and if any oscillator clock edges are detected, Limp-home mode will be exited. It must be decided whether it is safe to allow the microcontroller to continue operating, or to shut it down. It is recommended to shut down the microcontroller by disabling all interrupts, enabling the stop instruction (clear the S bit in the condition codes register) and executing the 'stop' instruction. Refer to **8.3 Stop Mode** for different Stop mode scenarios.

There is a risk associated with allowing operation to continue in Limp-home mode due to the possibility of partial oscillator recovery leading improper operation.

8.3 Stop Mode

The response of the microcontroller to the 'stop' instruction with the V_{DDPLL} pin at V_{DD} level depends on the state of the PSTP, NOLHM, CME and FCME bits.

The DLY bit in the INTCR register must always be set before entering Stop mode when using the internal oscillator. This ensures that a delay of 4096 XCLK cycles occurs before code is allowed to execute, this is to give time for the oscillator to stabilise after restarting. It is recommended to set the DLY bit in the INTCR register before entering Pseudo-stop mode. The following descriptions of Stop/Pseudo-stop mode recover assume that the DLY bit is set.

Stop mode and Pseudo-stop mode are exited by means of an interrupt or an external reset. Only specific interrupts can cause exit from Stop or Pseudo-stop modes, these are IRQ, XIRQ, key wakeup, and MSCAN wakeup.

Application Note

8.3.1 Limp-home Mode Disabled, Clock Monitor Disabled

NOLHM = 1, CME and FCME = 0

Execution of the 'stop' instruction causes all clocks to the microcontroller to stop. If the PSTP bit is set before the 'stop' instruction is executed, the oscillator will remain running in Pseudo-stop mode.

On exit from Stop (or Pseudo-stop) mode the microcontroller begins operation with the BCSP bit determining the clock source for the 4096 XCLK cycle count delay. Code execution begins at the end of this delay time.

If the BCSP bit is clear, operation begins with the EXTALi clock selected. If the oscillator fails to start the microcontroller will not exit Stop mode and will not start operating. If the oscillator partially fails, or does not stabilise during the 4096 XCLK delay time, there is a risk of improper operation of the microcontroller.

If the BCSP bit is set, operation begins with the PLLCLK selected. In this case the SLOW register may be configured before entering Stop mode to extend the 4096 XCLK cycle count so that the PLL is already locked by the time code execution begins.

If the oscillator fails to start the microcontroller will exit Stop mode and start operation at f_{VCOMIN} (but not in Limp-home mode). Peripheral modules which require a clock derived from EXTALi will not operate.

8.3.2 Limp-home Mode Disabled, Clock Monitor Enabled

NOLHM = 1, CME or FCME = 1

Execution of the 'stop' instruction causes the clock monitor to detect an oscillator clock "failure" which immediately results in a system reset. Stop mode is not entered. The status of the NOLHM signal is latched throughout the clock monitor reset so the microcontroller continues operation from the clock monitor reset vector using the EXTALi clock for SYSCLK. Note that the microcontroller distinguishes between an internal reset (COP or clock monitor) and external reset by sampling the level on the reset pin about 24 E-clock cycles after it is driven low. If the level on the reset pin is still low when it is sampled, an external reset is assumed. Thus if external circuitry on the reset pin prevents the reset pin from rising within this time, the reset vector will be taken instead of the clock monitor reset vector.

8.3.3 Limp-home Mode Enabled

NOLHM = 0

If Limp-home mode is enabled when the ‘stop’ instruction is executed, the CME and FCME bits are disregarded and the clock monitor is disabled. All clocks to the microcontroller stop and the oscillator remains running only if the PSTP bit is set.

On exit from Stop mode the clock monitor is forced to be enabled and the microcontroller begins operation in Limp-home mode at f_{VCOMIN} . At the end of the 4096 XCLK cycle count the clock monitor status is checked before code execution begins. If the clock monitor has detected oscillator clock edges at the end of the 4096 XCLK cycle count, then Limp-home mode is exited immediately and code execution begins with the value of the BCSP bit determining the source of SYSCLK. If no clock edges have been detected, the microcontroller remains in Limp-home mode and code execution begins at f_{VCOMIN} with the LHOME bit set. The clock monitor output is checked after another 4096 XCLK cycles and again every 8192 XCLK cycles thereafter. If any oscillator clock edges are detected, Limp-home mode will be exited, clearing the LHOME bit and generating an interrupt if enabled by the LHIE bit.

If the microcontroller begins code execution in Limp-home mode it must be decided whether it is safe to allow the microcontroller to continue operating, or to shut it down. It is recommended to shut down the microcontroller by disabling all interrupts and executing the ‘stop’ instruction.

There is a risk associated with allowing operation to continue in Limp-home mode due to the possibility of partial oscillator recovery leading improper operation.

8.4 Summary of Recommended Configuration with PLL Enabled

8.4.1 Power-on Reset

The reset pin must be held low with an external circuit until the oscillator clock has stabilised.

8.4.2 Normal Operation

Clock monitor enabled (CME or FCME set).

Reset is required on clock failure: Limp-home mode disabled (NOLHM set).

Software shutdown is required on clock failure: Limp-home mode enabled (NOLHM clear).

8.4.3 Stop Mode

Conditions to be set before entering Stop mode:

- DLY bit set.
- EXTALi clock selected (BCSP bit clear).
- PSTP bit set for faster Stop mode recovery at the expense of increased current consumption.

No operation required if clock fails to start: Limp-home mode disabled (NOLHM bit set), clock monitor disabled (CME and FCME bits clear), EXTALi clock selected (BCSP bit clear).

Software shutdown required if clock fails to start: Limp-home mode enabled (NOLHM clear), PLLCLK selected (BCSP is set).

8.5 Summary of Terms

Set – bit or byte value equal to ‘1’

Clear – bit or byte value equal to ‘0’

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