

AN2257/D  
Rev. 0, 1/2002

Design Information for  
Migration to MPC8260  
Rev. C.2

This document presents information that may impact customers who are migrating to revision C.2 silicon from any of the previous revisions (Rev. A.1, B.2, B.3) of the MPC8260. Please be aware that this document will be updated as necessary. Customers are encouraged to take note of new editions of this document.

## ERRATA

A number of device errata have been eliminated in revision C.2 of the MPC8260; however, a few remain. Customers are highly encouraged to review the MPC8260 device errata document in detail to determine if and/or how these fixes impact their design work. This document can be located at the following web address:

<http://e-www.freescale.com/brdata/PDFDB/docs/MPC8260CESUMM.pdf>

## RAM MICROCODES

Note the following updates regarding appropriate usage of microcode packages in relation to certain microcode revisions.

Updates for microcode packages for sale should be obtained through your usual Freescale sales contact.

- A different AAL2 microcode package is required for revision C.2 than used in all previous revisions.
- Different SS7 microcode patches are required for revision C.2, A.1, and B.x devices.
- Revision B.2 requires a microcode patch for ATM internal rate operation. This patch is not required for revision C.2.
- Note that when using AAL1 in revision C.2, it is recommended that users do the following:
  - Program the RCT and TCT's AAL\_TYPE field to AAL1\_CES (b101) instead of the old regular AAL1 setting (b001)
  - Enable CES functionality if needed by setting the CESM field

Updated microcode documentation for revision C.2 is available by going to <http://www.freescale.com/semiconductors>, and clicking on "PowerQUICC" and then "Tools":

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